

Assistant Commissioner for Patents
Washington, D.C. 20231

In re: Patent Appln. USSN: 09/841,505 Filed: April 24, 2001 Action Day:
Oct 29, 2004
Title: CMOS tapered gate and synthesis method
Inventor(s): Brian W. Curran et al.
Examiner: Magid Y Dimyan Group Art: 5674
Attorney Docket No.: PO9-2000-0107US1
Attorney/Agent: Lynn L. Augspurger, Reg. No.: 24,227 Deposit Acct: 09-0463

Dear Sir:

State of New York
County of Dutchess

Affidavit under 37 CFR 1.131

The undersigned Lisa Bryant Lacey before the designated Notary Public declare that the following facts applicable to the above application are true:

That appended code illustrates script that is taken from a file kept in the ordinary course of business at International Business Machines Corporation and printed to correctly illustrate the script which we inventors created and which the undersigned Lisa Bryant Lacey wrote in 1995 to implement the inventions described and claimed in U.S. Serial No. 09/841,505 filed April 24, 2001 entitled " CMOS tapered gate and synthesis method" which was used by Yiu Hing Chan and others at International Business Machines Corporation for synthesis of a working device for testing and proving that the process claimed worked for the intended purpose in 1999 and prior to April, 2001.

Furthermore, the undersigned has also appended hereto an abstract sheet taken from the log showing the use by Yiu Hing Chan documenting 1999 calls to the appended code script which were used for the synthesis method claimed in our patent application which we signed as the the completed patent application filed with the US Patent and Trademark Office in March, 2001 describing and claiming the process implemented by the appended code script. In addition Lisa Bryant Lacey made the an added comment in the log appended to the affidavit of Yiu Hing Chan pointing out the invocation of the TAPERED code of the invention in the file made in order to allow focus on that invocation by a reader of the log.

I make this declaration of facts before the undersigned Notary Public for presentation as proof under 37 CFR 1.131 because the reference to "Hwang" mentioned in the first official action regarding this application of which reference the undersigned Brian W. Curran was an author was made and published after our invention was conceived and reduced to practice.

Sworn to and subscribed before me a Notary Public, in the town of Poughkeepsie, county of Dutchess, State of New York on this 23rd day of February 2005.

Lisa Bryant Lacey
Lisa Bryant Lacey

Sandra Lyn Kilmer
Sandra Lyn Kilmer

Notary Public
Dutchess County New York

SANDRA LYN KILMER
Notary Public, State of New York
No. 5562885
Qualified in Dutchess County
Commission Expires Sept 30, 2006

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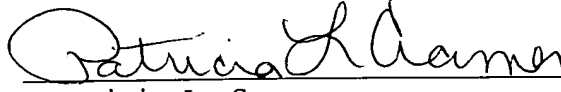
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Sworn to and subscribed before me a Notary Public, in the town of Poughkeepsie, county of Dutchess, State of New York on this 18th day of February 2005.


Brian W. Curran


Patricia L. Cramer
Notary Public
Dutches County, New York

PATRICIA L. CRAMER
Notary Public, State of New York
No. 4527213
Qualified in Dutchess County
Commission Expires 8/31/2006



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```

#
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#
# The source code for this program is not published or otherwise divested
# of its trade secrets, irrespective of what has been deposited within
# the U.S. Copyright Office.
#
#
# NAME:
#
#   tcl/late_time.tcl, BooleDozer, bdz-4.1 1.8 9/18/98 15:38:46
#
# AUTHOR / REVIEWER:
#
#   Michael Kazda
#
# DESCRIPTION:
#
#   Late timing correction Scenario
#
# MODIFICATIONS:
#
#   Date      UserID  Remark (newest to oldest)
#   -----
#   05/24/99 fvg    added cycle_steal 11 places. Saved dated backup
#   04/15/99 lbl    per dkung, num_clusters from (4) to (16) in lowvt
#   09/18/98 kazda  rename interlude due to collision
#   06/18/98 kazda  removed WORST from bufmatch,fanmatch
#                   removed NO_VIOLATIONS from faninv
#   06/15/98 kazda  added gain-based/window repowering
#   03/26/98 raze   str_parm not ued correctly.
#   02/23/98 kazda  added progress metering
#   02/16/98 kazda  reset tc parm offset to zero on exit
#   11/19/97 raze   syntax error, invalid command substitution
#   06/27/97 - MAK  - Correct randsim query before invoking
#   06/16/97 - MAK  - Added final fanout correction after dinv to correct
#                   any violations introduced by dinv or onebuff
#                   Correct delay_synlimit for medium in various places.
#   05/30/97 DJG    Added checksrc to beginning of scenario
#   03/27/97 DJG    Added INFO_ONLY flag to first checkfan call so as
#                   not to set the error level.
#   02/20/97 HC     Added reset_timing.
#   11/01/96 CKH    Replacing noncritical repower option LOWEST with
#                   LOWEST_NOT_EQUAL, which seems to give a big speedup
#   03/05/96 DJG    Try to get some statistics
#   11/08/95 - NDH  - Based upon debugging by Andy, always use fastpwr()
#                   instead of quick(repower) initialy.
#   10/17/95 - NDH  - Added tpushb() and tsteal() to main restructuring loop.

```

```

# 08/30/95 - NDH - Added randsim query before doing actual check
# 08/16/95 - DJG - Added sweep after delBufClks
# 07/28/95 - DSK - Added calls to Tony's tempBufClks and delBufClks when
#                 delay_lim >=4 and ! dont_bufclks
# 07/26/95 - NDH - Added tc_parm( CHK_SINKSLEW( X ) ) where X="N" when
#                 we set slew prop to false and X="Y" when we set
#                 slew prop to true. This will ensure that we
#                 accurately measure slew times for fanout correction.
# 6/14/95 - DJG - Removed args to late_area.scn it doesn't seem to
#                 take any anymore.
# 1/10/95 - DJG - Added checkfan call right before SLEW calculation
#                 turned on.
# 11/07/94 - LNR - Quit if technology is XC4000 or XC3000 or QSV
# 10/04/94 - Chao- Added final slew correction with LTOR order.
# 08/31/94 - DJG - Change ATTEMPS to 0 in two places for final legal
#                 fanout correction. 0 is infinite number of tries.
# 02/17/94 - DJG - Changed to ! new_assert so users will not see change
#                 unless they want it.
# 02/07/94 - RLK - Changed call to assert(SLEW/NOSLEW) to set_slew_prop
#                 unless is_parm("old_assert") is true.
# 10/20/93 - DJG - remove traceset before trulegen
# 09/15/93 - JRK - Added chkbuff before the last checkfan

```

```

proc late_time {use_sink_limit use_cap_limit args} {
    set delayEffort [get_default_delay_synlimit]
    set areaEffort [get_default_synlimit]

    # initialize some variables here
    set gain_based 0

    set args_num [llength $args]
    # run through the extra argumentes for late timing correction
    for { set i 0 } { $i < $args_num } { incr i } {
        set arg [lindex $args [expr $i]]
        switch -regexp -- $arg {
            -gain.*      { set gain_based 1 }
            default      { error "Parameter not recognized" ?$arg?; }
        }
    }
}

echo "In David's Exp. Timing Opt Scenario"
checkfan
if ($gain_based) {
    echo "Gain-based Late Time"
    lx_progress_update 0 "Gain-based Late Timing Correction..."
} else {
    echo "Standard Late Time"
    lx_progress_update 0 "Late Timing Correction..."
}
echo "Delay Effort = $delayEffort"
echo "Area Effort = $areaEffort"

#cputime

#set the trace level to HOWMANY

```

```

#traceset "syntrace HOWMANY"

echo "initialize window repower"
if {$CTE::use_tapered} {
    hide_tapered -clear
}
if {$CTE::use_lowvt} {
    hide_lowvt -clear
}
init_gain_based_repower "REPOWER_INTERVAL(8)"

# Check if there are any rules to unhide
set unhidden [str_parm "unhide_rules"]
if { [string compare $unhidden ""] != 0 } {
    unhide_rules $unhidden
}

#hide xpansion defs
hide_def_with_view "XPANDVIEW,SRULE"

#clear all hidden flags created by the synthesis process
syn_hide_boxes_clear
copy_hide

#traceset "syntrace NOTRACE"
trulegen
traceset "syntrace HOWMANY"

# set the max fanout value if one is in the parm file
setmaxfanout

# set the max number of icells this design can grow to
set_maxarea

#clear all hidden mapping flags
nextbox "syn_hide_set(!HIDE_DOMINANT)"

#do interlude timing measurements
lt_interlude
checksrc

#set timing mode to NOSLEW
if {![is_parm "new_assert"]} {
    assert "NOSLEW"
} else {
    set_slew_prop "OFF"
    tc_parm "CHK_SINKSLEW(N)"
}

#initial timing parameter set up
tc_parm "PINTYPE(OUTPUT_PIN),OFFSET(0)
MARGIN(0),ATTEMPTS(1),ITERATIONS(1),FUZZY(.01),MAX_CRIT(32)"
if {[info exists env(Low_POWER)]} {
    tc_parm "USE_POWER,BENEFIT_UNITS(0)"
} else {

```

```

    tc_parm "USE_AREA,BENEFIT_UNITS(0)"
}

#if delay limit 0 then simply return
if {$delayEffort <= 0} {
    return
}

# Buffer clock nets to improve run time!          ADD 19Dec94
# if {[is_parm "dont_bufclks"]} {
#     nextbox "tempBufClks"
# }

measure

tc_parm "SLEW_LIM(100)"
if {$use_sink_limit > 0} {
    tc_parm "SINK_LIM(100)"
}
if {$use_cap_limit > 0} {
    tc_parm "CAP_LIM(100)"
}
if [info exists CTE::cycle_steal] {
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
}
techredund "EQNVIEW"
simple_map
critical "repower(SCORE(ALL),INC,NO_VIOLATIONS) ,
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"

#checkfan
write_end_point_report -points 3 -paths 1

measure
# write_comprehensive_report -file "bpaths.rpt" -detail -audit
traceset "repower_paths HOWMANY"
#traceset "syntrace DEBUG"
#traceset "init_gain_based_repower WHEREWHAT"
tc_parm "MARGIN(10000000)"
repower_paths "FUZZY(0.02)"
write_end_point_report -points 3 -paths 1
#quit;

#tapered_critical

measure

lx_progress_update 3 "Initial Logic Cleanup..."

#initialize cleanup of logic
# tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),OFFSET(-1000)"
# quick "onebuff(SCORE(ALL),NO_VIOLATIONS),dinv(SCORE(ALL),NO_VIOLATIONS)"
measure
quick "tcte(SCORE(ALL),NO_VIOLATIONS)"
measure

```

```

if {$use_sink_limit > 0} {
    tc_parm "SINK_LIM(200)"
}
if {$use_cap_limit > 0} {
    tc_parm "CAP_LIM(200)"
}

#set capacitance and sink limits
if {$use_sink_limit > 0} {
    tc_parm "SINK_LIM(100)"
}
if {$use_cap_limit > 0} {
    tc_parm "CAP_LIM(100)"
}

lx_progress_update 5 "Initial Pin Swapping..."

if [info exists CTE::cycle_steal] {
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbos
}
#initial pin swapping
fanmatch "ESTIMATED, SORT, ONE_LEVEL"
measure
treematch "ESTIMATED, TWO_LEVEL, NO_VIOLATIONS"

measure
pad_pos
# load_xrule -file "/afs/apd/func/vlsi/alliance00/bssc8/prod/xrule/bssc8.xrule"
nextbox "synexpand(XPANDVIEW)"
measure

write_end_point_report -points 3 -paths 1

if {$delayEffort >= 4 && $areaEffort <= 6} {

    lx_progress_update 41 "Expand AO and merge..."

    #perform an initial expand AO and merge
    add_r_off
    tc_parm
    "WEIGHTED_BENEFIT(1), ATTEMPTS(1), ITERATIONS(1), WEIGHTED, DEFAULT_POWER_SCORE(AL
    L)"
    quick
    "texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WORST, SIMILAR, VIEW(TRULE_BASE_A
    UTOGEN), NO_VIOLATIONS)"

    add_r_off
    tc_parm
    "WEIGHTED_BENEFIT(1), ATTEMPTS(1), ITERATIONS(1), WEIGHTED, DEFAULT_POWER_SCORE(AL
    L)"
    quick "texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WORST
    , VIEW(TRULE_BASE_AUTOGEN) NO_VIOLATIONS)"

    add_r_off
    tc_parm

```

```
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(ALL)"
```

```
    quick
```

```
"texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST,SIMILAR,VIEW(TRUE_AND_OR_AUTOGEN)    ,NO_VIOLATIONS)"
```

```
    add_r_off
```

```
    tc_parm
```

```
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(ALL)"
```

```
    quick "texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST,VIEW(TRUE_AND_OR_AUTOGEN)    ,NO_VIOLATIONS)"
```

```
    add_r_off
```

```
    tc_parm
```

```
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(ALL)"
```

```
    quick "tmerge(SCORE(ALL),ORD2,SORT_PINS,NO_VIOLATIONS)"
```

```
}
```

```
if [info exists CTE::cycle_steal] {
```

```
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
```

```
}
```

```
write_end_point_report -points 3 -paths 1
```

```
lx_progress_update 131 "Powerup..."
```

```
measure
```

```
critical
```

```
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED,REPOWER(EXTERNAL)),faninv(LIMITED,REPOWER(EXTERNAL))"
```

```
    nextbox "synexpand(XPANDVIEW)"
```

```
measure
```

```
if [info exists CTE::cycle_steal] {
```

```
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
```

```
}
```

```
write_end_point_report -points 3 -paths 1
```

```
echo "Finished initial power up"
```

```
# write_end_point_report -points 3 -paths 1
```

```
# checkfan
```

```
lx_progress_update 279 "Pin swapping..."
```

```
#swap pins after repowering
```

```
fanmatch "ACTUAL,ONE_LEVEL,NO_VIOLATIONS"
```

```
lx_progress_update 301 "Powering up critical path..."
```

```
#initial powerup
```

```
add_r_off
```

```
if {$delayEffort >= 7} {
```

```

    tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RANK(5)"
  } else {
    tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1)      "
  }
  while {1} {
    reset_critical_slack_limit
    repower_paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC,NO_VIOLATIONS) ,
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0} {
      break
    }
  }

  if [info exists CTE::cycle_steal] {
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  }
  write_end_point_report -points 3 -paths 1

  if {$delayEffort >= 5} {
    tc_parm
    "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    if {![has_dual_rail_children "NAND"] ||
[has_dual_rail_children "NOR"]}] {
      #nextbox "tt2lev(TIMING,TECH,CRITICAL,PATTERN_LIMIT(4),FANOUT_LIMIT(1))"
      lx_progress_update 301 "Recovering and Kernel Factoring..."

      # find recovering from two level boxes
      nextbox "findtt(TWO_LEVEL,BOX(2),LIMITED)"
      nextbox "findtt(TWO_LEVEL,BOX(3),LIMITED)"
      if {$areaEffort >= 7} {
        nextbox "findtt(TWO_LEVEL,BOX(4),LIMITED)"
        nextbox "findtt(TWO_LEVEL,BOX(5),LIMITED)"
      }
      nextbox "tkern"
      add_r_off
      tc_parm
      "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
      nextbox "powerize"
      quick "trecover(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO1FAN,NO_VIOLATIONS)"
    }

    if {$delayEffort >= 7 && $areaEffort <= 6} {
      add_r_off
      tc_parm
      "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
      quick "texpand(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,
WORST,SIMILAR,VIEW(TRUEL_BASE_AUTOGEN),NO_VIOLATIONS)"
      add_r_off
      tc_parm
      "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"

```

```

        quick "texpend(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,        WORST,
VIEW(TRUE_BASE_AUTOGEN),NO_VIOLATIONS)"
        add_r_off
        tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
        quick "texpend(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,
WORST,SIMILAR,VIEW(TRUE_AND_OR_AUTOGEN),NO_VIOLATIONS)"
        add_r_off
        tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
        quick "texpend(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,        WORST,
VIEW(TRUE_AND_OR_AUTOGEN),NO_VIOLATIONS)"
        add_r_off
        tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
        quick "tmerge(SCORE(ALL),RE_POWER,INC,ORD2,SORT_PINS,WORST,NO_VIOLATIONS)"
    }
}

measure

critical
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS),fantom(LIMITED,REPOWER(EXTERNAL)),faninv(LIMITED,REPOWER(EXTERNAL))"
nextbox "synexpand(XPANDVIEW)"
measure
if [info exists CTE::cycle_steal] {
cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
}
write_end_point_report -points 3 -paths 1

lx_progress_update 667 "Pin Swapping..."

#swap pins in trees
treematch "ACTUAL ,TWO_LEVEL,NO_VIOLATIONS"

#swap pins on box
fanmatch "ACTUAL ,ONE_LEVEL,NO_VIOLATIONS"

lx_progress_update 690 "Powerup..."

#more powerup
add_r_off
if {$delayEffort >= 7} {
tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,RANK(5 )"
} else {
tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED        "
}
while {1} {
reset_critical_slack_limit
repower_paths "FUZZY(0.02)"
critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),

```



```

repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
  if {[compare_critical_slack_limit] == 0} {
    break
  }
}

for {set i 0} {$i < 8} {incr i} {
  if {[syntrace] >= 10} {
    lt_interlude
  }

  echo "inside loop"
  measure
  write_end_point_report -points 3 -paths 1

  reset_critical_slack_limit
  #run all timing correction transforms under critical
  add_r_off
  if {$delayEffort >= 8} {
    tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RANK(5
),DEFAULT_POWER_SCORE(ALL)"
  } else {
    tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),
DEFAULT_POWER_SCORE(ALL)"
  }

  hide_all -no_clear
  hide_nominal_optbeta -clear

  scriptflow "trestructure_tree( MAX_INPUTS( 16 ) MAX_DECOMPOSE( 4 ) SORT_PINS
CHECK_INPUTS MIN_INPUTS( 2 ) )"

  hide_nominal -clear
  if {$CTE::use_tapered} {
    hide_tapered -clear
  }
  if {$CTE::use_lowvt} {
    hide_lowvt -clear
  }

  #do critical path analysis of all structural transforms
  critical "tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)"
  critical "tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,UP,NO_VIOLATIONS)"
  critical "tpushl(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
  critical "tpushr(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
  critical "tpushb(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
  critical "texpand(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,SIMILAR,\
VIEW(TRUE_BASE_AUTOGEN),NO_VIOLATIONS)"
  critical
  "texpand(SCORE(ALL),PUSH,COMPLEMENT,RE_POWER,FASTEST,SORT_PINS,SIMILAR,\
VIEW(TRUE_BASE_AUTOGEN),NO_VIOLATIONS)"
  critical "texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
  critical "tbmove(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,MULTIPLE_CRITICAL,\
INVERTC,CLONE,NO_VIOLATIONS)"
  critical "tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,DOWN,NO_VIOLATIONS)"

```

```

critical
"tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tncube(SCORE(ALL),NO_VIOLATIONS)"
repower_paths "FUZZY(0.02)"
repower_paths "FUZZY(0.02), SIMULTANEOUS_REPOWER"
critical "repower(SCORE(ALL),FASTEST,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
critical "clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS)"

critical "onebuff(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS),\
dinv(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS)"
critical "tcte(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS)"

critical "speedreg(RE_POWER),absrbreg()"
noncritical "speedreg(RE_POWER),absrbreg()"

hide_all -no_clear
hide_nominal_optbeta -clear

scribflow "trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS
CHECK_INPUTS MIN_INPUTS( 2 ) )"

hide_nominal -clear
if {$CTE::use_tapered} {
hide_tapered -clear
}
if {$CTE::use_lowvt} {
hide_lowvt -clear
}
}
if {[compare_critical_slack_limit] == 0} {
#lower repower books
if {$delayEffort <= 3 || $areaEffort >= 4} {
tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFFSET(0)"
noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
} else {
tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
}
}
tc_parm "MARGIN(10000000)"
fanmatch "ACTUAL ,ONE_LEVEL,NO_VIOLATIONS"
tc_parm "OFFSET(0)"
tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED"
tc_parm "REGALL"
repower_paths "FUZZY(0.02)"
critical "repower(SCORE(ALL),FASTEST ,NO_VIOLATIONS),
repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
if {[compare_critical_slack_limit] == 0} {
break
}
}
}

measure

critical

```

```

"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED,REPOWER(EXTERNAL)),faninv(LIMITED,REPOWER(EXTERNAL))"
nextbox "synexpand(XPANDVIEW)"
measure
repower_paths "FUZZY(0.02)"
critical "repower(SCORE(ALL),FASTEST,NO_VIOLATIONS),
repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA))"

if [info exists CTE::cycle_steal] {
cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
}
write_end_point_report -points 3 -paths 1

#do interlude timing measurements
lt_interlude

lx_progress_update 1916 "Powering down noncritical paths..."

#lower repower books
if {$delayEffort <= 3 || $areaEffort >= 4} {
tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFFSET(0)"
noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
} else {
tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
}
tc_parm "MARGIN(10000000)"

lx_progress_update 1919 "Pin Swapping..."

#pin swapping
bufmatch "ESTIMATED,TWO_LEVEL,NO_VIOLATIONS"
fanmatch "ACTUAL,ONE_LEVEL,NO_VIOLATIONS"

#fix dual rail boxes, swap pins and repower
if {$delayEffort >= 4} {
add_r_off
tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(ALL)"
if {!$gain_based} {
quick "tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)"
}

#swap pins and repowering
if ($gain_based) {
tc_parm "BENEFIT_UNITS(10)"
}
tc_parm "OFFSET(0)"
tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED"
while {1} {
reset_critical_slack_limit
critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
tc_parm "REGALL"
repower_paths "FUZZY(0.02)"
}

```

```

        critical "repower(SCORE(ALL),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
        if {[compare_critical_slack_limit] == 0} {
            break
        }
    }
    if ($gain_based) {
        tc_parm "BENEFIT_UNITS(0)"
    }
}

```

```

#checkfan
write_end_point_report -points 3 -paths 1
#check that the network has legal connections
nextbox "chklegal"
nextnet "chklegal"

```

```

#reduce area if possible
late_area

```

```

#checkfan
if [info exists CTE::cycle_steal] {
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
}
write_end_point_report -points 3 -paths 1

```

```

lx_progress_update 1977 "Checking violations..."

```

```

# check before turning on SLEW propagation
#checkfan "INFO_ONLY"

```

```

#set timing mode to SLEW
if {[is_parm "new_assert"]} {
    assert "SLEW"
} else {
    set_slew_prop "ON"
    tc_parm "CHK_SINKSLEW( Y)"
}
tc_parm "SLEW_LIM(100)"

```

```

lx_progress_update 1977 "Correcting violations..."

```

```

#final legal fanout correction
if {$use_sink_limit > 0} {
    tc_parm "SINK_LIM(100)"
}
if {$use_cap_limit > 0} {
    tc_parm "CAP_LIM(100)"
}

```

```

critical
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED,REPOWER(EXTERNAL)),faninv(LIMITED,REPOWER(EXTERNAL))"
nextbox "synexpand(XPANDVIEW)"
while {1} {

```

```

    reset_critical_slack_limit
    critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
    tc_parm "REGALL"
    repower_paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0} {
        break
    }
}

if {$CTE::use_tapered} {
    #runs tapering on a critical path
    tapered_critical
}

#final swapping and repowering for speed
if {$delayEffort >= 4} {

    lx_progress_update 1980 "Final Swapping and Repowering..."

    tc_parm "OFFSET(0)"
    tc_parm
    "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    nextbox "tkern"
    nextbox "powerize"
    quick "trecover(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,NO1FAN,NO_VIOLATIONS)"
    while {1} {
        reset_critical_slack_limit
        critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
        tc_parm "REGALL"
        repower_paths "FUZZY(0.02)"
        critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
        if {[compare_critical_slack_limit] == 0} {
            break
        }
    }
}

if [info exists CTE::cycle_steal] {
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
}
    write_end_point_report -points 3 -paths 1

    hide_all -no_clear
    hide_nominal_optbeta -clear

    scritflow "trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS
CHECK_INPUTS MIN_INPUTS( 2 ) )"
    hide_nominal -clear
    if {$CTE::use_tapered} {
        hide_tapered -clear
    }
    if {$CTE::use_lowvt} {

```

```

    hide_lowvt -clear
}

#run transforms under slew
tc_parm "OFFSET(0)"
tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1)"
critical "texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
if {$delayEffort >= 5} {
    if {$delayEffort >= 8} {
        #run all transforms one last time
        critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
        critical "tshatter(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO_VIOLATIONS)"
        critical
        "tmerge(SCORE(ALL),RE_POWER,INC,ORD2,SORT_PINS,NO_VIOLATIONS),texpand(SCORE(ALL),PUSH,RE_POWER,INC,SORT_PINS,SIMILAR,NO_VIOLATIONS)"
        critical
        "tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tncube(SCORE(ALL),NO_VIOLATIONS)"
        critical
        "onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)"
        critical "tcte(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)"
        if {0} {
            # fanout correction without apportionment
            gb_fancorr 0
        } else {
            critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS)"
        }
        critical "speedreg(RE_POWER),absrbreg()"
        noncritical "speedreg(RE_POWER),absrbreg()"
    } else {
        #get rid of odd books on critical paths
        critical
        "texpand(SCORE(ALL),PUSH,RE_POWER,INC,SORT_PINS,SIMILAR,VIEW(TRUEL_BASE_AUTOGEN),NO_VIOLATIONS)"
        tc_parm "REGALL"
        critical "repower(SCORE(ALL),INC,NO_VIOLATIONS)"
    }
}

lx_progress_update 2060 "Correcting violations..."

}

echo "doing last techredund"
traceset "syntrace HOWMANY"
techredund "EQNVIEW"
simple_map

critical
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED,REPOWER(EXTERNAL)),faninv(LIMITED,REPOWER(EXTERNAL))"
nextbox "synexpand(XPANDVIEW)"

```

```

#traceset "repower_paths DEBUG"
while {1} {
    reset_critical_slack_limit
    critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
    tc_parm "REGALL"
    repower_paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0} {
        break
    }
}

#traceset "dinv DEBUG"
tc_parm "SLEW_LIM(120),CAP_LIM(120), SINK_LIM(120)"
critical
"onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),dinv(SCORE(ALL),RE_POWER,INC,NO_VI
OLATIONS)"
tc_parm "SLEW_LIM(100),CAP_LIM(100), SINK_LIM(100)"
critical "clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS)"

#traceset "pushxor DEBUG"
pushxor "NUM_CLUSTERS(8)"

#checkfan
if [info exists CTE::cycle_steal] {
    cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
}
write_end_point_report -points 3 -paths 1

lx_progress_update 2061 "Removing unnecessary buffers..."

#removal of buffers with one fanout
if {$delayEffort <= 3 || $areaEffort >= 4} {
    tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFFSET(0)"
    noncritical "onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
    noncritical "dinv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
} else {
    tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
    noncritical "onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
    noncritical "dinv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
}

lx_progress_update 2061 "Correcting violations..."

#checkfan
write_end_point_report -points 3 -paths 1

if {$CTE::use_tapered} {
    #runs lowvt on a critical path
    lowvt_critical
}

if {$CTE::use_tapered} {

```

```

#runs tapering on a critical path
tapered_critical
}

if {$CTE::use_tapered} {
#runs lowvt on a critical path
lowvt_critical
}

write_end_point_report -points 3 -paths 1

#traceset "repower_paths DEBUG"
critical "clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS)"
while {1} {
reset_critical_slack_limit
critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
tc_parm "REGALL"
repower_paths "FUZZY(0.02), SIMULTANEOUS_REPOWER"
repower_paths "FUZZY(0.02)"
critical "repower(SCORE(ALL),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
if {[compare_critical_slack_limit] == 0} {
break
}
}
if {$CTE::use_tapered} {
#runs lowvt on a critical path
lowvt_critical
}

if [info exists CTE::cycle_steal] {
cycle_steal -iterations 30 -epsilon 1 -no_verbose
}
write_end_point_report -points 3 -paths 1

#make sure you get rid of double buffers
chkbuff

#compute the number of inverters following IOPADs and REGs
dualcnt "REG"
dualcnt "IOPAD"

#check that the network has legal connections
dual_rail_to_single_rail
nextbox "chklegal"
nextnet "chklegal"

#check that network has no anomalies
checksrc

#find double buffers
nextbox "dbuff()"

#
reset_timing

```



```

#check fanout
checkfan

# Remove clock buffers added at the top of this scenario.  ADD 19Dec94
# if {[is_parm "dont_bufclks"]} {
#     nextbox "delBufClks"
#     sweep "1"
# }

lx_progress_update 2068 "Measuring..."

#do measure
measure

#do final interlude timing measurements
slackhist
prtdelay
lt_interlude

#run randsim
if {[randsim "q"] != 0} {
    randsim "c"
}

##cputime

# Try to get some statistics
good_names
}

# Add Relative Offset
proc add_r_off {} {
    # switch to relative offset depending on synlimit
    switch -regexp [get_default_delay_synlimit] {
        [0-3] { tc_parm "RELATIVE_OFFSET(100)" }
        [4-6] { tc_parm "OFFSET(0)" }
        [7-9] { tc_parm "OFFSET(-0.01)" }
        default { tc_parm "OFFSET(0)" }
    }
}

# Timing Interlude Scenario
proc lt_interlude {} {
    #cputime

    #print the worst slack report
    write_end_point_report -points 10

    #check fanout correction
    #checkfan();

    #do measure
    measure

    #check the random simulator

```

```

if {[randsim "q"] != 0} {
    randsim "c"
}
}

proc gb_fancorr {apportion} {
    echo "Gain-based fanout correction apportion=$apportion"

    assign_wire_cap
    checksrc
    randsim "c"
    if ($apportion) {
#ALLISPECIAL
        gb_apportion_fanouts "SCALE_INCR(0.6), MIN_BOX_SCALE(0.010), SLACK_TARGET(0.02),
ACC_FACTOR(3.0), USE_INV"
    } else {
#ALLISPECIAL
        gb_apportion_fanouts "SCALE_INCR(0.6), NO_APPORTION, MIN_BOX_SCALE(0.010),
SLACK_TARGET(0.02), ACC_FACTOR(3.0), USE_INV"
    }
    checksrc
    assign_wire_cap
    randsim "c"
# write_end_point_report -points 1

    gb_buffer_tree "GAIN_INCR(0.2), CHECK, LOAD_FRAC(0.6), UPPER_GAIN(6.0),
NUM_SLACK_INCR(4), USE_INV"

    checksrc

    nextbox "printbox"
    write_comprehensive_report

    assign_wire_cap
    randsim "c"
# measure ""
}

# Tapering the cells
proc tapered_critical {} {

    for {set i 0} {$i < 20} {incr i} {
        reset_critical_slack_limit

        quick "tswap(SCORE(ALL),ACTUAL,ONE_LEVEL)"

        tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RANK(5)"
        critical "repower(SCORE(ALL),REPOWER_GROUP(TAPERED),TAPERED_PIN_SWAP)"
        critical "repower(SCORE(ALL),NO_VIOLATIONS)"
        critical "repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(BETA))"

        tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
        noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
        tc_parm "MARGIN(10000000)"

        if {[compare_critical_slack_limit] == 0} {

```

```

        break
    }
}

}

# Lowvt conversion of cells
proc lowvt_critical {} {

    #traceset "repower_paths DEBUG"
    for {set i 0} {$i < 10} {incr i} {
        reset_critical_slack_limit
        write_end_point_report -points 5;
        repower_paths "FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)"
        write_end_point_report -points 5;
        if {[compare_critical_slack_limit] == 0} {
            break
        }
    }
    traceset "repower_paths HOWMANY"
}

```

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Be it known that in connection with my accompanying affidavit and log file appended to an affidavit of Yu-Hing Chan, I, Lisa Bryant Lacey, retrieved the following lines of information, to help clarify. I added a comment in the log "*****POU92000-0107US1***** code invocation" that should the reader of these pages.

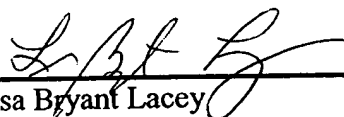
*****POU92000-0107US1***** code invocation

```
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
          > critical
repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPER...
critical( repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPERED_PIN_SWAP)
);
-1865.06 Avg: -167.73
maximum area for proto box IDCDSUC is 4606
repower: setting SCORE option to ALL.
repower: setting TAPERED_PIN_SWAP option.
```

Also, to document the date, note that the log maintains the date when run

*****POU92000-0107US1***** code invocation date

Sun Apr 18 21:58:17 1999
Part : IDCDSUC



Lisa Bryant Lacey

Sworn to and subscribed before me, this 23rd day of February, 2005
At Poughkeepsie, New York.



Sandra Kilmer, Notary Public, Dutchess County, New York

LYN

SANDRA LYN KILMER
Notary Public, State of New York
No. 5562885
Qualified in Dutchess County
Commission Expires Sept 30, 2006

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Assistant Commissioner for Patents
Washington, D.C. 20231

In re: Patent Appln. USSN: 09/841,505 Filed: April 24, 2001 Action Day:
Oct 29, 2004
Title: CMOS tapered gate and synthesis method
Inventor(s): Brian W. Curran et al.
Examiner: Magid Y Dimyan Group Art: 5674
Attorney Docket No.: PO9-2000-0107US1
Attorney/Agent: Lynn L. Augspurger, Reg. No.: 24,227 Deposit Acct: 09-0463

Dear Sir:

State of New York
County of Dutchess

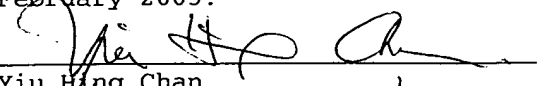
Corroborating Affidavit under 37 CFR 1.131

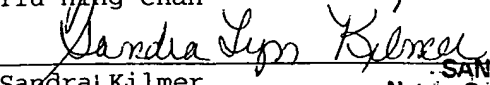
The undersigned Yiu Hing Chan before the designated Notary Public declare that the following facts applicable to the above application are true:

That I am a design engineer for International Business Machines Corporation and that the appended log printed from a log of work showing me using a tool which I used in 1999 when I was employed by International Business Machines Corporation, Poughkeepsie, New York, for testing the synthesis of working devices in accordance with a new method described in the aforementioned application and claims which I have read and understood. The appended log is a print from the log file kept by International Business Machines Corporation of my work and shows that in 1999 I personally used the code written by Lisa Bryant Lacey to implement the inventions described and claimed in U.S. Serial No. 09/841,505 filed April 24, 2001 entitled " CMOS tapered gate and synthesis method" and which I and others at International Business Machines Corporation used for synthesis of a working device for testing and proving that the process claimed worked for the intended purpose in 1999 and prior to April, 2001, and I say that the method of synthesis worked for me for the intended purpose in 1999 in accordance with the steps recited in the claims of US Patent Application Serial No. 09/841,505 which I have read and understand. Note that this log has an added comment pointing out the invocation of the TAPERED code of the invention in the file made in order to allow focus on that invocation by a reader of the log where the first line is Login: *BATCH*
ibm5081 bsp5n11

I make this declaration of facts before the undersigned Notary Public for presentation as proof under 37 CFR 1.131 in the aforesaid application because the reference to "Hwang" mentioned in the first official action regarding this application of which inventor Brian W. Curran was an author was made and published after the invention was conceived and reduced to practice of my own knowledge.

Sworn to and subscribed before me a Notary Public, in the town of Poughkeepsie, county of Dutchess, State of New York on this 19 day of February 2005.


Yiu Hing Chan


Sandra Lyn Kilmer
Notary Public

Dutchess County New York

SANDRA LYN KILMER
Notary Public, State of New York
No. 5562885

Qualified in Dutchess County
Commission Expires Sept 30, 2006

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Login: *BATCH* ibm5081 bsp5n11
Initializing environment for the Alliance 00 project (apd) ...
Initialized for apd...
Initializing for CHIPID=alliance00_cp ...
CTE: Initializing CTE environment @ apd.pok.ibm.com ...
CTE: Customizing CTE environment for project: alliance00 ...
CTE: Customizing CTE environment via user ./cterc ...
running: /afs/watson/projects/vlsi/cte/tools/bd2/0401v2/booledozer/4.1/bin/bdz -source ctesynz_cp.tcl

BooleDozer Logic Synthesis

Version 4.1 for AIX 4.1
Nutshell version 1.672 (03-25-1999)

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IBM and BooleDozer are Trademarks of IBM Corporation

Install Directory: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0
Machine: bsp5n11, AIX 4.1 32bit, 595 POWER2 (L1 i32k d128k, L2 0k), 1 cpu
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/.bdz
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_site_init.tcl
[CTE::site_init]: Starting cte Bdz under Nutshell site customization...
[CTE::site_init]: SEARCH auto_path set to . /tcl /dll /afs/apd.pok.ibm.com/u/lacey/tcl
/afs/apd.pok.ibm.com/u/lacey/dll /afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/tcl
/afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/dll /afs/watson/projects/vlsi/cte/tools/synzilla/1.0/tcl
/afs/watson/projects/vlsi/cte/tools/synzilla/1.0/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/tcl
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/dft
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_defaults.tcl
[CTE::site_init]: reading cte_defaults.tcl
[CTE::site_init]: done reading defaults.tcl
Loading: /afs/apd.pok.ibm.com/func/vlsi/alliance00/timing/parms/cp.tcl
Loading: /afs/apd.pok.ibm.com/func/vlsi/alliance00/timing/bsiu/batchz/batch/idcdsuc.tcl
[CTE::site_init]: ::CTE::site is gp390
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_setup_tech.tcl
[CTE::site_init]: Done
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/dll-rs6000/parmdb.dll
parmdb.dll version 0.0 (Mar 09 1999 20:01:28)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/idm/16/dll-rs6000/idm.dll
idm.dll version 16.0 (Mar 17 1999 03:19:04)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/srule.dll
srule.dll version 4.1 (Apr 14 1999 13:00:07)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/booledozer.dll
booledozer.dll version 4.1 (Apr 14 1999 17:19:37)
BooleDozer Build Version: 4.1.136
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/auto_setup.tcl
[auto_setup.tcl]: Loading std auto_setup...

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/auto_setup.tcl
 Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/wizard/3.1/tcl/wiz_setup.tcl
 [auto_setup.tcl]: Initializing cte specific auto_source and auto_load commands...
 [auto_setup.tcl]: CTE::run_dft not set to true - 'insscan' overridden with no op procedure
 [auto_setup.tcl]: Done
 Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/create_keywords.tcl
 [create_keywords.tcl]: Loading std create_keywords...
 Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/create_keywords.tcl
 [create_keywords.tcl]: Initializing cte specific create_keywords...
 [create_keywords.tcl]: Done
 Reading srule
 "/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/rules/all/tib/srule/tib.srule".
 Parsed 35 ruledefs, 0 powerdefs, 95 groups, 69 rulepins.
 bdz> bdz_post_srule
 Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/import_export.tcl
 [BLDEQN-12]: CMVC version 1.34 compiled on Apr 13 1999 at 18:02:41.
 [BD-450047]: CMVC version 1.17 compiled on Apr 13 1999 at 18:03:05.
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/icmcom.dll
 icmcom.dll version 3.1 (Mar 10 1999 09:48:07)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/icmvim.dll
 icmvim.dll version 3.1 (Mar 10 1999 09:48:09)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/dll/license.dll
 license.dll version 3.1 (Apr 07 1999 14:28:56)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/icmsrc.dll
 icmsrc.dll version 3.1 (Mar 24 1999 00:37:00)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/einsengine.dll
 einsengine.dll version 3.1 (Mar 24 1999 22:38:48)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/rice/4.0/.dll-rs_aix41/rice.dll
 rice.dll version 4.0 (Apr 07 1999 22:51:55)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvui.dll
 itvui.dll version 3.1 (Mar 24 1999 00:38:36)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvrc.dll
 itvrc.dll version 3.1 (Mar 10 1999 09:48:30)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvpd.dll
 itvpd.dll version 3.1 (Mar 25 1999 11:18:07)
 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/einstimer.dll
 einstimer.dll version 3.1 (Mar 24 1999 22:39:01)
 [ET-101]: Initializing EinsTimer...
 CMVC Release Level: 03.01
 Compiled: Wed Mar 24 22:00:23 1999
 [ET-102]: EinsTimer Version 3 Release 1
 Licensed Materials-Property of IBM
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 All rights reserved.

 US Government Users Restricted Rights -
 Use, duplication or disclosure restricted
 by GSA Schedule Contract with IBM Corp.

 "IBM" and "EinsTimer" are trademarks of
 "International Business Machines"
 [ET-110]: License obtained for EinsTimer 1.1

 Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvrep.dll
 itvrep.dll version 3.1 (Mar 24 1999 00:39:43)

```

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvpower.dll
itvpower.dll version 3.1 (Mar 24 1999 00:40:25)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvelec.dll
itvelec.dll version 3.1 (Mar 22 1999 23:52:50)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvete.dll
itvete.dll version 3.1 (Mar 22 1999 23:52:56)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll-rs6000/assertTimer.dll
assertTimer.dll version 1.0 (Apr 14 1999 13:00:13)
Timing Assertion Code
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll-rs6000/bdctime.dll
bdctime.dll version 4.1 (Apr 15 1999 13:15:19)
[BD-101]: License Obtained for ..... BooleDozer 4.x
[make_feedthru_boxes]: IOPADs, BRKPTs, etc. set to FEEDTHRU boxes.
Loading: /afs/apd.pok.ibm.com/u/lacey/l.bdz_variables
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/ctesynz_cp.tcl
> set_trace -debug_level -key tbmove
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvcdd.dll
itvcdd.dll version 3.1 (Mar 22 1999 23:53:02)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/dll/cte.dll
cte.dll version 1.0 (Apr 13 1999 13:39:58)
CTE BooleDozer under Nutshell compiled code
cte_ci_init
> CTE::tfuzz
Delays are given in units of 1.000000e-09 seconds
Fuzziness is 1.000000e-03 > load_logic_rule -tech blackbox -srule /afs/apd/func/vlsi...
Reading rule "/afs/apd/func/vlsi/alliance00/bd2/prod/srule/latches.srule".
[SRULE-17015]: line 24: Keyword "RACEFREE" not defined, adding as VARTYPE_STRING.
[SRULE-17015]: line 242: Keyword "SCAN_ONLY" not defined, adding as VARTYPE_STRING.
[SRULE-17015]: line 243: Keyword "NODEF" not defined, adding as VARTYPE_STRING.
Parsed 22 ruledefs, 0 powerdefs, 60 groups, 214 rulepins.
bdz> load_xrule -file {/afs/apd/func/vlsi/alliance00/bd2/prod/xrule/latches.xrule}
> load_xrule -file /afs/apd/func/vlsi/alliance00/bd2/prod/xrule/latches.xrule
[BD-450042]: Reading XRULE file '/afs/apd/func/vlsi/alliance00/bd2/prod/xrule/latches.xrule'
[BD-450041]: File '/afs/apd/func/vlsi/alliance00/bd2/prod/xrule/latches.xrule' is being read under VIEW
'XPANDVIEW'
bdz> bdz_post_srule
> bldeqn
[BLDEQN-29]: (W) note - \" no longer needed in srules (only this one warning)
> newgen
> check_logic_rule -technology BLACKBOX -drop_inputs
CMVC version 1.39 compiled on Apr 8 1999 at 05:49:53.
[SRULE-2]: (W) "latches.srule", line 318, Rule L_AO22:AO does not have power level children
[SRULE-2]: (W) "latches.srule", line 332, Rule L_AO222:AO does not have power level children
[SRULE-2]: (W) "latches.srule", line 351, Rule L_AO2222:AO does not have power level children
[SRULE-2]: (W) "latches.srule", line 276, Rule L_AOI22:AOI does not have power level children
[SRULE-2]: (W) "latches.srule", line 299, Rule L_AOI222:AOI does not have power level children
[SRULE-2]: (W) "latches.srule", line 268, Rule L_NAND:NAND does not have power level children
[SRULE-2]: (W) "latches.srule", line 290, Rule L_NAND3:NAND does not have power level children
[SRULE-2]: (W) "latches.srule", line 374, Rule L_NAND4:NAND does not have power level children
[SRULE-2]: (W) "latches.srule", line 261, Rule L_NOT:NOT does not have power level children
[SRULE-2]: (W) "latches.srule", line 23, Rule XDLATR:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 241, Rule XLATSO:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 388, Rule XDLATCORE:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 412, Rule XSCANCORE:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 209, Rule XLAT8R:SEQUENTIAL does not have power level children

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[SRULE-1]: (W) "latches.srule", line 23, Pin group M_OUT on XDLATR:REG has no pins in it
[SRULE-1]: (W) "latches.srule", line 388, Pin group M_OUT on XDLATCORE:REG has no pins in it
[SRULE-1025]: (E) "latches.srule", line 23, Pin group M_OUT on box XDLATR has zero pins
[SRULE-1025]: (E) "latches.srule", line 388, Pin group M_OUT on box XDLATCORE has zero pins
[CTE::setup_bsc8]: setting ctesrule
    > load_logic_rule -tech CC8S -srule /afs/apd/func/vlsi/all...
Reading srule "/afs/apd/func/vlsi/alliance00/bscc8/prod/srule/bscc8.srule.synz".
[SRULE-17015]: line 8: Keyword "BLOCK_TOP" not defined, adding as VARTYPE_STRING.
[SRULE-17015]: line 9: Keyword "GRP0" not defined, adding as VARTYPE_STRING.
[SRULE-17015]: line 3210: Keyword "ISCB" not defined, adding as VARTYPE_STRING.
Parsed 76 ruledefs, 1985 powerdefs, 206 groups, 361 rulepins.
bdz> bdz_post_srule
    > bldeqn
    > newgen
    > load_xrule -file /afs/apd/func/vlsi/alliance00/bscc8/pro...
[BD-450042]: Reading XRULE file '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule'
[BD-450041]: File '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule' is being read under VIEW
'XPANDVIEW'
    > check_logic_rule -technology CC8S -drop_inputs
CMVC version 1.39 compiled on Apr 8 1999 at 05:49:53.
[SRULE-2]: (W) "bscc8.srule.synz", line 8, Rule cs_kvdd:CONSTANT does not have power level children
[SRULE-2]: (W) "bscc8.srule.synz", line 12, Rule cs_kgnd:CONSTANT does not have power level
children
[SRULE-9]: (W) "bscc8.srule.synz", line 3191, One of the power levels of cl_scan:REG should be the
default
(first power level cl_scanonly will be used)
[SRULE-2]: (W) "bscc8.srule.synz", line 3232, Rule cb_clk_32_1:SEQUENTIAL does not have power
level children
    > load_cdc_rule -rule /afs/apd/func/vlsi/alliance00/bscc8/...
[ET-1757]: Initializing CDC...

[ET-1758]: Rule    = /afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface_RS6K

[ET-607]: Starting the dynamic link to CDC for rule:
    /afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface_RS6K
[DCL-512]: DCL Runtime Environment Version 3.1
    Last compiled on Apr 12 1999 at 10:00:33.
[DCL-642]: I am running in process ID 92476

[DCL-17001]: RLEV: DCMinterface rule, version v1.0.2 IEEE 1481-1998, technology GENERIC, was
compiled on 14:17:33 at Mar 12 1999

[DCL-19009]: CAP: Setting DEFAULT PINCAP value to: 0 as defined by environment variable
<DCM_DEFAULT_PINCAP>

[DCL-17001]: RLEV: Methods subrule, version v1.0.2 IEEE 1481-1998, was compiled on 14:17:39 at Mar
12 1999

[DCL-19021]: INFO: Maximum number of DCM messages to be printed has been set to 100000000

[DCL-17001]: RLEV: LimitPrint subrule, version v1.0 IEEE 1481-1998, was compiled on 14:17:44 at Mar
12 1999

[DCL-17001]: RLEV: printSummary subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:37 at
Mar 12 1999

```

[DCL-17001]: RLEV: Ceffective subrule, version v1.0 IEEE 1481-1998, was compiled on 14:17:50 at Mar 12 1999

[DCL-19000]: ENV: Environment variable <DCMCAPTHRESHOLD> NOT set by user.

[DCL-19017]: CAP: EffectiveC Cap Threshold not set.

[DCL-17001]: RLEV: techSpec subrule, version v1.0.3 IEEE 1481-1998, was compiled on 14:17:56 at Mar 12 1999

[DCL-17001]: RLEV: WireLoad subrule, version v1.0.1 IEEE 1481-1998, was compiled on 14:18:04 at Mar 12 1999

[DCL-17001]: RLEV: WireLoad table, Version 1.0.1 IEEE 1481-1998 Technology SA27 , was compiled on 14:18:04 at Mar 12 1999

[DCL-17040]: The available wireload model levels are: 5lm, 6lm

[DCL-17002]: Enviromental variable DCMWireLoadLevels not set using default.

[DCL-17001]: RLEV: NetDelay subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:12 at Mar 12 1999

[DCL-17001]: RLEV: cellName subrule, version v1.5 IEEE 1481-1998, was compiled on 14:18:17 at Mar 12 1999

[DCL-17001]: RLEV: CellName parser subrule, version v1.0.5 IEEE 1481-1998, was compiled on 14:18:30 at Mar 12 1999

[DCL-17001]: RLEV: Defaults subrule, version v1.0.4 IEEE 1481-1998, was compiled on 14:18:40 at Mar 12 1999

[DCL-17012]: Using the default supplied bomFile

[DCL-17001]: RLEV: _cc8s_rules_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 09:32:54 at Apr 12 1999

[DCL-17001]: RLEV: _cc8s_latches_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 12:12:01 at Apr 6 1999

[DCL-17001]: RLEV: railCache subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:52 at Mar 12 1999

[DCL-17020]: Enviromental variable DCMDoRangeCheck set to do no reporting.

[ET-655]: IEEE standard interface version "IEEE 1481-1998" for technology "GENERIC". Library identification: "IBM_GENERIC".

[ET-652]: (W) Could not find IEEE standard routine dpcmGetDelayGradient in rules. Substituting dummy routine.

[ET-652]: (W) Could not find IEEE standard routine dpcmGetSlewGradient in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGetAETCellPowerWithSensitivity in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGroupGetSettlingTime in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGroupGetSimultaneousSwitchTime in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmCalcPartialSwingEnergy in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmSetInitialState in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmFillPinCache in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmFreePinCache in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGetNetEnergy in rules. Substituting dummy routine.

[ET-611]: Dynamic link to CDC rule complete.

```
> read_timer_parms -file /afs/apd/func/vlsi/alliance00/bsc...
```

[ICM-15]: >Begin...Parm Reader

```
for file /afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/EINSdefaults.
```

[ICM-16]: <End.....Parm Reader.

```
> source hide.tcl
```

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/hide.tcl

```
> hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
> hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao...
> hide -no_clear -cells { cs_buffe }
> hide -no_clear -cells { cs_invvn cs_invvv }
> hide -no_clear -cells { cs_nnd2f cs_nnd2g cs_nnd2n cs_nn...
> hide -no_clear -cells { cs_nnd3f cs_nnd3g cs_nnd3h cs_nn...
> hide -no_clear -cells { cs_nnd4n cs_nnd4v }
> hide -no_clear -cells { cs_nor2f cs_nor2g cs_nor2n cs_no...
> hide -no_clear -cells { cs_nor3f cs_nor3g cs_nor3h cs_no...
> hide -no_clear -cells { cs_oa12f cs_oa12g cs_oa12n cs_oa...
> hide -no_clear -cells { cs_oa21n cs_oa21v }
> hide -no_clear -cells { cs_oa22n cs_oa22v }
> hide -no_clear -cells { cs_xbn2n cs_xbn2v }
> hide -no_clear -cells { cs_xbo2n cs_xbo2v }
> find cell cs_*
> hide -no_clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f0...
> find cell cs_buffe*
> hide -no_clear -cells {cs_buffe01a cs_buffe02a cs_buffe0...
> hide -clear -cells { "cs_invvn" }
> find cell cs_invvn*
> hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...
> hide -clear -cells { "cs_nnd2n" }
> find cell cs_nnd2n*
> hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...
> hide -clear -cells { "cs_nnd3n" }
```

```

> find cell cs_nnd3n*
> hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
> hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*
> hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
> hide -clear -cells { "cs_nor2n" }
> find cell cs_nor2n*
> hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
> hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*
> hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*
> hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*
> hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*
> hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*
> hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*
> hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*
> hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
> hide -clear -cells { "cs_buffe" }
> find cell cs_buffe*
> hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*
> hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*
> hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
> read_vim -def IDCDSUC -view HISVHDL -lib /afs/apd/func/v...
Reading proto IDCDSUC...
Reading proto DLAT_SCAN#1#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#1#B_0#1.LATCH...
bdz> vim_postimport __CiType_16_30aada78
> nextnet xpndbundles
> padnet
> brkloops
> nextbox xpndarr
> is_parm a_penny_saved_is_a_penny_earned
> nextnet_with_test test_worth(FALSE),delname(SAVE)
> nextbox xpndconcat
> nextbox_with_test test_key(SYN_CONCAT),onein
> nextbox xpndiopad
> nextbox_with_test {test_def(BRKPT), xpndprim}
> nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded

```

```

    > sweep 1
    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30aad4e0
    > nextnet xpndbundles
    > padnet
    > brkloops
    > nextbox xpndarr
    > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
    > nextbox xpndconcat
    > nextbox_with_test test_key(SYN_CONCAT),onein
    > nextbox xpndiopad
    > nextbox_with_test {test_def(BRKPT), xpndprim}
    > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
    > sweep 1
    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
Reading proto IDCDSUC_MAC.LATCH.CONCSTMS...
bdz> vim_postimport __CiType_16_31471e98
    > nextnet xpndbundles
    > padnet
    > brkloops
    > nextbox xpndarr
    > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
    > nextbox xpndconcat
    > nextbox_with_test test_key(SYN_CONCAT),onein
    > nextbox xpndiopad
    > nextbox_with_test {test_def(BRKPT), xpndprim}
    > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
    > sweep 1
    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
Reading proto DLAT_SCAN#2#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#2#B_00#1.LATCH...
bdz> vim_postimport __CiType_16_3148a228
    > nextnet xpndbundles

```



```

> padnet
> brkloops
> nextbox xpndarr
> is_parm a_penny_saved_is_a_penny_earned
  > nextnet_with_test test_worth(FALSE),delname(SAVE)
> nextbox xpndconcat
> nextbox_with_test test_key(SYN_CONCAT),onein
> nextbox xpndiopad
> nextbox_with_test {test_def(BRKPT), xpndprim}
> nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
  > sweep 1
  > his_attributes
  > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
  > sweep 1
  > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
  > nextnet ms2dot(BUS)
  > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30a55270
  > nextnet xpndbundles
  > padnet
  > brkloops
  > nextbox xpndarr
  > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
  > nextbox xpndconcat
  > nextbox_with_test test_key(SYN_CONCAT),onein
  > nextbox xpndiopad
  > nextbox_with_test {test_def(BRKPT), xpndprim}
  > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
  > sweep 1
  > his_attributes
  > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
  > sweep 1
  > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
  > nextnet ms2dot(BUS)
  > trim_idm_mem CURRENT
Reading proto DLAT_SCAN#12#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#12#B_00UUUUUUUUUU#1.LATCH...
bdz> vim_postimport __CiType_16_30a6aea0
  > nextnet xpndbundles
  > padnet
  > brkloops
  > nextbox xpndarr
  > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
  > nextbox xpndconcat
  > nextbox_with_test test_key(SYN_CONCAT),onein
  > nextbox xpndiopad
  > nextbox_with_test {test_def(BRKPT), xpndprim}
  > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded

```

```

    > sweep 1
    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_3148b770
    > nextnet xpndbundles
    > padnet
    > brkloops
    > nextbox xpndarr
    > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
    > nextbox xpndconcat
    > nextbox_with_test test_key(SYN_CONCAT),onein
    > nextbox xpndiopad
    > nextbox_with_test {test_def(BRKPT), xpndprim}
    > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
    > sweep 1
    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
Reading proto DLAT_SCAN#3#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#3#B_00U#1.LATCH...
bdz> vim_postimport __CiType_16_30a6f328
    > nextnet xpndbundles
    > padnet
    > brkloops
    > nextbox xpndarr
    > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
    > nextbox xpndconcat
    > nextbox_with_test test_key(SYN_CONCAT),onein
    > nextbox xpndiopad
    > nextbox_with_test {test_def(BRKPT), xpndprim}
    > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
    > sweep 1
    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30a6ada0
    > nextnet xpndbundles
    > padnet

```

```

> brkloops
> nextbox xpndarr
> is_parm a_penny_saved_is_a_penny_earned
  > nextnet_with_test test_worth(FALSE),delname(SAVE)
> nextbox xpndconcat
> nextbox_with_test test_key(SYN_CONCAT),onein
> nextbox xpndiopad
> nextbox_with_test {test_def(BRKPT), xpndprim}
> nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
> sweep 1
> his_attributes
> nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
> sweep 1
> nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
> nextnet ms2dot(BUS)
> trim_idm_mem CURRENT
Reading proto DLAT_SCAN#4#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#4#B_00UU#1.LATCH...
bdz> vim_postimport __CiType_16_30a71048
  > nextnet xpndbundles
  > padnet
  > brkloops
  > nextbox xpndarr
  > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
  > nextbox xpndconcat
  > nextbox_with_test test_key(SYN_CONCAT),onein
  > nextbox xpndiopad
  > nextbox_with_test {test_def(BRKPT), xpndprim}
  > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
  > sweep 1
  > his_attributes
  > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
> sweep 1
> nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
> nextnet ms2dot(BUS)
> trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30a6e6e0
  > nextnet xpndbundles
  > padnet
  > brkloops
  > nextbox xpndarr
  > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
  > nextbox xpndconcat
  > nextbox_with_test test_key(SYN_CONCAT),onein
  > nextbox xpndiopad
  > nextbox_with_test {test_def(BRKPT), xpndprim}
  > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
  > sweep 1

```

```

    > his_attributes
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30a445c8
    > nextnet xpndbundles
    > padnet
    > brkloops
    > nextbox xpndarr
    > is_parm a_penny_saved_is_a_penny_earned
    > nextnet_with_test test_worth(FALSE),delname(SAVE)
    > nextbox xpndconcat
    > nextbox_with_test test_key(SYN_CONCAT),onein
    > nextbox xpndiopad
    > nextbox_with_test {test_def(BRKPT), xpndprim}
    > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
    > sweep 1
    > his_attributes
[BD-350205]: (W) No config rule exists for attribute 'PIN_FUNCTION' on IDM_PROTO_PIN_TYPE
'clk_mode7->clk_mode7', defaulting to string.
    > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
    > sweep 1
    > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
    > nextnet ms2dot(BUS)
    > trim_idm_mem CURRENT
[ctesynz_cp.tcl]: model loaded aokay...flattening...
    > expand -hierarchy
bdz> post_expand
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/post_expand.tcl
    > sweep
    > delbrkpt BREAKLOOPS
    > brkloops
    > nextnet {delkey( EDIFNAME )}
    > nextbox {delkey( EDIFNAME )}
        > set_nochange
        > rtorbox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
        > sweep
        > ltorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
        > sweep
    > nochange
        > set_nochange
        > rtorbox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
        > sweep
        > ltorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
        > sweep
    > nochange
    > nextbox_with_test test_key(IOPAD_LOCATION,2),resolve_net...
    > nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
    > sweep
    > nextbox merge_dots()

```

```

> nextbox dot2ms()
> nextnet {ms2dot( BUS )}
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/hisprep.tcl
> proto_get_int HIS_BD_VIM_SYNC,0
> proto_get_int HISPREPSCN,0
> createkw HISPREPSCN,VARTYPE_INTEGER,CLAS_PROTO_BOX
> proto_set_key HISPREPSCN,1
> nextnet_with_test test_worth(FALSE,NO_QUALIFIER),delname...
> synsasname PROTECT
> syn_hide_from_keywords
[SRULE-17200]: 0 LOGIC_STYLE keywords set on usage boxes from proto box keyword
[SRULE-17205]: 0 LOGIC_STYLE keywords were found on usage boxes
[SRULE-17210]: 0 SYN_USAGE_BOX_HIDE keywords set on usage boxes
> nextbox exprnway,exprnot,exprorsel
> nextbox_with_test test_syn_hide(!HIDE_MAP,!HIDE_DOMINANT...
> nextbox expropt1(SSS,SSG,GSG,SGG),exprxpnd
> expr_reset
> nextbox_with_test test_key(LOGIC_STYLE,DATA_FLOW),syn_hi...
> nextbox bindvhdltibs
> nextbox_with_test test_clkcomp,eq2and,onein
> nextbox_with_test test_key(ADDER_EXPANSION),comp2sub
> nextbox xpndadd(USE_TIB)
> nextbox xpndabs
> nextbox xpndregs
> nextbox makesrl
> nextbox impregs
> is_parm new_assert
> nextbox xpndcmpnt,xpndprim
[ET-203]: Timing top level created for design: IDCDSUC, analysis mode: default.

```

```

> cleanup 1
> delbrkpt BREAKLOOP
> brkloops ERROR
> keyword_is_defined {BEC_HISPREP, CLAS_PROTO_BOX}
[BD-354300]: Keyword BEC_HISPREP for object_class CLAS_PROTO_BOX has <NOT> been defined
> echo {<<< hisprep.scn called from synthesis, running cle...
<<< hisprep.scn called from synthesis, running cleanse >>>
> cleanse
> nextbox eq2and
> constant_selector
> elimdc ZERO
> cleanup 1
> keyword_is_defined {BEC_HISPREP, CLAS_PROTO_BOX}
[BD-354300]: Keyword BEC_HISPREP for object_class CLAS_PROTO_BOX has <NOT> been defined
> echo {<<< hisprep.scn called from synthesis, running cle...
<<< hisprep.scn called from synthesis, running cleanse >>>
> cleanse
> move_component_times
> copyinfo
> ltorbox deldang()
> checksrc
[BD-40101]: (W) Disconnected input port clkl_mode7.
[BD-40101]: (W) Disconnected input port clk2.
[BD-40129]: Network IDCDSUC had no old problems.
[BD-40130]: (W) Network IDCDSUC has 2 potential problem(s).

```

```

> source cte_clock_block_processing.tcl
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_clock_block_processing.tcl
> summary_report
[measure]: Compiled on Mar 12 1999 at 05:03:29.

```

The model <IDCDSUC> has:

```

Primary Inputs      =      122
Primary Outputs     =      73
Primary BIDs        =       0
Signals             =     1187
Gate Count          =      863
Connections         =     2051
Master REG Bits     =      83
Slave REG Bits      =      83
Internal Area       =     4790
External Area       =       0
Gates/Connects     =     0.420770
Fanout Count        =     2051
Average Fanout      =     1.727885
Avg Tech Box Size   =     5.550406
Tech Box Size Stddev =     0.023559
Power               =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals        =      814
Real boxes          =      488
Real connections    =     1676
Real LSTs           =     2490
Real ICells/box     =     9.815574
Real LSTs/box       =     5.102459
Real nets/box       =     1.668033

```

```

Cell      Total
Each      Cell

```

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
164		AND	>	AND	0 0	0.000	0	0	0.000		
180		BRKPT	>	BRKPT	0 0	0.000	0	0	0.000		
195		IOPAD	>	IOPAD	0 0	0.000	0	0	0.000		
62		NAND	>	NAND	0 0	0.000	0	0	0.000		
23		NOR	>	NOR	0 0	0.000	0	0	0.000		
91		OR	>	OR	0 0	0.000	0	0	0.000		
83		XDLATCORE	>	REG	0 0	0.000	0	0	0.000		
1		cb_mode_block	A	> SEQUENTIAL	70 0	0.000	70	0	0.000		
59		XRFCBA	A	> SEQUENTIAL	80 0	0.000	4720	0	0.000		
5		XOR	>	XOR	0 0	0.000	0	0	0.000		

[End of measure]

[measure]: Execution time was 0.0 seconds.

[cte_clock_block_processing.tcl]: cb_mode_block

> CTE::mode_block DEF(cb_mode_block)

[mode_block]: Rel 1.0 Compiled on Jan 7 1999 at 18:31:02.

> source cte_fixmodeblock.tcl

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_fixmodeblock.tcl

> unpadnet

```

> idm::filter -on gates -expr {[regex XRFCBA @def_name ]}
> idm::object_name __CiType_18_305b89c8
> led::connect_net -net clk_mode7 -pin slow_mode.clockblo...
> idm::object_name __CiType_18_305b8c38
> led::connect_net -net clk_mode7 -pin ru_rq_blk.clockblo...
> idm::object_name __CiType_18_305b8ea8
> led::connect_net -net clk_mode7 -pin iu_rst_fst.clockbl...
> idm::object_name __CiType_18_305d17d8
> led::connect_net -net clk_mode7 -pin iu_restart.clockbl...
> idm::object_name __CiType_18_305d1a48
> led::connect_net -net clk_mode7 -pin ia_to_if.clockbloc...
> idm::object_name __CiType_18_305d1cb8
> led::connect_net -net clk_mode7 -pin frc_mmode.clockblo...
> idm::object_name __CiType_18_305d1f28
> led::connect_net -net clk_mode7 -pin local_milli.clockb...
> idm::object_name __CiType_18_305d2198
> led::connect_net -net clk_mode7 -pin ia_to_if_t1.clockb...
> idm::object_name __CiType_18_305d2408
> led::connect_net -net clk_mode7 -pin mia_to_if.clockblo...
> idm::object_name __CiType_18_305d2678
> led::connect_net -net clk_mode7 -pin slow_mode_t1.clock...
> idm::object_name __CiType_18_305d28e8
> led::connect_net -net clk_mode7 -pin iq_empty_dly.clock...
> idm::object_name __CiType_18_305d2b58
> led::connect_net -net clk_mode7 -pin slow_mode_t2.clock...
> idm::object_name __CiType_18_305d2dc8
> led::connect_net -net clk_mode7 -pin s390_updt_blk.cloc...
> idm::object_name __CiType_18_305d3038
> led::connect_net -net clk_mode7 -pin srlz_nomatch.clock...
> idm::object_name __CiType_18_305d32a8
> led::connect_net -net clk_mode7 -pin bce_hold_aa.clockb...
> idm::object_name __CiType_18_305d3518
> led::connect_net -net clk_mode7 -pin srlz_actn.clockblo...
> idm::object_name __CiType_18_305d3878
> led::connect_net -net clk_mode7 -pin op_44_dcd.clockblo...
> idm::object_name __CiType_18_305d3ae8
> led::connect_net -net clk_mode7 -pin op_cmp_tr.clockblo...
> idm::object_name __CiType_18_305d3d58
> led::connect_net -net clk_mode7 -pin num_dcd.clockblock...
> idm::object_name __CiType_18_305d40b8
> led::connect_net -net clk_mode7 -pin mia_to_if_t1.clock...
> idm::object_name __CiType_18_305d4328
> led::connect_net -net clk_mode7 -pin eu_op_encode.clock...
> idm::object_name __CiType_18_305d4fe8
> led::connect_net -net clk_mode7 -pin frc_blk_1cyc.clock...
> idm::object_name __CiType_18_305d5258
> led::connect_net -net clk_mode7 -pin local_milli_t1.clo...
> idm::object_name __CiType_18_305d54c8
> led::connect_net -net clk_mode7 -pin local_milli_t2.clo...
> idm::object_name __CiType_18_305d5738
> led::connect_net -net clk_mode7 -pin bht_block.clockblo...
> idm::object_name __CiType_18_305d59a8
> led::connect_net -net clk_mode7 -pin srlz_blk.clockbloc...
> idm::object_name __CiType_18_305d5c18
> led::connect_net -net clk_mode7 -pin exc_cond.clockbloc...

```

```

> idm::object_name __CiType_18_305d5e88
> led::connect_net -net clk_mode7 -pin slow_mode_dly.cloc...
> idm::object_name __CiType_18_305d60f8
> led::connect_net -net clk_mode7 -pin dcd_succ_disable_s...
> idm::object_name __CiType_18_305d6548
> led::connect_net -net clk_mode7 -pin drain_blk.clockblo...
> idm::object_name __CiType_18_305d67b8
> led::connect_net -net clk_mode7 -pin dcd_ilc.clockblock...
> idm::object_name __CiType_18_305d6b18
> led::connect_net -net clk_mode7 -pin slow_mode_blk.cloc...
> idm::object_name __CiType_18_305d6d88
> led::connect_net -net clk_mode7 -pin op_cmp_44.clockblo...
> idm::object_name __CiType_18_305d6ff8
> led::connect_net -net clk_mode7 -pin op_cmp_dsbl.clockb...
> idm::object_name __CiType_18_305d7268
> led::connect_net -net clk_mode7 -pin eu_frc_milli.clock...
> idm::object_name __CiType_18_305d74d8
> led::connect_net -net clk_mode7 -pin bcr_store_stat.clo...
> idm::object_name __CiType_18_305d7748
> led::connect_net -net clk_mode7 -pin exc_info.clockbloc...
> idm::object_name __CiType_18_305d7c88
> led::connect_net -net clk_mode7 -pin spare.clockblock/c...
> idm::object_name __CiType_18_305d7ef8
> led::connect_net -net clk_mode7 -pin mcset_e1.clockbloc...
> idm::object_name __CiType_18_305d8168
> led::connect_net -net clk_mode7 -pin eu_iu_spare.clockb...
> idm::object_name __CiType_18_305d83d8
> led::connect_net -net clk_mode7 -pin dsbl_ovrlp_blk.clo...
> idm::object_name __CiType_18_305d8648
> led::connect_net -net clk_mode7 -pin inst_fetch.clockbl...
> idm::object_name __CiType_18_305d88b8
> led::connect_net -net clk_mode7 -pin iu_dsbl_ovrlp.cloc...
> idm::object_name __CiType_18_305d8b28
> led::connect_net -net clk_mode7 -pin ex_in_prog.clockbl...
> idm::object_name __CiType_18_305d8d98
> led::connect_net -net clk_mode7 -pin blk_dcd.clockblock...
> idm::object_name __CiType_18_305d92d8
> led::connect_net -net clk_mode7 -pin dcd_succ_dly.clock...
> idm::object_name __CiType_18_305d9548
> led::connect_net -net clk_mode7 -pin exec_recov.clockbl...
> idm::object_name __CiType_18_305d97b8
> led::connect_net -net clk_mode7 -pin ru_updt_dly.clockb...
> idm::object_name __CiType_18_305d9a28
> led::connect_net -net clk_mode7 -pin iu_rstfst_t1.cloc...
> idm::object_name __CiType_18_305d9c98
> led::connect_net -net clk_mode7 -pin inst_store.clockbl...
> idm::object_name __CiType_18_305d9f08
> led::connect_net -net clk_mode7 -pin eu_dsbl_aftr.clock...
> idm::object_name __CiType_18_305da178
> led::connect_net -net clk_mode7 -pin dcdsuc_err.clockbl...
> idm::object_name __CiType_18_305da3e8
> led::connect_net -net clk_mode7 -pin dcd_cyl_cnt.clockb...
> idm::object_name __CiType_18_305da748
> led::connect_net -net clk_mode7 -pin blk_mccend.clockblo...
> idm::object_name __CiType_18_305da9b8

```



```

> led::connect_net -net clkl_mode7 -pin op_44_info.clockbl...
> idm::object_name __CiType_18_305dad18
> led::connect_net -net clkl_mode7 -pin rcvry_reset.clockb...
> idm::object_name __CiType_18_305daf88
> led::connect_net -net clkl_mode7 -pin br_wrongs.clockblo...
> idm::object_name __CiType_18_305db1f8
> led::connect_net -net clkl_mode7 -pin rstrt_reset.clockb...
> idm::object_name __CiType_18_305db468
> led::connect_net -net clkl_mode7 -pin br_dcd_pend.clockb...
> idm::filter -on gates -expr {[regexp cb_mode_block @def...
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/new_led.tcl
> idm::locate_or_create_keyword_def -clas group -name PGRO...
> idm::locate_or_create_keyword_def -clas group -name PGRO...
> idm::locate_or_create_keyword_def -clas group -name PGRO...
> idm::locate_or_create_keyword_def -clas group -name COMM...
> idm::get_active_network
> idm::locate_net -proto_box __CiType_16_30a445c8 -name cl...
> led::create_net -name clkl_mode4_0
> idm::object_name __CiType_18_305b1a98
> led::connect_net -net clkl_mode4_0 -pin gpтр_latch/clkl_...
> idm::object_name __CiType_18_305b89c8
> led::connect_net -net clkl_mode4_0 -pin slow_mode.clockb...
> idm::object_name __CiType_18_305b8c38
> led::connect_net -net clkl_mode4_0 -pin ru_rq_blk.clockb...
> idm::object_name __CiType_18_305b8ea8
> led::connect_net -net clkl_mode4_0 -pin iu_rstfst.clock...
> idm::object_name __CiType_18_305d17d8
> led::connect_net -net clkl_mode4_0 -pin iu_restart.clock...
> idm::object_name __CiType_18_305d1a48
> led::connect_net -net clkl_mode4_0 -pin ia_to_if.clockbl...
> idm::object_name __CiType_18_305d1cb8
> led::connect_net -net clkl_mode4_0 -pin frc_mmode.clockb...
> idm::object_name __CiType_18_305d1f28
> led::connect_net -net clkl_mode4_0 -pin local_milli.cloc...
> idm::object_name __CiType_18_305d2198
> led::connect_net -net clkl_mode4_0 -pin ia_to_if_t1.cloc...
> idm::object_name __CiType_18_305d2408
> led::connect_net -net clkl_mode4_0 -pin mia_to_if.clockb...
> idm::object_name __CiType_18_305d2678
> led::connect_net -net clkl_mode4_0 -pin slow_mode_t1.clo...
> idm::object_name __CiType_18_305d28e8
> led::connect_net -net clkl_mode4_0 -pin iq_empty_dly.clo...
> idm::object_name __CiType_18_305d2b58
> led::connect_net -net clkl_mode4_0 -pin slow_mode_t2.clo...
> idm::object_name __CiType_18_305d2dc8
> led::connect_net -net clkl_mode4_0 -pin s390_updt_blk.cl...
> idm::object_name __CiType_18_305d3038
> led::connect_net -net clkl_mode4_0 -pin srlz_nomatch.clo...
> idm::object_name __CiType_18_305d32a8
> led::connect_net -net clkl_mode4_0 -pin bce_hold_aa.cloc...
> idm::object_name __CiType_18_305d3518
> led::connect_net -net clkl_mode4_0 -pin srlz_actn.clockb...
> idm::object_name __CiType_18_305d3878
> led::connect_net -net clkl_mode4_0 -pin op_44_dcd.clockb...
> idm::object_name __CiType_18_305d3ae8

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> led::connect_net -net clk_mode4_0 -pin op_cmp_tr.clockb...
> idm::object_name __CiType_18_305d3d58
> led::connect_net -net clk_mode4_0 -pin num_dcd.clockblo...
> idm::object_name __CiType_18_305d40b8
> led::connect_net -net clk_mode4_0 -pin mia_to_if_t1.clo...
> idm::object_name __CiType_18_305d4328
> led::connect_net -net clk_mode4_0 -pin eu_op_encode.clo...
> idm::object_name __CiType_18_305d4fe8
> led::connect_net -net clk_mode4_0 -pin frc_blk_1cyc.clo...
> idm::object_name __CiType_18_305d5258
> led::connect_net -net clk_mode4_0 -pin local_milli_t1.c...
> idm::object_name __CiType_18_305d54c8
> led::connect_net -net clk_mode4_0 -pin local_milli_t2.c...
> idm::object_name __CiType_18_305d5738
> led::connect_net -net clk_mode4_0 -pin bht_block.clockb...
> idm::object_name __CiType_18_305d59a8
> led::connect_net -net clk_mode4_0 -pin srlz_blk.clockbl...
> idm::object_name __CiType_18_305d5c18
> led::connect_net -net clk_mode4_0 -pin exc_cond.clockbl...
> idm::object_name __CiType_18_305d5e88
> led::connect_net -net clk_mode4_0 -pin slow_mode_dly.cl...
> idm::object_name __CiType_18_305d60f8
> led::connect_net -net clk_mode4_0 -pin dcd_succ_disable...
> idm::object_name __CiType_18_305d6548
> led::connect_net -net clk_mode4_0 -pin drain_blk.clockb...
> idm::object_name __CiType_18_305d67b8
> led::connect_net -net clk_mode4_0 -pin dcd_ilc.clockblo...
> idm::object_name __CiType_18_305d6b18
> led::connect_net -net clk_mode4_0 -pin slow_mode_blk.cl...
> idm::object_name __CiType_18_305d6d88
> led::connect_net -net clk_mode4_0 -pin op_cmp_44.clockb...
> idm::object_name __CiType_18_305d6ff8
> led::connect_net -net clk_mode4_0 -pin op_cmp_dsbl.cloc...
> idm::object_name __CiType_18_305d7268
> led::connect_net -net clk_mode4_0 -pin eu_frc_milli.clo...
> idm::object_name __CiType_18_305d74d8
> led::connect_net -net clk_mode4_0 -pin bcr_store_stat.c...
> idm::object_name __CiType_18_305d7748
> led::connect_net -net clk_mode4_0 -pin exc_info.clockbl...
> idm::object_name __CiType_18_305d7c88
> led::connect_net -net clk_mode4_0 -pin spare.clockblock...
> idm::object_name __CiType_18_305d7ef8
> led::connect_net -net clk_mode4_0 -pin mcset_e1.clockbl...
> idm::object_name __CiType_18_305d8168
> led::connect_net -net clk_mode4_0 -pin eu_iu_spare.cloc...
> idm::object_name __CiType_18_305d83d8
> led::connect_net -net clk_mode4_0 -pin dsbl_ovrlp_blk.c...
> idm::object_name __CiType_18_305d8648
> led::connect_net -net clk_mode4_0 -pin inst_fetch.clock...
> idm::object_name __CiType_18_305d88b8
> led::connect_net -net clk_mode4_0 -pin iu_dsbl_ovrlp.cl...
> idm::object_name __CiType_18_305d8b28
> led::connect_net -net clk_mode4_0 -pin ex_in_prog.clock...
> idm::object_name __CiType_18_305d8d98
> led::connect_net -net clk_mode4_0 -pin blk_dcd.clockblo...

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> idm::object_name __CiType_18_305d92d8
> led::connect_net -net clk_mode4_0 -pin dcd_succ_dly.clo...
> idm::object_name __CiType_18_305d9548
> led::connect_net -net clk_mode4_0 -pin exec_recov.clock...
> idm::object_name __CiType_18_305d97b8
> led::connect_net -net clk_mode4_0 -pin ru_updt_dly.cloc...
> idm::object_name __CiType_18_305d9a28
> led::connect_net -net clk_mode4_0 -pin iu_rstfst_t1.cl...
> idm::object_name __CiType_18_305d9c98
> led::connect_net -net clk_mode4_0 -pin inst_store.clock...
> idm::object_name __CiType_18_305d9f08
> led::connect_net -net clk_mode4_0 -pin eu_dsbl_aftr.clo...
> idm::object_name __CiType_18_305da178
> led::connect_net -net clk_mode4_0 -pin dcdsuc_err.clock...
> idm::object_name __CiType_18_305da3e8
> led::connect_net -net clk_mode4_0 -pin dcd_cyl_cnt.cloc...
> idm::object_name __CiType_18_305da748
> led::connect_net -net clk_mode4_0 -pin blk_mccend.clockb...
> idm::object_name __CiType_18_305da9b8
> led::connect_net -net clk_mode4_0 -pin op_44_info.clock...
> idm::object_name __CiType_18_305dad18
> led::connect_net -net clk_mode4_0 -pin rcvry_reset.cloc...
> idm::object_name __CiType_18_305daf88
> led::connect_net -net clk_mode4_0 -pin br_wrongs.clockb...
> idm::object_name __CiType_18_305db1f8
> led::connect_net -net clk_mode4_0 -pin rst_rst_reset.cloc...
> idm::object_name __CiType_18_305db468
> led::connect_net -net clk_mode4_0 -pin br_dcd_pend.cloc...
> idm::get_active_network
> idm::locate_net -proto_box __CiType_16_30a445c8 -name cl...
> led::create_net -name clk_mode5_0
> idm::object_name __CiType_18_305b1a98
> led::connect_net -net clk_mode5_0 -pin gp_rst_latch/clk...
> idm::object_name __CiType_18_305b89c8
> led::connect_net -net clk_mode5_0 -pin slow_mode.clockb...
> idm::object_name __CiType_18_305b8c38
> led::connect_net -net clk_mode5_0 -pin ru_rq_blk.clockb...
> idm::object_name __CiType_18_305b8ea8
> led::connect_net -net clk_mode5_0 -pin iu_rstfst.clock...
> idm::object_name __CiType_18_305d17d8
> led::connect_net -net clk_mode5_0 -pin iu_restart.clock...
> idm::object_name __CiType_18_305d1a48
> led::connect_net -net clk_mode5_0 -pin ia_to_if.clockbl...
> idm::object_name __CiType_18_305d1cb8
> led::connect_net -net clk_mode5_0 -pin frc_mmode.clockb...
> idm::object_name __CiType_18_305d1f28
> led::connect_net -net clk_mode5_0 -pin local_milli.cloc...
> idm::object_name __CiType_18_305d2198
> led::connect_net -net clk_mode5_0 -pin ia_to_if_t1.cloc...
> idm::object_name __CiType_18_305d2408
> led::connect_net -net clk_mode5_0 -pin mia_to_if.clockb...
> idm::object_name __CiType_18_305d2678
> led::connect_net -net clk_mode5_0 -pin slow_mode_t1.clo...
> idm::object_name __CiType_18_305d28e8
> led::connect_net -net clk_mode5_0 -pin iq_empty_dly.clo...

```

```
> idm::object_name __CiType_18_305d2b58
> led::connect_net -net clk_mode5_0 -pin slow_mode_t2.clo...
> idm::object_name __CiType_18_305d2dc8
> led::connect_net -net clk_mode5_0 -pin s390_updt_blk.cl...
> idm::object_name __CiType_18_305d3038
> led::connect_net -net clk_mode5_0 -pin srlz_nomatch.clo...
> idm::object_name __CiType_18_305d32a8
> led::connect_net -net clk_mode5_0 -pin bce_hold_aa.cloc...
> idm::object_name __CiType_18_305d3518
> led::connect_net -net clk_mode5_0 -pin srlz_actn.clockb...
> idm::object_name __CiType_18_305d3878
> led::connect_net -net clk_mode5_0 -pin op_44_dcd.clockb...
> idm::object_name __CiType_18_305d3ae8
> led::connect_net -net clk_mode5_0 -pin op_cmp_tr.clockb...
> idm::object_name __CiType_18_305d3d58
> led::connect_net -net clk_mode5_0 -pin num_dcd.clockblo...
> idm::object_name __CiType_18_305d40b8
> led::connect_net -net clk_mode5_0 -pin mia_to_if_t1.clo...
> idm::object_name __CiType_18_305d4328
> led::connect_net -net clk_mode5_0 -pin eu_op_encode.clo...
> idm::object_name __CiType_18_305d4fe8
> led::connect_net -net clk_mode5_0 -pin frc_blk_1cyc.clo...
> idm::object_name __CiType_18_305d5258
> led::connect_net -net clk_mode5_0 -pin local_milli_t1.c...
> idm::object_name __CiType_18_305d54c8
> led::connect_net -net clk_mode5_0 -pin local_milli_t2.c...
> idm::object_name __CiType_18_305d5738
> led::connect_net -net clk_mode5_0 -pin bht_block.clockb...
> idm::object_name __CiType_18_305d59a8
> led::connect_net -net clk_mode5_0 -pin srlz_blk.clockbl...
> idm::object_name __CiType_18_305d5c18
> led::connect_net -net clk_mode5_0 -pin exc_cond.clockbl...
> idm::object_name __CiType_18_305d5e88
> led::connect_net -net clk_mode5_0 -pin slow_mode_dly.cl...
> idm::object_name __CiType_18_305d60f8
> led::connect_net -net clk_mode5_0 -pin dcd_succ_disable...
> idm::object_name __CiType_18_305d6548
> led::connect_net -net clk_mode5_0 -pin drain_blk.clockb...
> idm::object_name __CiType_18_305d67b8
> led::connect_net -net clk_mode5_0 -pin dcd_ilc.clockblo...
> idm::object_name __CiType_18_305d6b18
> led::connect_net -net clk_mode5_0 -pin slow_mode_blk.cl...
> idm::object_name __CiType_18_305d6d88
> led::connect_net -net clk_mode5_0 -pin op_cmp_44.clockb...
> idm::object_name __CiType_18_305d6ff8
> led::connect_net -net clk_mode5_0 -pin op_cmp_dsbl.cloc...
> idm::object_name __CiType_18_305d7268
> led::connect_net -net clk_mode5_0 -pin eu_frc_milli.clo...
> idm::object_name __CiType_18_305d74d8
> led::connect_net -net clk_mode5_0 -pin bcr_store_stat.c...
> idm::object_name __CiType_18_305d7748
> led::connect_net -net clk_mode5_0 -pin exc_info.clockbl...
> idm::object_name __CiType_18_305d7c88
> led::connect_net -net clk_mode5_0 -pin spare.clockblock...
> idm::object_name __CiType_18_305d7ef8
```

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> led::connect_net -net clk_mode5_0 -pin mcset_e1.clockbl...
> idm::object_name __CiType_18_305d8168
> led::connect_net -net clk_mode5_0 -pin eu_iu_spare.cloc...
> idm::object_name __CiType_18_305d83d8
> led::connect_net -net clk_mode5_0 -pin dsbl_ovrlp_blk.c...
> idm::object_name __CiType_18_305d8648
> led::connect_net -net clk_mode5_0 -pin inst_fetch.clock...
> idm::object_name __CiType_18_305d88b8
> led::connect_net -net clk_mode5_0 -pin iu_dsbl_ovrlp.cl...
> idm::object_name __CiType_18_305d8b28
> led::connect_net -net clk_mode5_0 -pin ex_in_prog.clock...
> idm::object_name __CiType_18_305d8d98
> led::connect_net -net clk_mode5_0 -pin blk_dcd.clockblo...
> idm::object_name __CiType_18_305d92d8
> led::connect_net -net clk_mode5_0 -pin dcd_succ_dly.clo...
> idm::object_name __CiType_18_305d9548
> led::connect_net -net clk_mode5_0 -pin exec_recov.clock...
> idm::object_name __CiType_18_305d97b8
> led::connect_net -net clk_mode5_0 -pin ru_updt_dly.cloc...
> idm::object_name __CiType_18_305d9a28
> led::connect_net -net clk_mode5_0 -pin iu_rstfst_t1.cl...
> idm::object_name __CiType_18_305d9c98
> led::connect_net -net clk_mode5_0 -pin inst_store.clock...
> idm::object_name __CiType_18_305d9f08
> led::connect_net -net clk_mode5_0 -pin eu_dsbl_aftr.clo...
> idm::object_name __CiType_18_305da178
> led::connect_net -net clk_mode5_0 -pin dcdsuc_err.clock...
> idm::object_name __CiType_18_305da3e8
> led::connect_net -net clk_mode5_0 -pin dcd_cyl_cnt.cloc...
> idm::object_name __CiType_18_305da748
> led::connect_net -net clk_mode5_0 -pin blk_mccend.clockb...
> idm::object_name __CiType_18_305da9b8
> led::connect_net -net clk_mode5_0 -pin op_44_info.clock...
> idm::object_name __CiType_18_305dad18
> led::connect_net -net clk_mode5_0 -pin rcvry_reset.cloc...
> idm::object_name __CiType_18_305daf88
> led::connect_net -net clk_mode5_0 -pin br_wrongs.clockb...
> idm::object_name __CiType_18_305db1f8
> led::connect_net -net clk_mode5_0 -pin rsttr_reset.cloc...
> idm::object_name __CiType_18_305db468
> led::connect_net -net clk_mode5_0 -pin br_dcd_pend.cloc...
> idm::get_active_network
> idm::locate_net -proto_box __CiType_16_30a445c8 -name cl...
> led::create_net -name clk_mode6_0
> idm::object_name __CiType_18_305b1a98
> led::connect_net -net clk_mode6_0 -pin gprr_latch/clkl...
> idm::object_name __CiType_18_305b89c8
> led::connect_net -net clk_mode6_0 -pin slow_mode.clockb...
> idm::object_name __CiType_18_305b8c38
> led::connect_net -net clk_mode6_0 -pin ru_rq_blk.clockb...
> idm::object_name __CiType_18_305b8ea8
> led::connect_net -net clk_mode6_0 -pin iu_rstfst.clock...
> idm::object_name __CiType_18_305d17d8
> led::connect_net -net clk_mode6_0 -pin iu_restart.clock...
> idm::object_name __CiType_18_305d1a48

```

```

> led::connect_net -net clk_mode6_0 -pin ia_to_if.clockbl...
> idm::object_name __CiType_18_305d1cb8
> led::connect_net -net clk_mode6_0 -pin frc_mmode.clockb...
> idm::object_name __CiType_18_305d1f28
> led::connect_net -net clk_mode6_0 -pin local_milli.cloc...
> idm::object_name __CiType_18_305d2198
> led::connect_net -net clk_mode6_0 -pin ia_to_if_t1.cloc...
> idm::object_name __CiType_18_305d2408
> led::connect_net -net clk_mode6_0 -pin mia_to_if.clockb...
> idm::object_name __CiType_18_305d2678
> led::connect_net -net clk_mode6_0 -pin slow_mode_t1.clo...
> idm::object_name __CiType_18_305d28e8
> led::connect_net -net clk_mode6_0 -pin iq_empty_dly.clo...
> idm::object_name __CiType_18_305d2b58
> led::connect_net -net clk_mode6_0 -pin slow_mode_t2.clo...
> idm::object_name __CiType_18_305d2dc8
> led::connect_net -net clk_mode6_0 -pin s390_updt_blk.cl...
> idm::object_name __CiType_18_305d3038
> led::connect_net -net clk_mode6_0 -pin srlz_nomatch.clo...
> idm::object_name __CiType_18_305d32a8
> led::connect_net -net clk_mode6_0 -pin bce_hold_aa.cloc...
> idm::object_name __CiType_18_305d3518
> led::connect_net -net clk_mode6_0 -pin srlz_actn.clockb...
> idm::object_name __CiType_18_305d3878
> led::connect_net -net clk_mode6_0 -pin op_44_dcd.clockb...
> idm::object_name __CiType_18_305d3ae8
> led::connect_net -net clk_mode6_0 -pin op_cmp_tr.clockb...
> idm::object_name __CiType_18_305d3d58
> led::connect_net -net clk_mode6_0 -pin num_dcd.clockblo...
> idm::object_name __CiType_18_305d40b8
> led::connect_net -net clk_mode6_0 -pin mia_to_if_t1.clo...
> idm::object_name __CiType_18_305d4328
> led::connect_net -net clk_mode6_0 -pin eu_op_encode.clo...
> idm::object_name __CiType_18_305d4fe8
> led::connect_net -net clk_mode6_0 -pin frc_blk_1cyc.clo...
> idm::object_name __CiType_18_305d5258
> led::connect_net -net clk_mode6_0 -pin local_milli_t1.c...
> idm::object_name __CiType_18_305d54c8
> led::connect_net -net clk_mode6_0 -pin local_milli_t2.c...
> idm::object_name __CiType_18_305d5738
> led::connect_net -net clk_mode6_0 -pin bht_block.clockb...
> idm::object_name __CiType_18_305d59a8
> led::connect_net -net clk_mode6_0 -pin srlz_blk.clockbl...
> idm::object_name __CiType_18_305d5c18
> led::connect_net -net clk_mode6_0 -pin exc_cond.clockbl...
> idm::object_name __CiType_18_305d5e88
> led::connect_net -net clk_mode6_0 -pin slow_mode_dly.cl...
> idm::object_name __CiType_18_305d60f8
> led::connect_net -net clk_mode6_0 -pin dcd_succ_disable...
> idm::object_name __CiType_18_305d6548
> led::connect_net -net clk_mode6_0 -pin drain_blk.clockb...
> idm::object_name __CiType_18_305d67b8
> led::connect_net -net clk_mode6_0 -pin dcd_ilc.clockblo...
> idm::object_name __CiType_18_305d6b18
> led::connect_net -net clk_mode6_0 -pin slow_mode_blk.cl...

```

```

> idm::object_name __CiType_18_305d6d88
> led::connect_net -net clk_mode6_0 -pin op_cmp_44.clockb...
> idm::object_name __CiType_18_305d6ff8
> led::connect_net -net clk_mode6_0 -pin op_cmp_dsbl.cloc...
> idm::object_name __CiType_18_305d7268
> led::connect_net -net clk_mode6_0 -pin eu_frc_milli.clo...
> idm::object_name __CiType_18_305d74d8
> led::connect_net -net clk_mode6_0 -pin bcr_store_stat.c...
> idm::object_name __CiType_18_305d7748
> led::connect_net -net clk_mode6_0 -pin exc_info.clockbl...
> idm::object_name __CiType_18_305d7c88
> led::connect_net -net clk_mode6_0 -pin spare.clockblock...
> idm::object_name __CiType_18_305d7ef8
> led::connect_net -net clk_mode6_0 -pin mcset_e1.clockbl...
> idm::object_name __CiType_18_305d8168
> led::connect_net -net clk_mode6_0 -pin eu_iu_spare.cloc...
> idm::object_name __CiType_18_305d83d8
> led::connect_net -net clk_mode6_0 -pin dsbl_ovrlp_blk.c...
> idm::object_name __CiType_18_305d8648
> led::connect_net -net clk_mode6_0 -pin inst_fetch.clock...
> idm::object_name __CiType_18_305d88b8
> led::connect_net -net clk_mode6_0 -pin iu_dsbl_ovrlp.cl...
> idm::object_name __CiType_18_305d8b28
> led::connect_net -net clk_mode6_0 -pin ex_in_prog.clock...
> idm::object_name __CiType_18_305d8d98
> led::connect_net -net clk_mode6_0 -pin blk_dcd.clockblo...
> idm::object_name __CiType_18_305d92d8
> led::connect_net -net clk_mode6_0 -pin dcd_succ_dly.clo...
> idm::object_name __CiType_18_305d9548
> led::connect_net -net clk_mode6_0 -pin exec_recov.clock...
> idm::object_name __CiType_18_305d97b8
> led::connect_net -net clk_mode6_0 -pin ru_updt_dly.cloc...
> idm::object_name __CiType_18_305d9a28
> led::connect_net -net clk_mode6_0 -pin iu_rstfst_t1.cl...
> idm::object_name __CiType_18_305d9c98
> led::connect_net -net clk_mode6_0 -pin inst_store.clock...
> idm::object_name __CiType_18_305d9f08
> led::connect_net -net clk_mode6_0 -pin eu_dsbl_aftr.clo...
> idm::object_name __CiType_18_305da178
> led::connect_net -net clk_mode6_0 -pin dcdsuc_err.clock...
> idm::object_name __CiType_18_305da3e8
> led::connect_net -net clk_mode6_0 -pin dcd_cyl_cnt.cloc...
> idm::object_name __CiType_18_305da748
> led::connect_net -net clk_mode6_0 -pin blk_mccnd.clockb...
> idm::object_name __CiType_18_305da9b8
> led::connect_net -net clk_mode6_0 -pin op_44_info.clock...
> idm::object_name __CiType_18_305dad18
> led::connect_net -net clk_mode6_0 -pin rcvry_reset.cloc...
> idm::object_name __CiType_18_305daf88
> led::connect_net -net clk_mode6_0 -pin br_wrongs.clockb...
> idm::object_name __CiType_18_305db1f8
> led::connect_net -net clk_mode6_0 -pin rsttr_reset.cloc...
> idm::object_name __CiType_18_305db468
> led::connect_net -net clk_mode6_0 -pin br_dcd_pend.cloc...
> CTE::cte_lcb_drv {MERGE_BOOKS TRUE}

```

[cte_lcb_drv]: (W) Internal error : Row 1 for XRFCBA has errors
[cte_lcb_drv]: (W) Internal error : Row 2 for cb_clk_32_1 has errors
[cte_lcb_drv]: (W) Internal error : Row 4 for cb_mode_block has errors
[cte_lcb_drv]: Merging books by DRV input nets due to MERGE_BOOKS setting.
[cte_lcb_drv]: Merging of LCB/DRV books only based on input pins matching exactly.

Index	Usage box name	Def box name inputs
[cte_lcb_drv]:	Merging books by LCB input nets due to MERGE_BOOKS setting.	
[cte_lcb_drv]:	Merging of LCB/DRV books only based on input pins matching exactly.	
[cte_lcb_drv]:	Transferred ru_rq_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ru_rq_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ru_rq_blk.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iu_rst_fst.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iu_rst_fst.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iu_rst_fst.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iu_restart.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iu_restart.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iu_restart.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ia_to_if.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ia_to_if.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ia_to_if.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred frc_mmode.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred frc_mmode.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred frc_mmode.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred local_milli.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred local_milli.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred local_milli.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ia_to_if_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ia_to_if_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred ia_to_if_t1.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred mia_to_if.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred mia_to_if.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred mia_to_if.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred slow_mode_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred slow_mode_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred slow_mode_t1.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iq_empty_dly.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iq_empty_dly.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred iq_empty_dly.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred slow_mode_t2.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred slow_mode_t2.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred slow_mode_t2.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred s390_updt_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred s390_updt_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred s390_updt_blk.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_nomatch.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_nomatch.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_nomatch.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred bce_hold_aa.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred bce_hold_aa.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred bce_hold_aa.reg_n.lat_0 pin clka to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_actn.reg_n.lat_0 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_actn.reg_n.lat_1 pin c1 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_actn.reg_n.lat_0 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_actn.reg_n.lat_1 pin c2 to slow_mode.clockblock	
[cte_lcb_drv]:	Transferred srlz_actn.reg_n.lat_0 pin clka to slow_mode.clockblock	

[illegible]

[illegible]

[illegible]

[cte_lcb_drv]: Transferred inst_store.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_dsbl_aftr.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_dsbl_aftr.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_dsbl_aftr.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcdsuc_err.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcdsuc_err.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcdsuc_err.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_mcend.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_mcend.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_mcend.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred rcvry_reset.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rcvry_reset.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rcvry_reset.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_wrongs.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_wrongs.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_wrongs.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred rst_rst_reset.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rst_rst_reset.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rst_rst_reset.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_dcd_pend.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_dcd_pend.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_dcd_pend.reg_n.lat_0 pin clka to slow_mode.clockblock

Index	Usage box name	Def box name inputs
0	slow_mode.clockblock	XRFCBA 10

[cte_lcb_drv]: Found 1 LCBs and created 5 new LCBs

[cte_lcb_drv]: Found 1 DRVs and created 0 new DRVs

> idm::filter -on gates -expr {[regexp XRFCBA @def_name]}

> idm::object_name __CiType_18_305b89c8

[cte_fixmodeblock.tcl]: slow_mode.clockblock

> idm::object_name __CiType_18_305b89c8

> rebind -gates slow_mode.clockblock -new_cell cb_clk_32_1...

> idm::object_name __CiType_18_305db468

[cte_fixmodeblock.tcl]: slow_mode.clockblock_1

> idm::object_name __CiType_18_305db468

> rebind -gates slow_mode.clockblock_1 -new_cell cb_clk_32...

> idm::object_name __CiType_18_305db1f8

[cte_fixmodeblock.tcl]: slow_mode.clockblock_2

> idm::object_name __CiType_18_305db1f8

> rebind -gates slow_mode.clockblock_2 -new_cell cb_clk_32...

> idm::object_name __CiType_18_305daf88

[cte_fixmodeblock.tcl]: slow_mode.clockblock_3

> idm::object_name __CiType_18_305daf88

> rebind -gates slow_mode.clockblock_3 -new_cell cb_clk_32...

```

> idm::object_name __CiType_18_305dad18
[cte_fixmodeblock.tcl]: slow_mode.clockblock_4
> idm::object_name __CiType_18_305dad18
> rebind -gates slow_mode.clockblock_4 -new_cell cb_clk_32...
> idm::object_name __CiType_18_305da9b8
[cte_fixmodeblock.tcl]: slow_mode.clockblock_5
> idm::object_name __CiType_18_305da9b8
> rebind -gates slow_mode.clockblock_5 -new_cell cb_clk_32...
> cleanse
> padnet
[[padnet]]: (W) Feed-thru or mult-PO net dcd_succ_last_t1 has been renamed to dcd_succ_last_t1&0 at
proto pin dcd_succ_last_t1 because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net dcd_success_tr has been renamed to dcd_success_tr&0 at
proto pin dcd_success_tr because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net dcd_succ_first_t1 has been renamed to dcd_succ_first_t1&0 at
proto pin dcd_succ_first_t1 because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_milli_mode_t1 has been renamed to iu_milli_mode_t1&0 at
proto pin iu_milli_mode_t1 because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_milli_mode_t2 has been renamed to iu_milli_mode_t2&0 at
proto pin iu_milli_mode_t2 because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_exc_cond has been renamed to iu_exc_cond&0 at proto pin
iu_exc_cond because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_inrupt_info(0) has been renamed to iu_inrupt_info&0(0) at
proto pin iu_inrupt_info(0) because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_inrupt_info(1) has been renamed to iu_inrupt_info&0(1) at
proto pin iu_inrupt_info(1) because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_inrupt_info(2) has been renamed to iu_inrupt_info&0(2) at
proto pin iu_inrupt_info(2) because itconnects to multiple proto pins.
[[padnet]]: (W) Feed-thru or mult-PO net iu_inrupt_info(3) has been renamed to iu_inrupt_info&0(3) at
proto pin iu_inrupt_info(3) because itconnects to multiple proto pins.
> summary_report

```

The model <IDCDSUC> has:

Primary Inputs	=	122
Primary Outputs	=	73
Primary BIDs	=	0
Signals	=	1033
Gate Count	=	810
Connections	=	1757
Master REG Bits	=	83
Slave REG Bits	=	83
Internal Area	=	550
External Area	=	0
Gates/Connects	=	0.461013
Fanout Count	=	1757
Average Fanout	=	1.700871
Avg Tech Box Size	=	0.679012
Tech Box Size Stddev	=	0.008999
Power	=	0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals	=	659
Real boxes	=	435
Real connections	=	1382
Real LSTs	=	2041

Real ICells/box = 1.264368
 Real LSTs/box = 4.691954
 Real nets/box = 1.514943

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
164	AND	>	AND	0	0	0.000	0	0	0.000		
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
62	NAND	>	NAND	0	0	0.000	0	0	0.000		
23	NOR	>	NOR	0	0	0.000	0	0	0.000		
91	OR	>	OR	0	0	0.000	0	0	0.000		
83	XDLATCORE	>	REG	0	0	0.000	0	0	0.000		
1	cb_mode_block	A >	SEQUENTIAL	70	0	0.000	70	0	0.000		
6	cb_clk_32_1	>	SEQUENTIAL	80	0	0.000	480	0	0.000		
5	XOR	>	XOR	0	0	0.000	0	0	0.000		

[End of measure]

[measure]: Execution time was 0.0 seconds.

> hidetech HIDE(BLACKBOX)
 > summary_report

The model <IDCDSUC> has:

Primary Inputs = 122
 Primary Outputs = 73
 Primary BIDs = 0
 Signals = 1033
 Gate Count = 810
 Connections = 1757
 Master REG Bits = 83
 Slave REG Bits = 83
 Internal Area = 550
 External Area = 0
 Gates/Connects = 0.461013
 Fanout Count = 1757
 Average Fanout = 1.700871
 Avg Tech Box Size = 0.679012
 Tech Box Size Stddev = 0.008999
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 659
 Real boxes = 435
 Real connections = 1382
 Real LSTs = 2041
 Real ICells/box = 1.264368
 Real LSTs/box = 4.691954
 Real nets/box = 1.514943

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
164	AND	>	AND	0	0	0.000	0	0	0.000		
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		

```

195  IOPAD          >  IOPAD  0  0  0.000  0  0  0.000
62   NAND          >  NAND   0  0  0.000  0  0  0.000
23   NOR           >  NOR    0  0  0.000  0  0  0.000
91   OR            >  OR     0  0  0.000  0  0  0.000
83   XDLATCORE     >  REG    0  0  0.000  0  0  0.000
1    cb_mode_block A > SEQUENTIAL 70  0  0.000  70  0  0.000
6    cb_clk_32_1   > SEQUENTIAL 80  0  0.000  480  0  0.000
5    XOR           >  XOR    0  0  0.000  0  0  0.000

```

[End of measure]

[measure]: Execution time was 0.0 seconds.

> source gp_unmap_reg.tcl

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/gp_unmap_reg.tcl

> observe -none

[gp_unmap_reg.tcl]: Unmapping all gates bound to: cmsff_sc_a

[gp_unmap_reg.tcl]: Unmapping all gates bound to: cns_msff_a

[gp_unmap_reg.tcl]: Unmapping all gates bound to: csl_scan_a

[gp_unmap_reg.tcl]: Unmapping all gates bound to: csl_ns_a

[gp_unmap_reg.tcl]: Unmapping all gates bound to: cls_msc_a

[gp_unmap_reg.tcl]: Unmapping all gates bound to: cs_cns_msffa

[gp_unmap_reg.tcl]: Unmapping all gates bound to: CMSFF_SC_A

[gp_unmap_reg.tcl]: Unmapping all gates bound to: CNS_MSFF_A

[gp_unmap_reg.tcl]: Unmapping all gates bound to: CSL_SCAN_A

[gp_unmap_reg.tcl]: Unmapping all gates bound to: CSL_NS_A

[gp_unmap_reg.tcl]: Unmapping all gates bound to: CSL_MSC_A

[gp_unmap_reg.tcl]: Unmapping all gates bound to: CS_CNS_MSFFA

[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLLAT6S

[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLDLATS

[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLLAT2S

[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLLAT5S

[gp_unmap_reg.tcl]: Unmapping all gates bound to: XDLATR

[gp_unmap_reg.tcl]: Unmapping all gates bound to: XDLATCORE

[gp_unmap_reg.tcl]: Unmapping all gates bound to: XSCANCORE

> nextbox xpndregs

[multick]: Release 1.0 Compiled on Feb 17 1999 at 16:37:02.

[multick]: There are 2 clock pins and 6 clock blocks

> cleanse

> check_model_report

[BD-40132]: Network IDCDSUC has no potential problems.

[ctesynz_cp.tcl]: SEARCH auto_path set to . ./tcl ./dll /afs/apd.pok.ibm.com/u/lacey/tcl

/afs/apd.pok.ibm.com/u/lacey/dll /afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/tcl

/afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/dll /afs/watson/projects/vlsi/cte/tools/synzilla/1.0/tcl

/afs/watson/projects/vlsi/cte/tools/synzilla/1.0/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/tcl

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/dft

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll-rs6000/.

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/wizard/3.1/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.

```

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/dll-rs_aix41/.
/afs/eda/project/EinsTimer/0301.stage/modules/einstimer/3.1/dll
/afs/eda.fishkill.ibm.com/prod/einstimer/3.1/dll
***** start Synzilla *****
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/write_synz.tcl
> use_cds
The Constant Delay Synthesis Engine is under development and should
be considered experimental.
> use_cds
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/hnl.dll
hnl.dll version 1.0 (Apr 14 1999 18:12:01)
HNL Banner
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll-rs6000/synzext.dll
synzext.dll version 1.1 (Apr 14 1999 17:23:02)
Synzilla Extension
> write_top -dir /data/lacey/synztmp/IDCDSUC -root IDCDSUC
bdz> export_envs 1
> write_vim_as_hnl -file /data/lacey/synztmp/IDCDSUC/IDCD...
bdz> synzprep
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/synzprep.tcl
> expand -view HISVHDL -hierarchy -hide
bdz> post_expand
> sweep
> delbrkpt BREAKLOOPS
> brkloops
> nextnet {delkey( EDIFNAME )}
> nextbox {delkey( EDIFNAME )}
> set_nochange
> rtoibox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
> sweep
> ltoibox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
> sweep
> nochange
> nextbox_with_test test_key(IOPAD_LOCATION,2),resolve_net...
> nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
> sweep
> nextbox merge_dots()
> nextbox dot2ms()
> nextnet {ms2dot( BUS )}
> good_names

```

Good names for IDCDSUC

			Count	User	Like	New
For all nets	1033	66.12%	13.84%	20.04%		
For register output nets	166	100.00%	0.00%	0.00%		
For break point input nets	180	100.00%	0.00%	0.00%		
For model input/output nets	195	94.87%	5.13%	0.00%		

			Count	User	Like	New
For all boxes	810	53.58%	0.00%	46.42%		
For register boxes	83	100.00%	0.00%	0.00%		

```

> view_name_is VHDL1076
> view_name_is HIAVIEW
> view_name_is HISVHDL
> proto_get_int HIS_BD_VIM_SYNC,0

```



```

> proto_get_int HISPREPSCN,0
> view_name_is BSN
> good_names

```

Good names for IDCDSUC

			Count	User	Like	New
For all nets	1033	66.12%	13.84%	20.04%		
For register output nets	166	100.00%	0.00%	0.00%		
For break point input nets	180	100.00%	0.00%	0.00%		
For model input/output nets	195	94.87%	5.13%	0.00%		

			Count	User	Like	New
For all boxes	810	53.58%	0.00%	46.42%		
For register boxes	83	100.00%	0.00%	0.00%		

```

> copyinfo
> any_dontcare
> nextbox_with_test test_syn_hide(!HIDE_MAP,!HIDE_DOMINANT...
> nextbox_with_test test_syn_hide(!HIDE_MAP),decode_or
> nextbox_with_test test_syn_hide(!HIDE_MAP),decode_and
> propcon 1
> cleanup 1
> nextbox prep_minterm,minterm
> any_dontcare
> cleanse
> nextbox mapterm
> has_children CONSTANT
> nextbox mapcon
> nextbox_with_test test_syn_hide(HIDE_MAP),mapcomp,mapadd...

```

[mapadd]: Execution time was 0.0 seconds.

```

> nextbox xpndcomp
> nextbox xpndmux
> nextbox xpndsel,xpnddcd
> nextbox xpndadd
> nextbox xpndao
> nextbox xpndcsa
> cleanse
> fixpads
> unpadnet
> good_names

```

Good names for IDCDSUC

			Count	User	Like	New
For all nets	838	75.30%	0.00%	24.70%		
For register output nets	166	100.00%	0.00%	0.00%		
For break point input nets	180	100.00%	0.00%	0.00%		
For model input/output nets	185	100.00%	0.00%	0.00%		

			Count	User	Like	New
For all boxes	615	70.57%	0.00%	29.43%		
For register boxes	83	100.00%	0.00%	0.00%		

```

> synzexpnd -hierarchy
> checksrc
> msg::get_level -msgid BD-41519
> msg::set_level -msgid BD-41519 -hidden
> expand -view SYNZ_EXPANSIONS -hide -copy_all_keys

```

```

bdz> post_expand
> sweep
> delbrkpt BREAKLOOPS
> brkloops
> nextnet {delkey( EDIFNAME )}
> nextbox {delkey( EDIFNAME )}
    > set_nochange
    > rtoibox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
    > sweep
    > ltoibox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
    > sweep
    > nochange
> nextbox_with_test test_key(IOPAD_LOCATION,2),resolve_net...
> nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
> sweep
> nextbox merge_dots()
> nextbox dot2ms()
> nextnet {ms2dot( BUS )}
> expand -view SYNZ_EXPANSIONS -hide -copy_all_keys

```

```

bdz> post_expand
> sweep
> delbrkpt BREAKLOOPS
> brkloops
> nextnet {delkey( EDIFNAME )}
> nextbox {delkey( EDIFNAME )}
    > set_nochange
    > rtoibox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
    > sweep
    > ltoibox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
    > sweep
    > nochange
> nextbox_with_test test_key(IOPAD_LOCATION,2),resolve_net...
> nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
> sweep
> nextbox merge_dots()
> nextbox dot2ms()
> nextnet {ms2dot( BUS )}
> msg::set_level -msgid BD-41519 -warning

```

[SynzExt-19]: Wrote design hierarchy IDCDSUC with 2 proto boxes to HNL file
'/data/lacey/synztmp/IDCDSUC/IDCDSUC.hnl'

> write_timer_parms -file /data/lacey/synztmp/IDCDSUC/IDC...

[ICM-15]: >Begin...Parms Export

for file /data/lacey/synztmp/IDCDSUC/IDCDSUC.tparms.

[ICM-16]: <End.....Parms Export.

> write_lib -file /data/lacey/synztmp/IDCDSUC/IDCDSUC/CC8...

[SynzExt-22]: Writing to file /data/lacey/synztmp/IDCDSUC/IDCDSUC/CC8S.lib

Please wait while the Constant Delay Synthesis engine is initialized...

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/tcl/8.0/dll-rs6000/expect.dll
expect.dll version 5.26 (Nov 19 1998 15:52:48)

Expect Tcl extension

> observe

observe -none -ci_cmds read_bdz -remove -dir /data/lacey/synztmp/IDCDSUC -file IDCDSUC -libanal
bscc8_anal.tcl -no_liblint -no_interact -no_assert Loading:
/data/lacey/synztmp/IDCDSUC/IDCDSUC/top.tcl

```

Synz                      -----                      Nutshell version 1.672
(03-25-1999)              Licensed Materials - Property of IBM
5765-XXX                  (C) Copyright IBM Corporation 1997      All Rights Reserved
Install Directory: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0 Machine: bsp5n11, AIX
4.1 32bit, 595 POWER2 (L1 i32k d128k, L2 0k), 1 cpu Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/.synz Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/hnl.dll hnl.dll version 1.0 (Apr 14 1999
18:12:01) HNL Banner Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/dll/license.dll
license.dll version 3.1 (Apr 07 1999 14:28:56) Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/timer.dll timer.dll version 1.0 (Apr 14
1999 18:12:09) [ET-0101]:Initializing EinsTimer...          CMVC Release Level: 03.01          Compiled: Fri
Feb 5 09:05:11 1999 [ET-0102]:EinsTimer Version 3 Release 1    Licensed Materials-Property of
IBM          5765-801 (C) Copyright IBM Corp. 1994-97        All rights reserved.          US
Government Users Restricted Rights -          Use, duplication or disclosure restricted          by GSA
Schedule Contract with IBM Corp.              "IBM" and "EinsTimer" are trademarks of
"International Business Machines" [ET-0110]:License obtained for ..... EinsTimer 1.1 Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/synzilla.dll synzilla.dll version 1.0 (Apr
16 1999 10:14:14) Synzilla Build Version: 1.0.219 Load calculator version 2 - initialized Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/synz_init.tcl Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/create_attributes.tcl Loading:
/afs/apd.pok.ibm.com/u/lacey/l/.synz_variables Interactive nutshell, "help" for help, "exit" or ctrl-d to exit.
[] [7msynz>[] [0m>[] [1m>@bsp5n11>>[] [0m
>[] [14Cobserve -none -ci_cmds>[] [7msynz>[] [0m>[] [1m>@bsp5n11>>[] [0m
>[] [14Cread_bdz -remove -dir /data/lacey/synztmp/IDCDSUC -file IDCDSUC -libanal bscc8_anal.tcl
-no_liblint -no_interact -no_assert Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/read_bdz.tcl          > echo {synz interact 0}
synz interact 0          > read_timer_parms -file /data/lacey/synztmp/IDCDSUC/IDCD... ICM-015 I:
>Begin...Parm Reader          for file /data/lacey/synztmp/IDCDSUC/IDCDSUC.tparms. ICM-016 I:
<End.....Parm Reader.          > echo {Reading library file /data/lacey/synztmp/IDCDSUC/...
Reading library file /data/lacey/synztmp/IDCDSUC/IDCDSUC/CC8S.lib          > msg::get_level -msgid
MASK-108          > msg::set_level -msgid MASK-108 -hidden          > msg::set_level -msgid MASK-108
-warning          > load_cdc_rule -rule /afs/apd/func/vlsi/alliance00/bscc8/... [ET-1757]:Initializing CDC...
[ET-1758]: Rule    = /afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface_RS6K [ET-1759]: Sub
Rules =
/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/%RULENAME
[ET-1760]: Tables =
/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/tables:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/.../tables:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/%RULENAME
[ET-0607]:Starting the dynamic link to CDC for rule:
/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface_RS6K [DCL-0512]: DCL Runtime Environment
Version 3.1          Last compiled on Apr 12 1999 at 10:00:33. [DCL-0642]: I am running in process ID
147522 [DCL-17001]: RLEV: DCMinterface rule, version v1.0.2 IEEE 1481-1998, technology GENERIC,
-19009]: CAP: Setting DEFAULT PINCAP value to: 0 as defined by environment variable
<DCM_DEFAULT_PINCAP> [DCL-17001]: RLEV: Methods subrule, version v1.0.2 IEEE 1481-1998,
was compiled on 14:17:39 at Mar 12 1999 [DCL-19021]: INFO: Maximum number of DCM messages to
be printed has been set to 100000000 [DCL-17001]: RLEV: LimitPrint subrule, version v1.0 IEEE
1481-1998, was compiled on 14:17:44 at Mar 12 1999 [DCL-17001]: RLEV: printSummary subrule,
version v1.0 IEEE 1481-1998, was compiled on 14:18:37 at Mar 12 1999 [DCL-17001]: RLEV: Ceffective
subrule, version v1.0 IEEE 1481-1998, was compiled on 14:17:50 at Mar 12 1999 [DCL-19000]: ENV:
Environment variable <DCMCAPTHRESHOLD> NOT set by user. [DCL-19017]: CAP: EffectiveC Cap
Threshold not set. [DCL-17001]: RLEV: techSpec subrule, version v1.0.3 IEEE 1481-1998, was compiled
on 14:17:56 at Mar 12 1999 [DCL-17001]: RLEV: WireLoad subrule, version v1.0.1 IEEE 1481-1998, was
compiled on 14:18:04 at Mar 12 1999 [DCL-17001]: RLEV: WireLoad table, Version 1.0.1 IEEE
1481-1998 Technology SA27 , was compiled on 14:18:04 at Mar 12 1999 [DCL-17040]: The available
wireload model levels are: 5lm, 6lm [DCL-17002]: Enviromental variable DCMWireLoadLevels not set

```

using default. [DCL-17001]: RLEV: NetDelay subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:12 at Mar 12 1999 [DCL-17001]: RLEV: cellName subrule, version v1.5 IEEE 1481-1998, was compiled on 14:18:17 at Mar 12 1999 [DCL-17001]: RLEV: CellName parser subrule, version v1.0.5 IEEE 1481-1998, was compiled on 14:18:30 at Mar 12 1999 [DCL-17001]: RLEV: Defaults subrule, version v1.0.4 IEEE 1481-1998, was compiled on 14:18:40 at Mar 12 1999 [DCL-17012]: Using the default supplied bomFile [DCL-17001]: RLEV: _cc8s_rules_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 09:32:54 at Apr 12 1999 [DCL-17001]: RLEV: _cc8s_latches_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 12:12:01 at Apr 6 1999 [DCL-17001]: RLEV: railCache subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:52 at Mar 12 1999 [DCL-17020]: Enviromental variable DCMDoRangeCheck set to do no reporting. [ET-0655]:IEEE standard interface version "IEEE 1481-1998" for technology "GENERIC". Library identification: "IBM_GENERIC". [ET-0652]:Could not find IEEE standard routine dpcmGetDelayGradient in rules. Substituting dummy routine. [ET-0652]:Could not find IEEE standard routine dpcmGetSlewGradient in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGetAETCellPowerWithSensitivity in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGroupGetSettlingTime in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGroupGetSimultaneousSwitchTime in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmCalcPartialSwingEnergy in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmSetInitialState in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmFillPinCache in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmFreePinCache in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGetNetEnergy in rules. Substituting dummy routine. [ET-0611]:Dynamic link to CDC rule complete. [HNLIO-2007]: Loaded library 'HISVHDL'. > hnl::hnl_nets_preserve -initialize > echo SYNZ_READ_BDZ SYNZ_READ_BDZ > source bsc8_anal.tcl Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/bscc8_anal.tcl > echo {Setting picap to 0.2} Setting picap to 0.2 > hnl::get_active_idesign > load_units -fermo > time_units -pico > hnl_attr_get_by_name -obj_type port -name PIN_FUNCTION > top level created for design: IDCDSUC, analysis mode: SLOW_CHIP. [ET-1709]:Could not find clock or phase "C3". set load limit for port a_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port b_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port test_c1 to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port gp_tr_scan_in to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port scan_in to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port gp_tr_b_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port clk2 to 10000.0 set load limit for port scan_enable to 10000.0 [ET-1709]:Could not find clock or phase "C3". slow_mode.clockblock cb_clk_32_1 set load limit on slow_mode.clockblock/c1 to 10000.0 set slew limit on slow_mode.clockblock/c1 to 650.0 set slew limit on iu_rstfst_t1.reg_n.lat_0/C1 to 650.0 set slew limit on inst_store.reg_n.lat_0/C1 to 650.0 set slew limit on eu_dsbl_aftr.reg_n.lat_0/C1 to 650.0 set slew limit on dcdsuc_err.reg_n.lat_0/C1 to 650.0 set slew limit on dcd_cyl_cnt.reg_n.lat_0/C1 to 650.0 set slew limit on dcd_cyl_cnt.reg_n.lat_1/C1 to 650.0 set slew limit on blk_mcend.reg_n.lat_0/C1 to 650.0 set slew limit on op_44_info.reg_n.lat_0/C1 to 650.0 set slew limit on op_44_info.reg_n.lat_1/C1 to 650.0 set slew limit on rcvry_reset.reg_n.lat_0/C1 to 650.0 set slew limit on br_wrongs.reg_n.lat_0/C1 to 650.0 set slew limit on rst_rst_reset.reg_n.lat_0/C1 to 650.0 set slew limit on br_dcd_pend.reg_n.lat_0/C1 to 650.0 set load limit on slow_mode.clockblock/c2 to 10000.0 set slew limit on slow_mode.clockblock/c2 to 650.0 set slew limit on iu_rstfst_t1.reg_n.lat_0/B to 650.0 set slew limit on inst_store.reg_n.lat_0/B to 650.0 set slew limit on eu_dsbl_aftr.reg_n.lat_0/B to 650.0 set slew limit on dcdsuc_err.reg_n.lat_0/B to 650.0 set slew limit on dcd_cyl_cnt.reg_n.lat_0/B to 650.0 set slew limit on dcd_cyl_cnt.reg_n.lat_1/B to 650.0 set slew limit on blk_mcend.reg_n.lat_0/B to 650.0 set slew limit on op_44_info.reg_n.lat_0/B to 650.0 set slew limit on op_44_info.reg_n.lat_1/B to 650.0 set slew limit on rcvry_reset.reg_n.lat_0/B to 650.0 set slew limit on br_wrongs.reg_n.lat_0/B to 650.0 set slew limit on rst_rst_reset.reg_n.lat_0/B to 650.0 set slew limit on br_dcd_pend.reg_n.lat_0/B to 650.0 set load limit on slow_mode.clockblock/clka to 10000.0 set slew limit on slow_mode.clockblock/clka to 650.0 set slew limit on iu_rstfst_t1.reg_n.lat_0/A to 650.0 set slew limit on inst_store.reg_n.lat_0/A to 650.0 set slew limit on eu_dsbl_aftr.reg_n.lat_0/A to 650.0 set slew limit on

dcdsuc_err.reg_n.lat_0/A to 650.0 set slew limit on dcd_cyl_cnt.reg_n.lat_0/A to 650.0 set slew limit on dcd_cyl_cnt.reg_n.lat_1/A to 650.0 set slew limit on blk_mkend.reg_n.lat_0/A to 650.0 set slew limit on op_44_info.reg_n.lat_0/A to 650.0 set slew limit on op_44_info.reg_n.lat_1/A to 650.0 set slew limit on rcvry_reset.reg_n.lat_0/A to 650.0 set slew limit on br_wrongs.reg_n.lat_0/A to 650.0 set slew limit on rstrt_reset.reg_n.lat_0/A to 650.0 set slew limit on br_dcd_pend.reg_n.lat_0/A to 650.0 set load limit on slow_mode.clockblock/a_clk to 10000.0 set slew limit on a_clk to 650.0 set slew limit on slow_mode.clockblock/a_clk to 650.0 set slew limit on slow_mode.clockblock_1/a_clk to 650.0 set slew limit on slow_mode.clockblock_2/a_clk to 650.0 set slew limit on slow_mode.clockblock_3/a_clk to 650.0 set slew limit on slow_mode.clockblock_4/a_clk to 650.0 set slew limit on slow_mode.clockblock_5/a_clk to 650.0 set load limit on slow_mode.clockblock/b_clk to 10000.0 set slew limit on b_clk to 650.0 set slew limit on slow_mode.clockblock/b_clk to 650.0 set slew limit on slow_mode.clockblock_1/b_clk to 650.0 set slew limit on slow_mode.clockblock_2/b_clk to 650.0 set slew limit on slow_mode.clockblock_3/b_clk to 650.0 set slew limit on slow_mode.clockblock_4/b_clk to 650.0 set slew limit on slow_mode.clockblock_5/b_clk to 650.0 set load limit on slow_mode.clockblock/clkg to 10000.0 set slew limit on clkg to 650.0 set slew limit on slow_mode.clockblock/clkg to 650.0 set slew limit on slow_mode.clockblock_1/clkg to 650.0 set slew limit on slow_mode.clockblock_2/clkg to 650.0 set load limit on slow_mode.clockblock/scan_enable to 10000.0 set slew limit on scan_enable to 650.0 set slew limit on slow_mode.clockblock/scan_enable to 650.0 set slew limit on slow_mode.clockblock_1/scan_enable to 650.0 set slew limit on slow_mode.clockblock_2/scan_enable to 650.0 set slew limit on slow_mode.clockblock_3/scan_enable to 650.0 set slew limit on slow_mode.clockblock_4/scan_enable to 650.0 set slew limit on slow_mode.clockblock_5/scan_enable to 650.0 set load limit on slow_mode.clockblock/clkl_mode4 to 10000.0 set slew limit on gpтр_latch/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_3/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode4 to 650.0 set load limit on slow_mode.clockblock/clkl_mode5 to 10000.0 set slew limit on gpтр_latch/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_3/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode5 to 650.0 set load limit on slow_mode.clockblock/clkl_mode6 to 10000.0 set slew limit on gpтр_latch/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_3/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode6 to 650.0 set load limit on slow_mode.clockblock/clkl_mode7 to 10000.0 set slew limit on clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_3/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode7 to 650.0 set load limit on slow_mode.clockblock/clkl_mode8 to 10000.0 set slew limit on gpтр_latch/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_3/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode8 to 650.0 set load limit on slow_mode.clockblock/test_c1 to 10000.0 set slew limit on test_c1 to 650.0 set slew limit on slow_mode.clockblock/test_c1 to 650.0 set slew limit on slow_mode.clockblock_1/test_c1 to 650.0 set slew limit on slow_mode.clockblock_2/test_c1 to 650.0 set slew limit on slow_mode.clockblock_3/test_c1 to 650.0 set slew limit on slow_mode.clockblock_4/test_c1 to 650.0 set slew limit on slow_mode.clockblock_5/test_c1 to 650.0 slow_mode.clockblock_1 cb_clk_32_1 set load limit on slow_mode.clockblock_1/c1 to 10000.0 set slew limit on slow_mode.reg_n.lat_0/C1 to 650.0 set slew limit on ru_rq_blk.reg_n.lat_0/C1 to 650.0 set slew limit on iu_rst_fst.reg_n.lat_0/C1 to 650.0 set slew limit on iu_restart.reg_n.lat_0/C1 to 650.0 set slew limit on ia_to_if.reg_n.lat_0/C1 to 650.0 set slew limit on frc_mmode.reg_n.lat_0/C1 to 650.0 set slew limit on local_milli.reg_n.lat_0/C1 to 650.0 set slew limit on

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

```

_mode6 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode6 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode6 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode6 to 650.0 set load limit on
slow_mode.clockblock_5/clkl_mode7 to 10000.0 set slew limit on clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock_2/clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode7 to 650.0 set load limit on
slow_mode.clockblock_5/clkl_mode8 to 10000.0 set slew limit on gpnr_latch/clkl_mode8 to 650.0 set slew
limit on slow_mode.clockblock/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode8
to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode8 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode8 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode8 to 650.0 set load limit on
slow_mode.clockblock_5/test_c1 to 10000.0 set slew limit on test_c1 to 650.0 set slew limit on
slow_mode.clockblock/test_c1 to 650.0 set slew limit on slow_mode.clockblock_1/test_c1 to 650.0 set
slew limit on slow_mode.clockblock_2/test_c1 to 650.0 set slew limit on slow_mode.clockblock_3/test_c1
to 650.0 set slew limit on slow_mode.clockblock_4/test_c1 to 650.0 set slew limit on
slow_mode.clockblock_5/test_c1 to 650.0
libanal_unhide -design /CC8S/cs_invvn*
> libanal_unhide -design /CC8S/cs_nnd3n*
> libanal_unhide -design /CC8S/cs_nnd4n*
> libanal_unhide -design /CC8S/cs_nor2n*
> libanal_unhide -design /CC8S/cs_nor3n*
> libanal_unhide -design /CC8S/cs_ao12n*
> libanal_unhide -design /CC8S/cs_ao22n*
> libanal_unhide -design /CC8S/cs_ao21n*
> libanal_unhide -design /CC8S/cs_ao22n*
> libanal_unhide -design /CC8S/cs_invvn*
> libanal_unhide -design /CC8S/cs_xbn2n*
> libanal_unhide -design /CC8S/cs_xbo2n*
> libanal_build -library CC8S -library SIZELESS
[ET-0203]:Timing top level created for design: def_proto, analysis mode: default.
libanal_model -library SIZELESS -clus_ratio -clus_move -... [libanal_fit_models]: Performing analysis of
sizeless models [libanal_cluster]: Performing clustering for library SIZELESS [libanal_cluster_ratio]:
Performing clustering for design cs_ao12n03b_sl [ET-0415]:Timer/Delay computation has been triggered.
[ET-0027]:No subsequent messages of this type will be reported. Increase timing debug level for
complete set of these messages. [libanal_cluster_ratio]: Performing clustering for design cs_ao22n03b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_nnd2n02b_sl [libanal_cluster_ratio]:
Performing clustering for design cs_nnd3n02b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_nnd4n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_nor2n02b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_nor3n03b_sl [libanal_cluster_ratio]: Performing
clustering for design cs_invvn01b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_ao21n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_ao22n03b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_xbo2n01b_sl [libanal_cluster_ratio]: Performing
clustering for design cs_xbn2n01b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_ao12n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_ao22n03b_sl
ng clustering for design cs_nnd3n02b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_nnd4n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_nor2n02b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_nor3n03b_sl [libanal_cluster_ratio]: Performing
clustering for design cs_invvn01b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_ao21n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_ao22n03b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_xbo2n01e_sl [libanal_cluster_ratio]: Performing
clustering for design cs_xbn2n01e_sl [libanal_cluster_ratio]: Performing clustering for design
cs_ao12n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_ao22n03b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_nnd2n02b_sl [libanal_cluster_ratio]:
Performing clustering for design cs_nnd3n02b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_nnd4n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_nor2n02b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_nor3n03b_sl [libanal_cluster_ratio]: Performing
clustering for design cs_invvn01b_sl [libanal_cluster_ratio]: Performing clustering for design
cs_ao21n03b_sl [libanal_cluster_ratio]: Performing clustering for design cs_ao22n03b_sl
[libanal_cluster_ratio]: Performing clustering for design cs_ao12n03e_sl [libanal_cluster_ratio]:

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[illegible]

[illegible]

[illegible]

[illegible]


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constant gain for design cs_nnd2n02c_sl [libanal_set_cnst_gain]: Setting constant gain for design
cs_nnd3n02c_sl [libanal_set_cnst_gain]: Setting constant gain for design cs_nnd4n03c_sl
[libanal_set_cnst_gain]: Setting constant gain for design cs_nor2n02c_sl [libanal_set_cnst_gain]: Setting
constant gain for design cs_nor3n03b_sl [libanal_set_cnst_gain]: Setting constant gain for design
cs_invvn01c_sl [libanal_set_cnst_gain]: Setting constant gain for design cs_ao21n03c_sl
[libanal_set_cnst_gain]: Setting constant gain for design cs_ao22n03c_sl [libanal_set_cnst_gain]: Setting
constant gain for design cs_ao12n03e_sl [libanal_set_cnst_gain]: Setting constant gain for design
cs_ao22n03b_sl [libanal_set_cnst_gain]: Setting constant gain for design cs_nnd2n02b_sl
[libanal_set_cnst_gain]: Setting constant gain for design cs_nnd3n02b_sl [libanal_set_cnst_gain]: Setting
constant gain for design cs_nnd4n03b_sl [libanal_set_cnst_gain]: Setting constant gain for design
cs_nor2n02b_sl [libanal_set_cnst_gain]: Setting constant gain for design cs_nor3n03e_sl
esign cs_invvn01b_sl [libanal_set_cnst_gain]: Setting constant gain for design cs_ao21n03b_sl
[libanal_set_cnst_gain]: Setting constant gain for design cs_ao22n03b_sl [libanal_fit_models]: Updated
models load: 1, area: 1, max_load: 1, delay: 1, cnst: 1 [LA-107]: Library analysis did not identify sizeless
one. [LA-108]: Library analysis did not identify sizeless zero. [LA-110]: Library analysis did not identify
sizeless buffer. [LA-113]: Library analysis did not identify sizeless xor with 3 inputs. [libanal_index]:
Function Index Lookups [libanal_index]: ----- [libanal_index]: Inverter = cs_invvn01c_sl
[libanal_index]: Nand[2] = cs_nnd2n02c_sl [libanal_index]: Nand[3] = cs_nnd3n02c_sl [libanal_index]:
Nand[4] = cs_nnd4n03c_sl [libanal_index]: Nor[2] = cs_nor2n02c_sl [libanal_index]: Nor[3] =
cs_nor3n03c_sl [libanal_index]: Xnor[2] = cs_xbn2n01b_sl [libanal_index]: Xor[2] = cs_xbo2n01b_sl
[libanal_index]: And-Nor[2](2,2)= cs_ao22n03c_sl [libanal_index]: And-Nor[2](2,1)= cs_ao12n03c_sl
[libanal_index]: Or-Nand[2](2,2)= cs_ao22n03c_sl [libanal_index]: Or-Nand[2](2,1)= cs_ao21n03c_sl
model_prim: Using inverter cs_invvn01c_sl : delay=52.23 slew=70.09 load=5.67 >
set_prim_mode 1 > load_units -femto 42.0 > time_units -pico -value 100 >
create_pseudo_reg -library CC8S -register cl_invvn05d -i... > echo {=== Finish libanal ===} ===
Finish libanal === > echo SYNZ_READY SYNZ_READY SYNZPROMPT
[]10Cif { [ catch { ; puts "***** start Synzilla: ltc == $CTE::run_synzilla_ltc, mask_groups ==
$CTE::synzilla_mask_group" ; ; observe -ci ; source cte_setup_timer.tcl ; source cte_set_rc.tcl ; ;
CTE::cte_setup_timer ; ; opt_and_map $CTE::synzilla_mask_group DEFAULT $CTE::run_synzilla_ltc
$CTE::synzilla_complex_regs ; puts "***** end Synzilla *****" ; } result } { exit } ***** start Synzilla: ltc
== 0, mask_groups == 0 > observe -ci > source cte_setup_timer.tcl Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_setup_timer.tcl > source
cte_set_rc.tcl Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_set_rc.tcl
> read_timer_parms -file /afs/apd/func/vlsi/alliance00/tim... ICM-015 I: >Begin...Parm Reader for
file /afs/apd/func/vlsi/alliance00/timing/parms/cpsynz.parms. ICM-016 I: <End.....Parm Reader.
> set_cap_limit_calc -type_zero > set_slew_propagation -propagated > set_timer_parm
-name netcalc.net-delay-mode -value no-rcest [ET-1737]:The parameter 'netcalc.net-delay-mode' could
not be located. Use command 'create_timer_parm' to create parameter. {setting nominal delay
mode} > set_delay_mode -nominal > set_vdd -vdd_best 1.7 -vdd_worst 1.45
-vdd_nominal 1.45 > set_temp -temp_best -10 -temp_worst 10 -temp_nominal 10 >
hide_clock_tree [ET-0601]:The model build for block: gpnr_latch, cell name: cb_mode_block failed.
Default modelling will be used for this block. 0 gates were hidden. > read_phase_file -file
/afs/apd/func/vlsi/alliance00/bssc... [ET-0018]:>Begin...PHASE reader for file
/afs/apd/func/vlsi/alliance00/bssc8/v4/ndr/a00.phase. [ET-0019]:<End.....PHASE reader. >
set_default_slew -slew 151 Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/synzFuncs.tcl > set_load_limit -cap
141 -ports {op_dsbl_after eu_iu_spar... > set_load_limit -cap 1001 -ports {iu_eu_opcode_cmp
iu_rcv... > read_assertions -path /afs/apd/func/vlsi/alliance00/timi... [ET-0018]:>Begin...PIS
reader for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pis.
[ET-0016]:Pin/Net: aa_blk_dcd_prtl not found on line no: 31. [ET-0016]:Pin/Net: clk0 not found on line
no: 132. [ET-0016]:Pin/Net: clk0_0 not found on line no: 133. [ET-0016]:Pin/Net: clk0_00 not found on
in/Net: clk0_1 not found on line no: 135. [ET-0016]:Pin/Net: clk0_1 not found on line no: 136.
[ET-0016]:Pin/Net: clk0_01 not found on line no: 137. [ET-0016]:Pin/Net: clk0_2 not found on line no:
139. [ET-0016]:Pin/Net: clk0_02 not found on line no: 140. [ET-0016]:Pin/Net: clk0_3 not found on line no:
141. [ET-0016]:Pin/Net: clk0_3 not found on line no: 142. [ET-0016]:Pin/Net: clk0_03 not found on line

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no: 143. [ET-0016]:Pin/Net: clkg4 not found on line no: 144. [ET-0016]:Pin/Net: clkg_4 not found on line
no: 145. [ET-0016]:Pin/Net: clkg_04 not found on line no: 146. [ET-0016]:Pin/Net: clkg5 not found on line
no: 147. [ET-0016]:Pin/Net: clkg_5 not found on line no: 148. [ET-0016]:Pin/Net: clkg_05 not found on
line no: 149. [ET-0016]:Pin/Net: clkg6 not found on line no: 150. [ET-0016]:Pin/Net: clkg_6 not found on
line no: 151. [ET-0016]:Pin/Net: clkg_06 not found on line no: 152. [ET-0016]:Pin/Net: clkg7 not found on
line no: 153. [ET-0016]:Pin/Net: clkg_7 not found on line no: 154. [ET-0016]:Pin/Net: clkg_07 not found
on line no: 155. [ET-0016]:Pin/Net: clkg8 not found on line no: 156. [ET-0016]:Pin/Net: clkg_8 not found
on line no: 157. [ET-0016]:Pin/Net: clkg_08 not found on line no: 158. [ET-0016]:Pin/Net: clkg9 not found
on line no: 159. [ET-0016]:Pin/Net: clkg_9 not found on line no: 160. [ET-0016]:Pin/Net: clkg_09 not
found on line no: 161. [ET-0016]:Pin/Net: clkg11 not found on line no: 162. [ET-0016]:Pin/Net: clkg22 not
found on line no: 163. [ET-0016]:Pin/Net: clkg33 not found on line no: 164. [ET-0019]:<End.....PIS
reader. [ET-0018]:>Begin...ETA reader for file
/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.eta. [ET-0019]:<End.....ETA reader.
[ET-0018]:>Begin...POS reader for file
/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pos. [ET-0019]:<End.....POS reader.
> hnl::all_inputs > get_asserted_phases -pin op_dsbl_after -at >
get_asserted_phases -pin eu_iu_spare1 -at > get_asserted_phases -pin second_op_lat -at
> get_asserted_phases -pin mcr41_trap -at > get_asserted_phases -pin ifet_xcptn -at
> get_asserted_phases -pin iu_eu_xcpt_pend -at > get_asserted_phases -pin iq_blk_d1 -at
> get_asserted_phases -pin clk_mode7 -at Pin: NO PHASES for clk_mode7: asserting default C3+R
> set_arrival -time 401 -phase C3+R -ports clk_mode7 -late > set_arrival -time 101 -phase
C3+R -ports clk_mode7 -early > get_asserted_phases -pin dcd_op_44 -at >
get_asserted_phases -pin ru_write_in_iq -at > get_asserted_phases -pin a_clk -at Pin: NO
PHASES for a_clk: asserting default C3+R > set_arrival -time 401 -phase C3+R -ports a_clk
-late > set_arrival -time 101 -phase C3+R -ports a_clk -early > get_asserted_phases
-pin b_clk -at Pin: NO PHASES for b_clk: asserting default C3+R > set_arrival -time 401
-phase C3+R -ports b_clk -late > set_arrival -time 101 -phase C3+R -ports b_clk -early
> get_asserted_phases -pin ru_iu_rcvy_rst -at > get_asserted_phases -pin
eu_iu_enter_slow_md -at > get_asserted_phases -pin id_instr_stores -at >
get_asserted_phases -pin op_inq_stores -at > get_asserted_phases -pin test_c1 -at Pin: NO
PHASES for test_c1: asserting default C3+R > set_arrival -time 401 -phase C3+R -ports
test_c1 -late > set_arrival -time 101 -phase C3+R -ports test_c1 -early >
get_asserted_phases -pin iq_blk_aa -at > get_asserted_phases -pin aa_ofc_available -at
> get_asserted_phases -pin eu_iu_mmode -at > get_asserted_phases -pin eu_iu_mcset_e1 -at
_ asserted_phases -pin ru_98_43 -at > get_asserted_phases -pin srlz_op_match -at >
get_asserted_phases -pin first_op_lat -at > get_asserted_phases -pin zero_branches -at
> get_asserted_phases -pin dcd_mcr41_blk -at > get_asserted_phases -pin xu_iu_xlat_busy
-at > get_asserted_phases -pin du_iu_hold_aa_req -at > get_asserted_phases -pin
eu_iu_fpu_end_op -at > get_asserted_phases -pin eu_iu_misc_hold -at >
get_asserted_phases -pin op_cmp_raw -at > get_asserted_phases -pin op_dsbl_before -at
> get_asserted_phases -pin op_drain -at > get_asserted_phases -pin eu_iu_fxu_end_op -at
> get_asserted_phases -pin op_mccend_raw -at > get_asserted_phases -pin eu_iu_br_wrong
-at > get_asserted_phases -pin need_opnd_req -at > get_asserted_phases -pin
legal_bht_br -at > get_asserted_phases -pin clkg -at > get_asserted_phases -pin
bht_branch_req -at Pin: NO PHASES for bht_branch_req: asserting default C3+R >
set_arrival -time 401 -phase C3+R -ports bht_branch_req ... > set_arrival -time 101 -phase
C3+R -ports bht_branch_req ... > get_asserted_phases -pin id_ex_in_mm -at >
get_asserted_phases -pin du_iu_quiesced -at > get_asserted_phases -pin iu_op_cmp_hit_a -at
> get_asserted_phases -pin iu_op_cmp_hit_b -at > get_asserted_phases -pin iu_op_cmp_hit_c
-at > get_asserted_phases -pin iu_op_cmp_hit_d -at > get_asserted_phases -pin
dcd_frc_milli -at > get_asserted_phases -pin iq_empty -at > get_asserted_phases
-pin op_serialize -at > get_asserted_phases -pin gpnr_scan_in -at Pin: NO PHASES for
gpnr_scan_in: asserting default C3+R > set_arrival -time 401 -phase C3+R -ports
gpnr_scan_in -late > set_arrival -time 101 -phase C3+R -ports gpnr_scan_in -e... >
get_asserted_phases -pin aa_agi_lat -at > get_asserted_phases -pin branch_request -at

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> get_asserted_phases -pin ru_9a_52 -at > get_asserted_phases -pin bu_iu_quiesced -at
> get_asserted_phases -pin dcd_blk_dsucc -at > get_asserted_phases -pin op_eim_dcd -at
> get_asserted_phases -pin iqrcode_mod_390gr -at > get_asserted_phases -pin scan_in -at
Pin: NO PHASES for scan_in: asserting default C3+R > set_arrival -time 401 -phase C3+R
-ports scan_in -late > set_arrival -time 101 -phase C3+R -ports scan_in -early >
get_asserted_phases -pin eu_iu_e1_exc_cond -at > get_asserted_phases -pin
aa_ofc_block_req -at > get_asserted_phases -pin eu_iu_fpu_excptn -at >
get_asserted_phases -pin block_aa_branch -at > get_asserted_phases -pin ru_iu_rq_blk -at
> get_asserted_phases -pin op_chkpt_synch -at > get_asserted_phases -pin ireg_valid -at
> get_asserted_phases -pin ru_9a_36 -at > get_asserted_phases -pin three_branches -at
> get_asserted_phases -pin bht_block_dcd -at Pin: NO PHASES for bht_block_dcd: asserting default
C3+R > set_arrival -time 401 -phase C3+R -ports bht_block_dcd -... > set_arrival
-time 101 -phase C3+R -ports bht_block_dcd -... > get_asserted_phases -pin ru_9a_20 -at
> get_asserted_phases -pin iu_eu_data_blocked -at > get_asserted_phases -pin gptra_a_clk -at
Pin: NO PHASES for gptra_a_clk: asserting default C3+R > set_arrival -time 401 -phase C3+R
> get_asserted_phases -pin gptra_b_clk -at Pin: NO PHASES for gptra_b_clk: asserting default C3+R
> set_arrival -time 401 -phase C3+R -ports gptra_b_clk -late > set_arrival -time 101 -phase
C3+R -ports gptra_b_clk -early > get_asserted_phases -pin op_is_44 -at >
get_asserted_phases -pin inst_fetches -at > get_asserted_phases -pin clk2 -at >
get_asserted_phases -pin eu_iu_fpu_exc_cond -at > get_asserted_phases -pin ru_9a_04 -at
> get_asserted_phases -pin br_wrong_targ -at > get_asserted_phases -pin scan_enable -at
> get_asserted_phases -pin du_iu_store_status(0) -at > get_asserted_phases -pin
du_iu_store_status(1) -at > get_asserted_phases -pin du_iu_store_status(2) -at >
get_asserted_phases -pin eu_iu_srlz_op_actn(0) -at > get_asserted_phases -pin
eu_iu_srlz_op_actn(1) -at > get_asserted_phases -pin ru_9a_0001(0) -at >
get_asserted_phases -pin ru_9a_0001(1) -at > get_asserted_phases -pin ireg_0_1(0) -at
> get_asserted_phases -pin ireg_0_1(1) -at > get_asserted_phases -pin num_dcd_cyl(0) -at
> get_asserted_phases -pin num_dcd_cyl(1) -at > get_asserted_phases -pin ru_9a_3233(32)
-at > get_asserted_phases -pin ru_9a_3233(33) -at > get_asserted_phases -pin
eu_iu_interrupt_info(0) -at > get_asserted_phases -pin eu_iu_interrupt_info(1) -at >
get_asserted_phases -pin eu_iu_interrupt_info(2) -at > get_asserted_phases -pin
eu_iu_interrupt_info(3) -at > get_asserted_phases -pin ru_9a_1617(16) -at >
get_asserted_phases -pin ru_9a_1617(17) -at > get_asserted_phases -pin
eu_iu_srlz_op_encode(0) -at > get_asserted_phases -pin eu_iu_srlz_op_encode(1) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(2) -at > get_asserted_phases -pin
eu_iu_srlz_op_encode(3) -at > get_asserted_phases -pin eu_iu_srlz_op_encode(4) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(5) -at > get_asserted_phases -pin
eu_iu_srlz_op_encode(6) -at > get_asserted_phases -pin eu_iu_srlz_op_encode(7) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(8) -at > get_asserted_phases -pin
eu_iu_srlz_op_encode(9) -at > get_asserted_phases -pin eu_iu_srlz_op_encode(10) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(11) -at > get_asserted_phases -pin
ru_9a_4849(48) -at > get_asserted_phases -pin ru_9a_4849(49) -at >
get_asserted_phases -pin ireg_1631(22) -at > get_asserted_phases -pin ireg_1631(23) -at
> get_asserted_phases -pin ireg_1631(24) -at > get_asserted_phases -pin ireg_1631(25) -at
> get_asserted_phases -pin ireg_1631(26) -at > get_asserted_phases -pin ireg_1631(27) -at
> get_asserted_phases -pin ireg_1631(28) -at > get_asserted_phases -pin ireg_1631(29) -at
> get_asserted_phases -pin ireg_1631(30) -at > hnl::all_outputs >
get_asserted_phases -pin iu_eu_opcode_cmp -rat > get_asserted_phases -pin iu_rcvry_reset
-rat > get_asserted_phases -pin iu_reset_op_c -rat > get_asserted_phases -pin
dcd_succ_last_t1 -rat Pin: NO PHASES for dcd_succ_last_t1: > set_required -time 999
-phase C3+R -ports dcd_succ_last_t1... > set_required -time -999 -phase C3+R -ports
dcd_succ_last_t1... > get_asserted_phases -pin iu_milli_mode -rat >
> set_required -time 999 -phase C3+R -ports iu_reset_op_c... > set_required -time -999
-phase C3+R -ports iu_reset_op_c... > get_asserted_phases -pin dcd_succ_last -rat
> get_asserted_phases -pin iu_eu_op_nomatch -rat > get_asserted_phases -pin

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ds_1st_maybe -rat > get_asserted_phases -pin id_xcute_targ -rat >
get_asserted_phases -pin xc_frc_ia_to_if_t1 -rat > get_asserted_phases -pin dcd_success_tr
-rat > get_asserted_phases -pin dsucc_or_agi_n -rat > get_asserted_phases -pin
dsucc_or_agi -rat > get_asserted_phases -pin iu_slow_mode -rat >
get_asserted_phases -pin slwmd_blk_n -rat > get_asserted_phases -pin xc_frc_milli -rat
> get_asserted_phases -pin dcd_succ_first_t1 -rat > get_asserted_phases -pin iu_reset_all -rat
> get_asserted_phases -pin iu_milli_mode_t1 -rat > get_asserted_phases -pin
iu_milli_mode_t2 -rat > get_asserted_phases -pin iu_milli_mode_t3 -rat >
get_asserted_phases -pin xc_frc_milli_t1 -rat > get_asserted_phases -pin iu_exc_cond -rat
> get_asserted_phases -pin slow_mode_tr -rat > get_asserted_phases -pin iu_eu_slow_mode
-rat > get_asserted_phases -pin dcd_success -rat > get_asserted_phases -pin
iu_milli_mode_tr -rat > get_asserted_phases -pin iu_reset_if -rat >
get_asserted_phases -pin exc_cond_tr -rat > get_asserted_phases -pin dcd_succ_first -rat
> get_asserted_phases -pin execute_recovery -rat > get_asserted_phases -pin execute_xcptn
-rat > get_asserted_phases -pin xc_frc_ia_to_if -rat > get_asserted_phases -pin
iu_slow_mode_t1 -rat Pin: NO PHASES for iu_slow_mode_t1: > set_required -time 999
-phase C3+R -ports iu_slow_mode_t... > set_required -time -999 -phase C3+R -ports
iu_slow_mode... > get_asserted_phases -pin gp_tr_scan_out -rat Pin: NO PHASES for
gp_tr_scan_out: > set_required -time 999 -phase C3+R -ports gp_tr_scan_out ... >
set_required -time -999 -phase C3+R -ports gp_tr_scan_out... > get_asserted_phases -pin
iu_resetfst -rat > get_asserted_phases -pin scan_out -rat Pin: NO PHASES for scan_out:
> set_required -time 999 -phase C3+R -ports scan_out -late > set_required -time -999 -phase
C3+R -ports scan_out -early > get_asserted_phases -pin iu_eu_dcd_succ_tr -rat >
get_asserted_phases -pin idcdsuc_err -rat Pin: NO PHASES for idcdsuc_err: > set_required
-time 999 -phase C3+R -ports idcdsuc_err -late > set_required -time -999 -phase C3+R -ports
idcdsuc_err -... > get_asserted_phases -pin frc_milli -rat > get_asserted_phases -pin
iu_intrupt_info(0) -rat > get_asserted_phases -pin iu_intrupt_info(1) -rat >
get_asserted_phases -pin iu_intrupt_info(2) -rat > get_asserted_phases -pin iu_intrupt_info(3)
-rat > get_asserted_phases -pin blk_dcd_info_tr(0) -rat > get_asserted_phases -pin
blk_dcd_info_tr(1) -rat > get_asserted_phases -pin blk_dcd_info_tr(2) -rat >
get_asserted_phases -pin blk_dcd_info_tr(3) -rat > get_asserted_phases -pin
iu_srlz_op_encode(0) -rat > get_asserted_phases -pin iu_srlz_op_encode(1) -rat >
get_asserted_phases -pin iu_srlz_op_encode(2) -rat > get_asserted_phases -pin
iu_srlz_op_encode(3) -rat > get_asserted_phases -pin iu_srlz_op_encode(4) -rat >
-pin iu_srlz_op_encode(6) -rat > get_asserted_phases -pin iu_srlz_op_encode(7) -rat
> get_asserted_phases -pin iu_srlz_op_encode(8) -rat > get_asserted_phases -pin
iu_srlz_op_encode(9) -rat > get_asserted_phases -pin iu_srlz_op_encode(10) -rat >
get_asserted_phases -pin iu_srlz_op_encode(11) -rat > get_asserted_phases -pin
decode_ilc(0) -rat > get_asserted_phases -pin decode_ilc(1) -rat >
get_asserted_phases -pin srlz_actn_tr(0) -rat > get_asserted_phases -pin srlz_actn_tr(1) -rat
> get_asserted_phases -pin intrpt_info_tr(0) -rat > get_asserted_phases -pin intrpt_info_tr(1)
-rat > get_asserted_phases -pin intrpt_info_tr(2) -rat > get_asserted_phases -pin
intrpt_info_tr(3) -rat > get_asserted_phases -pin op_44_info_tr(0) -rat >
get_asserted_phases -pin op_44_info_tr(1) -rat > get_asserted_phases -pin dcd_c_cnt(0) -rat
> get_asserted_phases -pin dcd_c_cnt(1) -rat > read_dcadj_file -file
/afs/apd/func/vlsi/alliance00/bssc... [ET-0018]:>Begin...ETE DCADJ reader for file
/afs/apd/func/vlsi/alliance00/bssc8/v5/ndr/a00.dcadj. [ET-0019]:<End.....ETE DCADJ reader.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/main.tcl >
hnl_idesign_get_name __CiType_13_30da5570 > use_pseudo_reg -idesign
__CiType_13_30da5570 [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3,
analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis

```

[illegible]

[illegible]

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buffers Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/optz.tcl >
freeze_net_loads -set -limit [TIMER-6412]: Asserted load on 369 inet(s). > ps Design
/HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
801 cells (516 AND; 5 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses
1022 nets (0 multiply-driven; 0 undriven) 2770 pins (623 inversions) 2.71 pins per
net 1675 literals 19 levels 10 max fanin 22 max fanout > ps Design
pcells 122 IN ports 73 OUT ports 713 cells (433 AND; 0 XOR; 0 SEQ; 0 TRI; 280
LINKED; 0 UNLINKED; 0 DC) 0 buses 934 nets (0 multiply-driven; 0 undriven)
2604 pins (608 inversions) 2.79 pins per net 1597 literals 16 levels 10 max fanin
42 max fanout Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/custom_report.tcl
> echo {Custom Synzilla Report} Custom Synzilla Report > ps -cell Design
/HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
713 cells (433 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses
934 nets (0 multiply-driven; 0 undriven) 2604 pins (608 inversions) 2.79 pins per
net 1597 literals 16 levels 10 max fanin 42 max fanout Cell
Information FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)
PSEUDO_REG (ncount 83 : area 0) cb_clk_32_1 (ncount 6 : area
480) cb_mode_block (ncount 1 : area 70)
cs_invv01c_sl (ncount 10 : area 20) Total Area = 570 (Comb = 20 :
Non-Comb = 550) > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:52:02 1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.
Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName
-----
----- 1 drain_blk.reg_n.lat_0/BASE_REG/a F C3+R 2468 -1147 0
27 1 cl_invvn 05d cl_invv05d 39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160 60 238 14 cl_invvn 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 2468 -1147 0 27 1 AND
/DELAY_ELEMENT/IN1 R C3+R 2516 -1147 0 21 1 AND AND -48
a ----> drain_blk.reg_n.lat_0/a R C3+R 2516 -1147 0 21 1 PSEUDO_REG
PSEUDO_REG 0 a ----> C89/OUT R C3+R 2516 -1147 0 21
1 AND AND 0 N89 ----> C89/IN1 F C3+R 2463
-1147 0 21 1 AND AND 52 drain_blk_in ---->{a}
M#2.EXPRESSION#104EXPR0/OUT F C3+R 2463 -1147 0 21 1 AND
AND 0 drain_blk_in ----> M#2.EXPRESSION#104EXPR0/IN1 F C3+R 2307
-1147 0 21 1 AND AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT

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F C3+R 2307 -1147 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 F C3+R 2046 -1147 0 21 1 AND
AND 261 drain_cond(8) ---->{c} M#2.EXPRESSION#103EXPR0/OUT F C3+R 2046
-1147 0 21 1 AND AND 0 drain_cond(8) ---->
M#2.EXPRESSION#103EXPR0/IN2 R C3+R 1941 -1147 0 37 2 AND
AND 104 stores_in_l2 ---->{d} M#2.EXPRESSION#94EXPR0/OUT R C3+R 1941
-1147 0 37 2 AND AND 0 stores_in_l2 ---->
M#2.EXPRESSION#94EXPR0/IN3 R C3+R 1784 -1147 0 53 3 AND
AND 157 NET994 ---->{e} M#2.EXPRESSION#92EXPR2/OUT R C3+R 1784
-1147 0 53 3 AND AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2
F C3+R 1680 -1147 0 1222 7 AND AND 104 dcd_success ---->{f}
M#2.EXPRESSION#131EXPR0/OUT F C3+R 1680 -1147 0 1222 7 AND
AND 0 dcd_success ----> M#2.EXPRESSION#131EXPR0/IN1 F C3+R 1471
-1147 0 37 2 AND AND 209 slow_blks_s ---->{g}
M#2.EXPRESSION#124EXPR0/OUT F C3+R 1471 -1147 0 37 2 AND
AND 0 slow_blks_s ----> M#2.EXPRESSION#124EXPR0/IN1 R C3+R 1367
-1147 0 21 1 AND AND 104 NET749 ---->{h}
M#2.EXPRESSION#124EXPR1/OUT R C3+R 1367 -1147 0 21 1 AND
AND 0 NET749 ----> M#2.EXPRESSION#124EXPR1/IN1 F C3+R 1262 -1147
0 21 1 AND AND 104 NET750 ---->{i} M#2.EXPRESSION#124EXPR2/OUT
F C3+R 1262 -1147 0 21 1 AND AND 0 NET750 ---->
M#2.EXPRESSION#124EXPR2/IN1 F C3+R 1105 -1147 0 37 2 AND
AND 157 medium_blks ---->{j} M#2.EXPRESSION#122EXPR0/OUT F C3+R 1105
-1147 0 37 2 AND AND 0 medium_blks ---->
M#2.EXPRESSION#122EXPR0/IN1 F C3+R 949 -1147 0 37 2 AND
AND 157 quick_blks ---->{k} M#2.EXPRESSION#121EXPR0/OUT F C3+R 949
-1147 0 37 2 AND AND 0 quick_blks ---->
M#2.EXPRESSION#121EXPR0/IN2 R C3+R 792 -1147 0 37 2 AND
2 -1147 0 37 2 AND AND 0 insn_blk_dcd ---->
M#2.EXPRESSION#82EXPR0/IN2 R C3+R 687 -1147 0 21 1 AND
AND 104 NET689 ---->{m} M#2.EXPRESSION#82EXPR1/OUT R C3+R 687
-1147 0 21 1 AND AND 0 NET689 ----> M#2.EXPRESSION#82EXPR1/IN1
R C3+R 583 -1147 110 31 2 AND AND 104 three_branches ---->
three_branches R C3+R 583 -1147 110 31 2 PI
0 three_branches

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----- 2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2477 -1105 0
27 1 cl_invvn 05d cl_invvn05d -12 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160 60 238 14 cl_invvn 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT R C3+R 2477 -1105 0 27 1 AND
AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 F C3+R 2531 -1105
0 21 1 AND AND -54 a ----> drain_blk.reg_n.lat_0/a F C3+R
2531 -1105 0 21 1 PSEUDO_REG PSEUDO_REG 0 a ----> C89/OUT
F C3+R 2531 -1105 0 21 1 AND AND 0 N89 ----> C89/IN1
R C3+R 2478 -1105 0 21 1 AND AND 52 drain_blk_in ---->{a}
M#2.EXPRESSION#104EXPR0/OUT R C3+R 2478 -1105 0 21 1 AND
AND 0 drain_blk_in ----> M#2.EXPRESSION#104EXPR0/IN1 R C3+R 2322
-1105 0 21 1 AND AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
R C3+R 2322 -1105 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 R C3+R 2061 -1105 0 21 1 AND
AND 261 drain_cond(8) ---->{c} M#2.EXPRESSION#103EXPR0/OUT R C3+R
2061 -1105 0 21 1 AND AND 0 drain_cond(8) ---->
M#2.EXPRESSION#103EXPR0/IN2 F C3+R 1956 -1105 0 37 2 AND
AND 104 stores_in_l2 ---->{d} M#2.EXPRESSION#94EXPR0/OUT F C3+R 1956
-1105 0 37 2 AND AND 0 stores_in_l2 ---->

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M#2.EXPRESSION#94EXPR0/IN3          F C3+R 1799 -1105 0 53 3 AND
AND 157 NET994 ---->{e} M#2.EXPRESSION#92EXPR2/OUT          F C3+R 1799
-1105 0 53 3 AND          AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2
R C3+R 1695 -1105 0 1222 7 AND          AND 104 dcd_success ---->{f}
M#2.EXPRESSION#131EXPR0/OUT          R C3+R 1695 -1105 0 1222 7 AND
AND 0 dcd_success ----> M#2.EXPRESSION#131EXPR0/IN1          R C3+R 1486
-1105 0 37 2 AND          AND 209 slow_blks_s ---->{g}
M#2.EXPRESSION#124EXPR0/OUT          R C3+R 1486 -1105 0 37 2 AND
AND 0 slow_blks_s ----> M#2.EXPRESSION#124EXPR0/IN1          F C3+R 1382
          AND 104 NET749 ---->{h} M#2.EXPRESSION#124EXPR1/OUT          F
C3+R 1382 -1105 0 21 1 AND          AND 0 NET749 ---->
M#2.EXPRESSION#124EXPR1/IN1          R C3+R 1277 -1105 0 21 1 AND
AND 104 NET750 ---->{i} M#2.EXPRESSION#124EXPR2/OUT          R C3+R 1277
-1105 0 21 1 AND          AND 0 NET750 ---->
M#2.EXPRESSION#124EXPR2/IN1          R C3+R 1120 -1105 0 37 2 AND
AND 157 medium_blks ---->{j} M#2.EXPRESSION#122EXPR0/OUT          R C3+R 1120
-1105 0 37 2 AND          AND 0 medium_blks ---->
M#2.EXPRESSION#122EXPR0/IN1          R C3+R 964 -1105 0 37 2 AND
AND 157 quick_blks ---->{k} M#2.EXPRESSION#121EXPR0/OUT          R C3+R 964
-1105 0 37 2 AND          AND 0 quick_blks ---->
M#2.EXPRESSION#121EXPR0/IN2          F C3+R 807 -1105 0 37 2 AND
AND 157 insn_blk_dcd ---->{l} M#2.EXPRESSION#82EXPR0/OUT          F C3+R 807
-1105 0 37 2 AND          AND 0 insn_blk_dcd ---->
M#2.EXPRESSION#82EXPR0/IN2          F C3+R 702 -1105 0 21 1 AND
AND 104 NET689 ---->{m} M#2.EXPRESSION#82EXPR1/OUT          F C3+R 702
-1105 0 21 1 AND          AND 0 NET689 ----> M#2.EXPRESSION#82EXPR1/IN1
F C3+R 598 -1105 81 31 2 AND          AND 104 three_branches ---->
three_branches          F C3+R 598 -1105 81 31 2 PI          0
three_branches

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-----
> report_area [ET-0413]:Using default pin capacitance 0.200000 for
boundary output pin iu_reset_op_c_t1. [ET-0027]:No subsequent messages of this type will be reported.
Increase timing debug level for complete set of these messages. [load_update]: Number of pin load
calculations: 83 since last stats [load_update]: Number of pin weight calculations: 0 since last stats
Design: /IDCDSUC - Area: 2731.154785, Area(Weight): 561.845093          > cputime Used 0.00
cpu seconds or 00:00:00 wall time, used 0 bytes or 0 byte.          > pmove -cost 3 -dup -trace 0
> bmove -cost 4 -dup -trace 0          > merge -cost 1 -dup -trace 0          > pmove
-cost 0 -dup -trace 0          > merge -cost 0 -dup -trace 0          > decomp -nand -ddi
-dfi -no_xor Performing Circuit Decomposition for design IDCDSUC ... Performing NAND decomposition
... .. Finished performing NAND decomposition NAND CPU time: 0.23 secs. NAND memory usage:
266240 bytes Performing DDI decomposition ... .. Finished performing DDI decomposition DDI CPU
time: 0.20 secs. DDI memory usage: 0 bytes Performing DFI decomposition ... .. Finished performing
DFI decomposition DFI CPU time: 0.07 secs. DFI memory usage: 0 bytes ...Finished Performing Circuit
Decomposition for design IDCDSUC Decomposition CPU time: 0.50 secs. Decomposition memory usage:
266240 bytes          > merge -cost 0 -dup -trace 10 Merging Cella
M#2.EXPRESSION#17EXPR0, Cellb C371, Cellc M#2.EXPRESSION#153EXPR1 Merging Cella
M#2.OR_VECT#2, Cellb C226, Cellc M#2.EXPRESSION#49EXPR1 Merging Cella
M#2.EXPRESSION#62EXPR4, Cellb C778, Cellc M#2.EXPRESSION#62EXPR3 Merging Cella
ella M#2.EXPRESSION#6EXPR0, Cellb C336, Cellc M#2.EXPRESSION#18EXPR1 Merging Cella
M#2.EXPRESSION#9EXPR0, Cellb C341, Cellc M#2.EXPRESSION#18EXPR2 Merging Cella
M#2.EXPRESSION#12EXPR0, Cellb C354, Cellc M#2.EXPRESSION#18EXPR3 Merging Cella
M#2.EXPRESSION#15EXPR0, Cellb C366, Cellc M#2.EXPRESSION#18EXPR4 Merging Cella
M#2.EXPRESSION#5EXPR0, Cellb C331, Cellc M#2.EXPRESSION#17EXPR1 Merging Cella
M#2.EXPRESSION#8EXPR0, Cellb C340, Cellc M#2.EXPRESSION#17EXPR2 Merging Cella
M#2.EXPRESSION#11EXPR0, Cellb C353, Cellc M#2.EXPRESSION#17EXPR3 Merging Cella

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M#2.EXPRESSION#14EXPR0, Cellb C364, Cellc M#2.EXPRESSION#17EXPR4 Merging Cella
M#2.EXPRESSION#114EXPR0, Cellb C498, Cellc M#2.EXPRESSION#124EXPR0 Merging Cella
M#2.EXPRESSION#90EXPR1, Cellb C713, Cellc M#2.EXPRESSION#90EXPR0 Merging Cella
M#2.EXPRESSION#125EXPR0, Cellb C432, Cellc M#2.EXPRESSION#134EXPR2 Merging Cella
M#2.EXPRESSION#123EXPR0, Cellb C415, Cellc M#2.EXPRESSION#125EXPR0 Merging Cella
M#2.EXPRESSION#126EXPR0, Cellb C438, Cellc M#2.EXPRESSION#132EXPR0 Merging Cella
M#2.EXPRESSION#107EXPR0, Cellb C705, Cellc M#2.EXPRESSION#108EXPR0 Merging Cella
M#2.EXPRESSION#88EXPR1, Cellb C339, Cellc M#2.EXPRESSION#88EXPR0 There were a total of 19
merge moves performed > fx_opt -s Number of connections before fx_opt: 1727
Number of connections after fx_opt: 1540 > tgfs_redund -effort 100 -max_iteration 3
> pmove -cost 3 -dup -trace 0 > bmove -cost 4 -dup -trace 0 > merge
-cost 1 -dup -trace 0 > pmove -cost 0 -dup -trace 0 > merge -cost 0 -dup
-trace 0 > decomp -nand -ddi -dfi -no_xor Performing Circuit Decomposition for design
IDCDSUC ... Performing NAND decomposition ... Finished performing NAND decomposition NAND
CPU time: 0.08 secs. NAND memory usage: 0 bytes Performing DDI decomposition ... Finished
performing DDI decomposition DDI CPU time: 0.00 secs. DDI memory usage: 0 bytes Performing DFI
decomposition ... Finished performing DFI decomposition DFI CPU time: 0.05 secs. DFI memory
usage: 0 bytes ... Finished Performing Circuit Decomposition for design IDCDSUC Decomposition CPU
time: 0.13 secs. Decomposition memory usage: 0 bytes > merge -cost 0 -dup -trace 10
Merging Cella C1114, Cellb C1175, Cellc M#2.EXPRESSION#77EXPR1 Merging Cella C1132, Cellb
C1190, Cellc M#2.EXPRESSION#85EXPR3 Merging Cella M#2.EXPRESSION#147EXPR2, Cellb C225,
Cellc C899 Merging Cella C1120, Cellb C1214, Cellc M#2.EXPRESSION#111EXPR7 Merging Cella
C1045, Cellb C1170, Cellc M#2.EXPRESSION#155EXPR1 Merging Cella
M#2.EXPRESSION#92EXPR0, Cellb C1283, Cellc M#2.EXPRESSION#169EXPR1 Merging Cella
M#2.EXPRESSION#94EXPR0, Cellb C1284, Cellc M#2.EXPRESSION#169EXPR2 Merging Cella
C1047, Cellb C1192, Cellc M#2.EXPRESSION#170EXPR0 Merging Cella C1126, Cellb C1230, Cellc
M#2.EXPRESSION#141EXPR1 Merging Cella C1155, Cellb C1356, Cellc M#2.EXPRESSION#6EXPR0
Merging Cella C1156, Cellb C1358, Cellc M#2.EXPRESSION#9EXPR0 Merging Cella C1157, Cellb
C1360, Cellc M#2.EXPRESSION#12EXPR0 Merging Cella C1158, Cellb C1362, Cellc
M#2.EXPRESSION#15EXPR0 Merging Cella C934, Cellb C1335, Cellc C1075 There were a total of 14
merge moves performed > fx_opt -s Number of connections before fx_opt: 1524
Number of connections after fx_opt: 1508 > tgfs_redund -effort 100 -max_iteration 3
> ps Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses
966 nets (0 multiply-driven; 0 undriven) 2547 pins (465 inversions) 2.64 pins per
net 1508 literals 21 levels 10 max fanin 19 max fanout >
tgfs_redund -effort 100 -max_iteration 3 > echo {Custom Synzilla Report} Custom Synzilla
22 IN ports 73 OUT ports 745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0
UNLINKED; 0 DC) 0 buses 966 nets (0 multiply-driven; 0 undriven) 2547 pins
(465 inversions) 2.64 pins per net 1508 literals 21 levels 10 max fanin
19 max fanout Cell Information FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area 0) PSEUDO_REG (ncount 83 : area 0)
cb_clk_32_1 (ncount 6 : area 480) cb_mode_block (ncount 1 : area
70) cs_invvn01c_sl (ncount 10 : area 20) Total Area =
570 (Comb = 20 : Non-Comb = 550) > write_end_point_report -points 2
[ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:52:17 1999 Part : IDCDSUC Mode : Late
Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SskCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AsstRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK

```

GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
 CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
 (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
 (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
 EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
 SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
 ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
 ATLimit Slack discontinuity due to failed test Num/
 LimitedAT/ Delay/ Failed Test/ Test PinName
 E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```

-----
1 drain_blk.reg_n.lat_0/BASE_REG/a F C3+R 2849 -1528 0
27 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160 60 238 14 cl_invvn 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 2849 -1528 0 27 1 AND
AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 2897 -1528
0 21 1 AND AND -48 a ----> drain_blk.reg_n.lat_0/a R C3+R
2897 -1528 0 21 1 PSEUDO_REG PSEUDO_REG 0 a ---->{a}
M#2.EXPRESSION#104EXPR0/OUT R C3+R 2897 -1528 0 21 1 AND
AND 0 N687 ----> M#2.EXPRESSION#104EXPR0/IN1 F C3+R 2740 -1528
21 1 AND AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
F C3+R 2740 -1528 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 R C3+R 2479 -1528 0 21 1 AND
AND 261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT R C3+R 2479 -1528
0 21 1 AND AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
F C3+R 2374 -1528 0 37 2 AND AND 104 N1393 ---->{d} C1398/OUT
F C3+R 2374 -1528 0 37 2 AND AND 0 N1393 ----> C1398/IN2
R C3+R 2270 -1528 0 53 3 AND AND 104 N927 ----> C1297/OUT
R C3+R 2270 -1528 0 53 3 AND AND 0 N927 ----> C1297/IN1
F C3+R 2218 -1528 0 21 1 AND AND 52 N1292
---->{e} C932/OUT F C3+R 2218 -1528 0 21 1 AND
AND 0 N1292 ----> C932/IN1 R C3+R 2113 -1528 0 21 1
AND AND 104 NET994 ---->{f} M#2.EXPRESSION#92EXPR2/OUT R
C3+R 2113 -1528 0 21 1 AND AND 0 NET994 ---->
M#2.EXPRESSION#92EXPR2/IN2 F C3+R 2009 -1528 0 1190 5 AND
AND 104 N1098 ---->{g} C1103/OUT F C3+R 2009 -1528 0 1190
5 AND AND 0 N1098 ----> C1103/IN1 R C3+R 1904
-1528 0 21 1 AND AND 104 N1097 ---->{h} C1102/OUT
R C3+R 1904 -1528 0 21 1 AND AND 0 N1097 ----> C1102/IN14
F C3+R 1800 -1528 0 21 1 AND AND 104 N1480 ----> C1485/OUT
F C3+R 1800 -1528 0 21 1 AND AND 0 N1480 ----> C1485/IN1
R C3+R 1747 -1528 0 37 2 AND AND 52 N1479 ---->{i} C1484/OUT
R C3+R 1747 -1528 0 37 2 AND AND 0 N1479 ----> C1484/IN5
F C3+R 1591 -1528 0 37 2 AND AND 157 N1498 ----> C1503/OUT
F C3+R 1591 -1528 0 37 2 AND AND 0 N1498 ----> C1503/IN1
R C3+R 1539 -1528 0 21 1 AND AND 52 N1497 ---->{j} C1502/OUT
R C3+R 1539 -1528 0 21 1 AND AND 0 N1497 ----> C1502/IN10
F C3+R 1330 -1528 0 37 2 AND AND 209 N1502 ----> C1507/OUT
F C3+R 1330 -1528 0 37 2 AND AND 0 N1502 ----> C1507/IN1
R C3+R 1277 -1528 0 21 1 AND AND 52 N1501 ---->{k} C1506/OUT
0 21 1 AND AND 0 N1501 ----> C1506/IN2 F
C3+R 1068 -1528 0 21 1 AND AND 209 N1002 ---->{l} C1007/OUT
F C3+R 1068 -1528 0 21 1 AND AND 0 N1002 ----> C1007/IN1

```

```

R C3+R 912 -1528 0 21 1 AND AND 157 N1001 ---->{m} C1006/OUT
R C3+R 912 -1528 0 21 1 AND AND 0 N1001 ----> C1006/IN1
F C3+R 807 -1528 0 21 1 AND AND 104 N1314 ----> C1319/OUT
F C3+R 807 -1528 0 21 1 AND AND 0 N1314 ----> C1319/IN1
R C3+R 755 -1528 80 16 1 AND AND 52 op_dsbl_before ---->
op_dsbl_before R C3+R 755 -1528 80 16 1 PI 0
op_dsbl_before

```

```

-----
2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2816 -1444 0
27 1 cl_invvn 05d cl_invvn05d -12 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3+R 160 60 238 14 cl_invvn 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT R C3+R 2816 -1444 0 27 1 AND
AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 F C3+R 2870 -1444
0 21 1 AND AND -54 a ----> drain_blk.reg_n.lat_0/a F C3+R
2870 -1444 0 21 1 PSEUDO_REG PSEUDO_REG 0 a ---->{a}
M#2.EXPRESSION#104EXPR0/OUT F C3+R 2870 -1444 0 21 1 AND
AND 0 N687 ----> M#2.EXPRESSION#104EXPR0/IN1 R C3+R 2713 -1444
0 21 1 AND AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
R C3+R 2713 -1444 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 F C3+R 2452 -1444 0 21 1 AND
AND 261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT F C3+R 2452 -1444
0 21 1 AND AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
R C3+R 2347 -1444 0 37 2 AND AND 104 N1393 ---->{d} C1398/OUT
R C3+R 2347 -1444 0 37 2 AND AND 0 N1393 ----> C1398/IN2
F C3+R 2243 -1444 0 53 3 AND AND 104 N927 ----> C1297/OUT
F C3+R 2243 -1444 0 53 3 AND AND 0 N927 ----> C1297/IN1
R C3+R 2191 -1444 0 21 1 AND AND 52 N1292 ---->{e} C932/OUT
R C3+R 2191 -1444 0 21 1 AND AND 0 N1292 ----> C932/IN1
F C3+R 2086 -1444 0 21 1 AND AND 104 NET994 ---->{f}
F C3+R 2086 -1444 0 21 1 AND AND 0 NET994 ---->
M#2.EXPRESSION#92EXPR2/IN2 R C3+R 1982 -1444 0 1190 5 AND
AND 104 N1098 ---->{g} C1103/OUT R C3+R 1982 -1444 0 1190
5 AND AND 0 N1098 ----> C1103/IN1 F C3+R 1877
-1444 0 21 1 AND AND 104 N1097 ---->{h} C1102/OUT
F C3+R 1877 -1444 0 21 1 AND AND 0 N1097 ----> C1102/IN14
R C3+R 1773 -1444 0 21 1 AND AND 104 N1480 ----> C1485/OUT
R C3+R 1773 -1444 0 21 1 AND AND 0 N1480 ----> C1485/IN1
F C3+R 1720 -1444 0 37 2 AND AND 52 N1479 ---->{i} C1484/OUT
F C3+R 1720 -1444 0 37 2 AND AND 0 N1479 ----> C1484/IN5
R C3+R 1564 -1444 0 37 2 AND AND 157 N1498 ----> C1503/OUT
R C3+R 1564 -1444 0 37 2 AND AND 0 N1498 ----> C1503/IN1
F C3+R 1512 -1444 0 21 1 AND AND 52 N1497 ---->{j} C1502/OUT
F C3+R 1512 -1444 0 21 1 AND AND 0 N1497 ----> C1502/IN10
R C3+R 1303 -1444 0 37 2 AND AND 209 N1502 ----> C1507/OUT
R C3+R 1303 -1444 0 37 2 AND AND 0 N1502 ----> C1507/IN1
F C3+R 1250 -1444 0 21 1 AND AND 52 N1501 ---->{k} C1506/OUT
F C3+R 1250 -1444 0 21 1 AND AND 0 N1501 ----> C1506/IN2
R C3+R 1041 -1444 0 21 1 AND AND 209 N1002 ---->{l} C1007/OUT
R C3+R 1041 -1444 0 21 1 AND AND 0 N1002 ----> C1007/IN1
F C3+R 885 -1444 0 21 1 AND AND 157 N1001 ---->{m} C1006/OUT
F C3+R 885 -1444 0 21 1 AND AND 0 N1001 ----> C1006/IN1
R C3+R 780 -1444 0 21 1 AND AND 104 N1314 ----> C1319/OUT
R C3+R 780 -1444 0 21 1 AND AND 0 N1314 ----> C1319/IN1
F C3+R 728 -1444 80 16 1 AND AND 52 op_dsbl_before ---->
op_dsbl_before F C3+R 728 -1444 80 16 1 PI 0

```

op_dsbl_before

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-----
> report_area Design: /IDCDSUC - Area: 2731.154785, Area(Weight):
0:15 wall time, used 1376256 bytes or 1 meg. > ps Design /HISVHDL/IDCDSUC has: 1
instances 0 upcells 122 IN ports 73 OUT ports 745 cells (465 AND; 0 XOR; 0 SEQ; 0
TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses 966 nets (0 multiply-driven; 0 undriven)
2547 pins (465 inversions) 2.64 pins per net 1508 literals 21 levels 10 max fanin
19 max fanout > echo {Custom Synzilla Report} Custom Synzilla Report > ps
-cell Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses
966 nets (0 multiply-driven; 0 undriven) 2547 pins (465 inversions) 2.64 pins per
net 1508 literals 21 levels 10 max fanin 19 max fanout Cell
Information FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)
PSEUDO_REG (ncount 83 : area 0) cb_clk_32_1 (ncount 6 : area
480) cb_mode_block (ncount 1 : area 70)
cs_invv01c_sl (ncount 10 : area 20) Total Area = 570 (Comb = 20 :
Non-Comb = 550) > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:52:18 1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.
Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName
-----
----- 1 drain_blk.reg_n.lat_0/BASE_REG/a F C3+R 2849 -1528 0
27 1 cl_invv01 05d cl_invv05d 39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160 60 238 14 cl_invv01 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 2849 -1528 0 27 1 AND
drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 2897 -1528 0 21 1 AND
AND -48 a ----> drain_blk.reg_n.lat_0/a R C3+R 2897 -1528 0 21 1
PSEUDO_REG PSEUDO_REG 0 a ---->{a} M#2.EXPRESSION#104EXPR0/OUT
R C3+R 2897 -1528 0 21 1 AND AND 0 N687 ---->
M#2.EXPRESSION#104EXPR0/IN1 F C3+R 2740 -1528 0 21 1 AND
AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT F C3+R 2740 -1528
0 21 1 AND AND 0 NET667 ----> M#2.OR_VECT#3/IN9 R
C3+R 2479 -1528 0 21 1 AND AND 261 N685 ---->{c}
M#2.EXPRESSION#103EXPR0/OUT R C3+R 2479 -1528 0 21 1 AND
AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2 F C3+R 2374 -1528
0 37 2 AND AND 104 N1393 ---->{d} C1398/OUT F
```

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C3+R 2374 -1528 0 37 2 AND AND 0 N1393 ----> C1398/IN2
R C3+R 2270 -1528 0 53 3 AND AND 104 N927 ----> C1297/OUT
R C3+R 2270 -1528 0 53 3 AND AND 0 N927 ----> C1297/IN1
F C3+R 2218 -1528 0 21 1 AND AND 52 N1292
---->{e} C932/OUT F C3+R 2218 -1528 0 21 1 AND
AND 0 N1292 ----> C932/IN1 R C3+R 2113 -1528 0 21 1
AND AND 104 NET994 ---->{f} M#2.EXPRESSION#92EXPR2/OUT R
C3+R 2113 -1528 0 21 1 AND AND 0 NET994 ---->
M#2.EXPRESSION#92EXPR2/IN2 F C3+R 2009 -1528 0 1190 5 AND
AND 104 N1098 ---->{g} C1103/OUT F C3+R 2009 -1528 0 1190
5 AND AND 0 N1098 ----> C1103/IN1 R C3+R 1904
-1528 0 21 1 AND AND 104 N1097 ---->{h} C1102/OUT
R C3+R 1904 -1528 0 21 1 AND AND 0 N1097 ----> C1102/IN14
F C3+R 1800 -1528 0 21 1 AND AND 104 N1480 ----> C1485/OUT
F C3+R 1800 -1528 0 21 1 AND AND 0 N1480 ----> C1485/IN1
R C3+R 1747 -1528 0 37 2 AND AND 52 N1479 ---->{i} C1484/OUT
R C3+R 1747 -1528 0 37 2 AND AND 0 N1479 ----> C1484/IN5
F C3+R 1591 -1528 0 37 2 AND AND 157 N1498 ----> C1503/OUT
F C3+R 1591 -1528 0 37 2 AND AND 0 N1498 ----> C1503/IN1
R C3+R 1539 -1528 0 21 1 AND AND 52 N1497 ---->{j} C1502/OUT
-> C1502/IN10 F C3+R 1330 -1528 0 37 2 AND
AND 209 N1502 ----> C1507/OUT F C3+R 1330 -1528 0 37 2
AND AND 0 N1502 ----> C1507/IN1 R C3+R 1277
-1528 0 21 1 AND AND 52 N1501 ---->{k} C1506/OUT
R C3+R 1277 -1528 0 21 1 AND AND 0 N1501 ----> C1506/IN2
F C3+R 1068 -1528 0 21 1 AND AND 209 N1002 ---->{l} C1007/OUT
F C3+R 1068 -1528 0 21 1 AND AND 0 N1002 ----> C1007/IN1
R C3+R 912 -1528 0 21 1 AND AND 157 N1001 ---->{m} C1006/OUT
R C3+R 912 -1528 0 21 1 AND AND 0 N1001 ----> C1006/IN1
F C3+R 807 -1528 0 21 1 AND AND 104 N1314 ----> C1319/OUT
F C3+R 807 -1528 0 21 1 AND AND 0 N1314 ----> C1319/IN1
R C3+R 755 -1528 80 16 1 AND AND 52 op_dsbl_before ---->
op_dsbl_before R C3+R 755 -1528 80 16 1 PI 0
op_dsbl_before

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----- 2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2816 -1444 0
27 1 cl_invvn 05d cl_invvn05d -12 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160 60 238 14 cl_invvn 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT R C3+R 2816 -1444 0 27 1 AND
AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 F C3+R 2870 -1444
0 21 1 AND AND -54 a ----> drain_blk.reg_n.lat_0/a F C3+R
2870 -1444 0 21 1 PSEUDO_REG PSEUDO_REG 0 a ---->{a}
M#2.EXPRESSION#104EXPR0/OUT F C3+R 2870 -1444 0 21 1 AND
AND 0 N687 ----> M#2.EXPRESSION#104EXPR0/IN1 R C3+R 2713 -1444
0 21 1 AND AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
R C3+R 2713 -1444 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 F C3+R 2452 -1444 0 21 1 AND
AND 261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT F C3+R 2452 -1444
0 21 1 AND AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
R C3+R 2347 -1444 0 37 2 AND AND 104 N1393 ---->{d} C1398/OUT
R C3+R 2347 -1444 0 37 2 AND AND 0 N1393 ----> C1398/IN2
F C3+R 2243 -1444 0 53 3 AND AND 104 N927 ----> C1297/OUT
AND 0 N927 ----> C1297/IN1 R C3+R 2191 -1444 0
21 1 AND AND 52 N1292 ---->{e} C932/OUT R C3+R
2191 -1444 0 21 1 AND AND 0 N1292 ----> C932/IN1

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F C3+R 2086 -1444 0 21 1 AND AND 104 NET994 ---->{f}
M#2.EXPRESSION#92EXPR2/OUT F C3+R 2086 -1444 0 21 1 AND
AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2 R C3+R 1982 -1444
0 1190 5 AND AND 104 N1098 ---->{g} C1103/OUT R
C3+R 1982 -1444 0 1190 5 AND AND 0 N1098 ----> C1103/IN1
F C3+R 1877 -1444 0 21 1 AND AND 104 N1097 ---->{h} C1102/OUT
F C3+R 1877 -1444 0 21 1 AND AND 0 N1097 ----> C1102/IN14
R C3+R 1773 -1444 0 21 1 AND AND 104 N1480 ----> C1485/OUT
R C3+R 1773 -1444 0 21 1 AND AND 0 N1480 ----> C1485/IN1
F C3+R 1720 -1444 0 37 2 AND AND 52 N1479 ---->{i} C1484/OUT
F C3+R 1720 -1444 0 37 2 AND AND 0 N1479 ----> C1484/IN5
R C3+R 1564 -1444 0 37 2 AND AND 157 N1498 ----> C1503/OUT
R C3+R 1564 -1444 0 37 2 AND AND 0 N1498 ----> C1503/IN1
F C3+R 1512 -1444 0 21 1 AND AND 52 N1497 ---->{j} C1502/OUT
F C3+R 1512 -1444 0 21 1 AND AND 0 N1497 ----> C1502/IN10
R C3+R 1303 -1444 0 37 2 AND AND 209 N1502 ----> C1507/OUT
R C3+R 1303 -1444 0 37 2 AND AND 0 N1502 ----> C1507/IN1
F C3+R 1250 -1444 0 21 1 AND AND 52 N1501 ---->{k} C1506/OUT
F C3+R 1250 -1444 0 21 1 AND AND 0 N1501 ----> C1506/IN2
R C3+R 1041 -1444 0 21 1 AND AND 209 N1002 ---->{l} C1007/OUT
R C3+R 1041 -1444 0 21 1 AND AND 0 N1002 ----> C1007/IN1
F C3+R 885 -1444 0 21 1 AND AND 157 N1001 ---->{m} C1006/OUT
F C3+R 885 -1444 0 21 1 AND AND 0 N1001 ----> C1006/IN1
R C3+R 780 -1444 0 21 1 AND AND 104 N1314 ----> C1319/OUT
R C3+R 780 -1444 0 21 1 AND AND 0 N1314 ----> C1319/IN1
AND 52 op_dsbl_before ----> op_dsbl_before F C3+R
728 -1444 80 16 1 PI 0 op_dsbl_before

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-----
> report_area Design: /IDCDSUC - Area: 2731.154785, Area(Weight):
561.845093 > cputime Used 1.04 cpu seconds or 00:00:01 wall time, used 0 bytes or 0 byte.
> ps Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses
966 nets (0 multiply-driven; 0 undriven) 2547 pins (465 inversions) 2.64 pins per
net 1508 literals 21 levels 10 max fanin 19 max fanout > ps Design
/HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
648 cells (368 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC) 0 buses
869 nets (0 multiply-driven; 0 undriven) 2353 pins (553 inversions) 2.71 pins per
net 1411 literals 14 levels 10 max fanin 20 max fanout > decomp
-nand -ddi -dfi -no_xor Performing Circuit Decomposition for design IDCDSUC ... Performing NAND
decomposition ... Finished performing NAND decomposition NAND CPU time: 0.08 secs. NAND
memory usage: 0 bytes Performing DDI decomposition ... Finished performing DDI decomposition DDI
CPU time: 0.01 secs. DDI memory usage: 0 bytes Performing DFI decomposition ... Finished
performing DFI decomposition DFI CPU time: 0.06 secs. DFI memory usage: 0 bytes ...Finished
Performing Circuit Decomposition for design IDCDSUC Decomposition CPU time: 0.15 secs.
Decomposition memory usage: 0 bytes > gf -area -t 10 Number of connections before gf:
1508 Number of connections after gf: 1505 gf CPU time: 0.63 secs. gf memory usage: 0 bytes
> decomp -nand -ddi -dfi -no_xor Performing Circuit Decomposition for design IDCDSUC ... Performing
NAND decomposition ... Finished performing NAND decomposition NAND CPU time: 0.01 secs. NAND
memory usage: 0 bytes Performing DDI decomposition ... Finished performing DDI decomposition DDI
CPU time: 0.00 secs. DDI memory usage: 0 bytes Performing DFI decomposition ... Finished
performing DFI decomposition DFI CPU time: 0.00 secs. DFI memory usage: 0 bytes ...Finished
Performing Circuit Decomposition for design IDCDSUC Decomposition CPU time: 0.01 secs.
Decomposition memory usage: 0 bytes > tgfs_redund -effort 100 -max_iteration 3
> equiv -time -trace 10 Processing on 0:20 levels Bdd Equivalence routine found 0 redundancies and 24
equivalences Processing on 21:20 levels > tgfs_redund -effort 100 -max_iteration 3

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> ps Design /HISVHDL/IDCDSUC has:          1 instances  0 upcells   122 IN ports 73 OUT ports
722 cells (442 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)          0 buses
943 nets (0 multiply-driven; 0 undriven)          2498 pins (486 inversions)          2.65 pins per
net          1482 literals 19 levels          10 max fanin          20 max fanout          > ps Design
/HISVHDL/IDCDSUC has:          1 instances  0 upcells   122 IN ports 73 OUT ports
722 cells (442 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)          0 buses
943 nets (0 multiply-driven; 0 undriven)          2498 pins (486 inversions)          2.65 pins per
net          1482 literals 19 levels          10 max fanin          20 max fanout          > tgfs_redund
-effort 100 -report_only [TGFS-800]: Out of a total of 2822 faults identified 0 redundancies: could not
decide on: 0.          > echo {=== Optimization process finished ===} === Optimization process finished
===          > echo {Custom Synzilla Report} Custom Synzilla Report          > ps -cell Design
/HISVHDL/IDCDSUC has:          1 instances  0 upcells   122 IN ports 73 OUT ports
KED; 0 DC) 0 buses          943 nets (0 multiply-driven; 0 undriven)          2498 pins (486 inversions)
2.65 pins per net          1482 literals 19 levels          10 max fanin          20 max fanout
Cell Information          FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)
PSEUDO_REG (ncount 83 : area 0)          cb_clk_32_1 (ncount 6 : area
480)          cb_mode_block (ncount 1 : area 70)
cs_invv01c_sl (ncount 10 : area 20)          Total Area = 570 (Comb = 20 :
Non-Comb = 550)          > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.          Sun Apr 18
21:52:29 1999 Part : IDCDSUC Mode : Late Mode / Nominal          EDA EinsTimer EndPoint
Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack          Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description -----
Continuation          SlkCont          Slack due to a point downstream on path          Required Arrival Time
RAT          (ARRIVAL TIME < REQUIRED ARRIVAL TIME)          Asserted Required Arrival Time AssrtRAT
(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)          Clock Gating Setup          ClkGSet          (
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST )          Clock Gating
Hold          ClkGHld          (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
+ ADJUST )          Clock Tree Pulse Width          ClkTPW          (CLOCK LEADING EDGE + PULSE WIDTH <
CLOCK TRAILING EDGE )          Setup          Setup          (DATA ARRIVAL TIME + SETUP <
CLOCK ARRIVAL TIME + ADJUST )          Hold          Hold          (DATA ARRIVAL TIME - HOLD
> CLOCK ARRIVAL TIME + ADJUST )          EndOfCycle          EndOfC          (DATA ARRIVAL TIME
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST )          ClockPulseWidth          ClkPW          (CLOCK
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE )          ClockSeparation          ClkSep
(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST )          Loop
ALTest          (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
Arrival Time Limiting          ATLimit          Slack discontinuity due to failed test          Num/
LimitedAT/          Delay/          Failed Test/          Test PinName
E Phase          AT          Slack          Slew          CL          FO          Cell          P Func          T.Adj          NetName
-----
-----          1 drain_blk.reg_n.lat_0/BASE_REG/a          F C3+R          2796          -1476          0
27 1 cl_invv01          05d cl_invv05d          39 DELAY Setup          drain_blk.reg_n.lat_0/BASE_REG/c1
F C3-          160          60          238          14 cl_invv01          05d          1200          c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT          F C3+R          2796          -1476          0          27 1 AND
AND          0 DELAY ---->          drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1          R C3+R          2844          -1476
0          21 1 AND          AND          -48 a ---->          drain_blk.reg_n.lat_0/a          R C3+R
2844          -1476          0          21 1 PSEUDO_REG          PSEUDO_REG          0 a ---->{a}
M#2.EXPRESSION#104EXPR0/OUT          R C3+R          2844          -1476          0          21 1 AND
AND          0 N687 ---->          M#2.EXPRESSION#104EXPR0/IN1          F C3+R          2688          -1476
AND          F C3+R          2688          -1476          0          21 1 AND          AND          0 NET667 ---->
M#2.OR_VECT#3/IN9          R C3+R          2427          -1476          0          21 1 AND
AND          261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT          R C3+R          2427          -1476
0          21 1 AND          AND          0 N685 ---->          M#2.EXPRESSION#103EXPR0/IN2
F C3+R          2322          -1476          0          37 2 AND          AND          104 N1393 ---->{d} C1398/OUT

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F C3+R 2322 -1476 0 37 2 AND AND 0 N1393 ----> C1398/IN2
R C3+R 2218 -1476 0 53 3 AND AND 104 N1292 ----> C1655/OUT
R C3+R 2218 -1476 0 53 3 AND AND 0 N1292 ----> C1655/IN1
F C3+R 2165 -1476 0 21 1 AND AND 52 N1650 ----> {e} C932/OUT
F C3+R 2165 -1476 0 21 1 AND AND 0 N1650 ----> C932/IN1
R C3+R 2061 -1476 0 21 1 AND AND 104 NET994 ----> {f}
M#2.EXPRESSION#92EXPR2/OUT R C3+R 2061 -1476 0 21 1 AND
AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2 F C3+R 1956 -1476
0 1190 5 AND AND 104 N1098 ----> {g} C1103/OUT F
C3+R 1956 -1476 0 1190 5 AND AND 0 N1098 ----> C1103/IN1
R C3+R 1852 -1476 0 21 1 AND AND 104 N1097 ----> {h} C1102/OUT
R C3+R 1852 -1476 0 21 1 AND AND 0 N1097 ----> C1102/IN14
F C3+R 1747 -1476 0 21 1 AND AND 104 N1692 ----> C1697/OUT
F C3+R 1747 -1476 0 21 1 AND AND 0 N1692 ----> C1697/IN1
R C3+R 1695 -1476 0 37 2 AND AND 52 N1479 ----> {i} C1484/OUT
R C3+R 1695 -1476 0 37 2 AND AND 0 N1479 ----> C1484/IN5
F C3+R 1539 -1476 0 37 2 AND AND 157 N1497 ----> C1726/OUT
F C3+R 1539 -1476 0 37 2 AND AND 0 N1497 ----> C1726/IN1
R C3+R 1486 -1476 0 21 1 AND AND 52 N1721 ----> {j} C1502/OUT
R C3+R 1486 -1476 0 21 1 AND AND 0 N1721 ----> C1502/IN10
F C3+R 1277 -1476 0 37 2 AND AND 209 N1723 ----> {k} C1506/OUT
F C3+R 1277 -1476 0 37 2 AND AND 0 N1723 ----> C1506/IN2
F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1007/OUT
R C3+R 912 -1476 0 21 1 AND AND 157 N1001
----> {m} C1006/OUT R C3+R 912 -1476 0 21 1 AND
AND 0 N1001 ----> C1006/IN1 F C3+R 807 -1476 0 21 1
AND AND 104 N1673 ----> C1678/OUT F C3+R 807
-1476 0 21 1 AND AND 0 N1673 ----> C1678/IN1
R C3+R 755 -1476 80 16 1 AND AND 52 op_dsbl_before ---->
op_dsbl_before R C3+R 755 -1476 80 16 1 PI 0
op_dsbl_before

-----
2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2764 -1392 0
27 1 cl_invvn 05d cl_invvn05d -12 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160 60 238 14 cl_invvn 05d 1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT R C3+R 2764 -1392 0 27 1 AND
AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 F C3+R 2817 -1392
0 21 1 AND AND -54 a ----> drain_blk.reg_n.lat_0/a F C3+R
2817 -1392 0 21 1 PSEUDO_REG PSEUDO_REG 0 a ----> {a}
M#2.EXPRESSION#104EXPR0/OUT F C3+R 2817 -1392 0 21 1 AND
AND 0 N687 ----> M#2.EXPRESSION#104EXPR0/IN1 R C3+R 2661 -1392
0 21 1 AND AND 157 NET667 ----> {b} M#2.OR_VECT#3/OUT
R C3+R 2661 -1392 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 F C3+R 2400 -1392 0 21 1 AND
AND 261 N685 ----> {c} M#2.EXPRESSION#103EXPR0/OUT F C3+R 2400 -1392
0 21 1 AND AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
R C3+R 2295 -1392 0 37 2 AND AND 104 N1393 ----> {d} C1398/OUT
R C3+R 2295 -1392 0 37 2 AND AND 0 N1393 ----> C1398/IN2
F C3+R 2191 -1392 0 53 3 AND AND 104 N1292 ----> C1655/OUT
F C3+R 2191 -1392 0 53 3 AND AND 0 N1292 ----> C1655/IN1
R C3+R 2138 -1392 0 21 1 AND AND 52 N1650 ----> {e} C932/OUT
R C3+R 2138 -1392 0 21 1 AND AND 0 N1650 ----> C932/IN1
F C3+R 2034 -1392 0 21 1 AND AND 104 NET994 ----> {f}
M#2.EXPRESSION#92EXPR2/OUT F C3+R 2034 -1392 0 21 1 AND
AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2 R C3+R 1929 -1392

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0 1190 5 AND          AND 104 N1098 ---->{g} C1103/OUT          R
0 N1098 ----> C1103/IN1          F C3+R 1825 -1392 0 21 1 AND
AND 104 N1097 ---->{h} C1102/OUT          F C3+R 1825 -1392 0 21
1 AND          AND 0 N1097 ----> C1102/IN14          R C3+R 1720
-1392 0 21 1 AND          AND 104 N1692 ----> C1697/OUT
R C3+R 1720 -1392 0 21 1 AND          AND 0 N1692 ----> C1697/IN1
F C3+R 1668 -1392 0 37 2 AND          AND 52 N1479 ---->{i} C1484/OUT
F C3+R 1668 -1392 0 37 2 AND          AND 0 N1479 ----> C1484/IN5
R C3+R 1512 -1392 0 37 2 AND          AND 157 N1497 ----> C1726/OUT
R C3+R 1512 -1392 0 37 2 AND          AND 0 N1497 ----> C1726/IN1
F C3+R 1459 -1392 0 21 1 AND          AND 52 N1721 ---->{j} C1502/OUT
F C3+R 1459 -1392 0 21 1 AND          AND 0 N1721 ----> C1502/IN10
R C3+R 1250 -1392 0 37 2 AND          AND 209 N1723 ---->{k} C1506/OUT
R C3+R 1250 -1392 0 37 2 AND          AND 0 N1723 ----> C1506/IN2
R C3+R 1041 -1392 0 21 1 AND          AND 209 N1002 ---->{l} C1007/OUT
R C3+R 1041 -1392 0 21 1 AND          AND 0 N1002 ----> C1007/IN1
F C3+R 885 -1392 0 21 1 AND          AND 157 N1001 ---->{m} C1006/OUT
F C3+R 885 -1392 0 21 1 AND          AND 0 N1001 ----> C1006/IN1
R C3+R 780 -1392 0 21 1 AND          AND 104 N1673 ----> C1678/OUT
R C3+R 780 -1392 0 21 1 AND          AND 0 N1673 ----> C1678/IN1
F C3+R 728 -1392 80 16 1 AND          AND 52 op_dsbl_before ---->
op_dsbl_before          F C3+R 728 -1392 80 16 1 PI          0
op_dsbl_before

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-----
> report_area Design: /IDCDSUC - Area: 2731.154785, Area(Weight):
561.845093 > cputime Used 11.00 cpu seconds or 00:00:11 wall time, used 0 bytes or 0 byte.
> echo {=== Techmap process ===} === Techmap process === Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/tmap.tcl > echo {=== Technology
mapping using wave 5 patterns 400 ===} === Technology mapping using wave 5 patterns 400 ===
> freeze_net_loads -set -limit [TIMER-6411]: Unasserted load on 369 inet(s). [TIMER-6412]: Asserted
load on 369 inet(s). > resize -trace 0 -local -mincut -inc -sequential -ana 100... Average
Inverter area (used for gain scaling) = 7.5875 resize Area : before 2731.15 after 2731.15
%) Cell : before 722 after 722 (0.00 %) Time : 0.750000 > decomp -ddi -dfi
-step2 -xor Performing Circuit Decomposition for design IDCDSUC ... Performing DDI decomposition ...
... Finished performing DDI decomposition DDI CPU time: 0.01 secs. DDI memory usage: 0 bytes
Performing DFI decomposition ... ... Finished performing DFI decomposition DFI CPU time: 0.00 secs.
DFI memory usage: 0 bytes Levelizing design ... ... Finished levelizing design Levelization CPU time:
0.03 secs. Levelization memory usage: 0 bytes Performing STEP 2 composition ... ... Finished
performing STEP 2 composition STEP 2 CPU time: 0.01 secs. STEP 2 memory usage: 0 bytes
...Finished Performing Circuit Decomposition for design IDCDSUC Decomposition CPU time: 0.05 secs.
Decomposition memory usage: 0 bytes > freeze_net_loads -reset [TIMER-6411]: Unasserted
load on 369 inet(s). > resize -trace 0 -local -mincut -inc -sequential -ana 100... resize
Area : before 2731.15 after 2731.15 (0.00 %) Slack : before -1475.6755 after -1475.6755 (0.00 %)
Cell : before 722 after 722 (0.00 %) Time : 1.520000 > freeze_net_loads -set -limit
[TIMER-6412]: Asserted load on 369 inet(s). > decomp -nand -ddi -dfi -step2 -step3 -no_xor
-timer Performing Circuit Decomposition for design IDCDSUC ... Performing NAND decomposition ...
Finished performing NAND decomposition NAND CPU time: 0.03 secs. NAND memory usage: 0 bytes
Performing DDI decomposition ... ... Finished performing DDI decomposition DDI CPU time: 0.00 secs.
DDI memory usage: 0 bytes Performing DFI decomposition ... ... Finished performing DFI decomposition
DFI CPU time: 0.02 secs. DFI memory usage: 0 bytes Levelizing design ... ... Finished levelizing design
Levelization CPU time: 0.03 secs. Levelization memory usage: 0 bytes Performing STEP 2 composition
... ... Finished performing STEP 2 composition STEP 2 CPU time: 0.01 secs. STEP 2 memory usage: 0
bytes Performing STEP 3 decomposition ... ... Finished performing STEP 3 decomposition STEP 3 CPU
time: 0.82 secs. STEP 3 memory usage: 0 bytes ...Finished Performing Circuit Decomposition for design
IDCDSUC Decomposition CPU time: 0.91 secs. Decomposition memory usage: 0 bytes >

```

[illegible]

```

0 ----> C2744/y                                F C3+R 1483 -604 71 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a                                R C3+R 1435
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675
----> C2738/b                                F C3+R 1368 -604 83 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y                                F C3+R 1368 -604 83
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
C2728/y                                R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b                                F C3+R 1251 -604 71
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1692 ----> C2725/y
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a                                R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y                                R C3+R 1203 -604 118
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/y                                F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2                                R C3+R 1086 -604 118
61 1 cs_ao22n03c_sl cs_ao22n03c_sl 51 N1437 ---->{f} C2427/y
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b                                F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 64 N1778 ----> C2334/y                                F C3+R 1021 -604 71
30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a                                R
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
C2171/y                                R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1119 ----> C2171/b                                F C3+R 909 -604 71
33 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1696 ----> C1937/y
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a                                R C3+R 868 -604 80 19 1 cs_invvn01c_sl
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc                                R C3+R 868
-604 80 19 1 PI                                0 dcd_blk_dsucc

```

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----- 2 dcd_succ_last                                R C3+R 1474 -545 108 1116 7
PO                                0 dcd_succ_last_t1 RAT                                929
0 ----> C2744/y                                R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a                                F C3+R 1415
cs_invvn01c_sl 59 N675 ---->{a} C2738/y                                F C3+R 1415 -545 83
384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ----> C2738/b
R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 50 N1098 ---->{b}
C2734/y                                R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1098 ----> C2734/a                                F C3+R 1304 -545 83
450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c} C2728/y
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1097 ---->
C2728/b                                R C3+R 1255 -545 108 156 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1692 ----> C2725/y                                R C3+R 1255 -545 108
156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ----> C2725/a                                F
C3+R 1196 -545 83 293 2 cs_invvn01c_sl cs_invvn01c_sl 59 N1479 ---->{d}
C2721/y                                F C3+R 1196 -545 83 293 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1479 ----> C2721/a                                R C3+R 1138 -545 170
108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e} C2550/y
R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl cs_ao22n03c_sl 0 N1858 ---->
C2550/a2                                F C3+R 1044 -545 83 61 1 cs_ao22n03c_sl
cs_ao22n03c_sl 94 N1437 ---->{f} C2427/y                                F C3+R 1044 -545 83
61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ----> C2427/b
R C3+R 995 -545 108 30 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1778 ---->
C2334/y                                R C3+R 995 -545 108 30 1 cs_invvn01c_sl

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cs_invvn01c_sl 0 N1778 ----> C2334/a F C3+R 936 -545 83
71 4 cs_invvn01c_sl cs_invvn01c_sl 59 N1119 ---->{g} C2171/y F
C3+R 936 -545 83 71 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1119 ---->
C2171/b R C3+R 887 -545 108 33 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1696 ----> C1937/y R C3+R 887 -545 108
33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ----> C1937/a F
C3+R 829 -545 80 19 1 cs_invvn01c_sl cs_invvn01c_sl 58 dcd_blk_dsucc ---->
dcd_blk_dsucc F C3+R 829 -545 80 19 1 PI 0
dcd_blk_dsucc

```

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-----
> report_area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
1255.610474 > cputime Used 18.55 cpu seconds or 00:00:18 wall time, used 458752 bytes
or 448 kbytes. > techmap -tlibrary CC8S -seq -timer > echo {Custom Synzilla
Report} Custom Synzilla Report > ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0
upcells 122 IN ports 73 OUT ports 763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763
0 buses 984 nets (0 multiply-driven; 0 undriven) 2585 pins (0 inversions)
2.63 pins per net 1528 literals 22 levels 10 max fanin 19 max fanout
Cell Information FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)
PSEUDO_REG (ncount 83 : area 0) cb_clk_32_1 (ncount 6 : area
480) cb_mode_block (ncount 1 : area 70)
cs_ao12n03c_sl (ncount 5 : area 20) cs_ao22n03c_sl (ncount 17 : area
102) cs_invvn01c_sl (ncount 202 : area 404)
cs_nnd2n02c_sl (ncount 217 : area 651) cs_nnd3n02c_sl (ncount 26 : area
104) cs_nnd4n03c_sl (ncount 8 : area 40)
cs_nor2n02c_sl (ncount 12 : area 36) cs_nor3n03c_sl (ncount 1 : area
4) cs_ao21n03c_sl (ncount 2 : area 10)
cs_ao22n03c_sl (ncount 1 : area 6) cs_xbn2n01b_sl (ncount 1 : area
8) cs_xbo2n01b_sl (ncount 1 : area 8) Total Area =
1943 (Comb = 1393 : Non-Comb = 550) > write_end_point_report -points 2
[ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:52:49 1999 Part : IDCDSUC Mode : Late
Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack Abbreviation Comparison/Description
-----
Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

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```

-----
1 dcd_succ_last F C3+R 1483 -604 71 1116 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1483 -604 71 1116 7 cs_invvn01c_sl

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cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1368 -604 83 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y F C3+R 1368 -604 83
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
C2728/y R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b F C3+R 1251 -604 71
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1692 ----> C2725/y
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y R C3+R 1203 -604 118
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/y F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2 R C3+R 1086 -604 118
61 1 cs_ao22n03c_sl cs_ao22n03c_sl 51 N1437 ---->{f} C2427/y
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 64 N1778 ----> C2334/y F C3+R 1021 -604 71
30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a R
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
C2171/y R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1119 ----> C2171/b F C3+R 909 -604 71
33 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1696 ----> C1937/y
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a R C3+R 868 -604 80 19 1 cs_invvn01c_sl
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc R C3+R 868
-604 80 19 1 PI 0 dcd_blk_dsucc

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```

----- 2 dcd_succ_last R C3+R 1474 -545 108 1116 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y R C3+R 1365 -545 118
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
C2728/y F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b R C3+R 1255 -545 108
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1692 ----> C2725/y
R C3+R 1255 -545 108 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a F C3+R 1196 -545 83 293 2 cs_invvn01c_sl
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y F C3+R 1196 -545 83
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
C2550/y R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2 F C3+R 1044 -545 83
61 1 cs_ao22n03c_sl cs_ao22n03c_sl 94 N1437 ---->{f} C2427/y
F C3+R 1044 -545 83 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b R C3+R 995 -545 108 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1778 ----> C2334/y R C3+R 995 -545 108

```

```

30 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1778 ----> C2334/a                      F
C3+R  936  -545   83   71 4 cs_invvn01c_sl      cs_invvn01c_sl  59 N1119 ---->{g} C2171/y
F C3+R  936  -545   83   71 4 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1119 ---->
C2171/b                      R C3+R  887  -545   108   33 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  49 N1696 ----> C1937/y                      R C3+R  887  -545   108
33 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1696 ----> C1937/a                      F
C3+R  829  -545   80   19 1 cs_invvn01c_sl      cs_invvn01c_sl  58 dcd_blk_dsucc ---->
dcd_blk_dsucc                      F C3+R  829  -545   80   19 1 PI                      0
dcd_blk_dsucc

```

```

-----
> report_area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
1255.610474 > cputime Used 0.99 cpu seconds or 00:00:01 wall time, used 131072 bytes
or 128 kbytes. > freeze_net_loads -reset [TIMER-6411]: Unasserted load on 369 inet(s).
> resize -trace 0 -local -mincut -inc -sequential -ana 100... resize Area : before 5081.39 after
5081.39 (0.00 %) Slack : before -603.6691 after -603.6691 (0.00 %) Cell : before 763 after 763
(0.00 %) Time : 1.750000 > freeze_net_loads -set -limit [TIMER-6412]: Asserted load
on 369 inet(s). > echo {Custom Synzilla Report} Custom Synzilla Report >
ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC) 0 buses 984 nets (0
multiply-driven; 0 undriven) 2585 pins (0 inversions) 2.63 pins per net 1528 literals
22 levels 10 max fanin 19 max fanout Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0) PSEUDO_REG (ncount
83 : area 0) cb_clk_32_1 (ncount 6 : area 480)
cb_mode_block (ncount 1 : area 70) cs_ao12n03c_sl (ncount 5 : area
20) cs_ao22n03c_sl (ncount 17 : area 102)
cs_invvn01c_sl (ncount 202 : area 404) cs_nnd2n02c_sl (ncount 217 : area
651) cs_nnd3n02c_sl (ncount 26 : area 104)
cs_nnd4n03c_sl (ncount 8 : area 40) cs_nor2n02c_sl (ncount 12 : area
36) cs_nor3n03c_sl (ncount 1 : area 4)
cs_ao21n03c_sl (ncount 2 : area 10) cs_ao22n03c_sl (ncount 1 : area
6) cs_xbn2n01b_sl (ncount 1 : area 8)
cs_xbo2n01b_sl (ncount 1 : area 8) Total Area = 1943 (Comb = 1393 :
Non-Comb = 550) > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:52:56 1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.
Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

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```

-----
1 dcd_succ_last          F C3+R  1483  -604   71  1116  7
PO          0 dcd_succ_last_t1 RAT          879
0 ----> C2744/y          F C3+R  1483  -604   71  1116  7 cs_invvn01c_sl
cs_invvn01c_sl  0 dcd_succ_last_t1 ----> C2744/a          R C3+R  1435
-604  118  384  4 cs_invvn01c_sl          cs_invvn01c_sl  47 N675 ---->{a} C2738/y
R C3+R  1435  -604  118  384  4 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N675 ---->
C2738/b          F C3+R  1368  -604   83  1320  5 cs_nnd2n02c_sl
cs_nnd2n02c_sl  68 N1098 ---->{b} C2734/y          F C3+R  1368  -604   83
1320  5 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1098 ----> C2734/a
R C3+R  1315  -604  118  450  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  52 N1097 ---->{c}
C2728/y          R C3+R  1315  -604  118  450  1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N1097 ----> C2728/b          F C3+R  1251  -604   71
156  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  64 N1692 ----> C2725/y
F C3+R  1251  -604   71  156  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1692 ---->
C2725/a          R C3+R  1203  -604  118  293  2 cs_invvn01c_sl
cs_invvn01c_sl  47 N1479 ---->{d} C2721/y          R C3+R  1203  -604  118
293  2 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1479 ----> C2721/a
F C3+R  1137  -604  105  108  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  67 N1858 ---->{e}
C2550/y          F C3+R  1137  -604  105  108  1 cs_ao22n03c_sl
cs_ao22n03c_sl  0 N1858 ----> C2550/a2          R C3+R  1086  -604  118
61  1 cs_ao22n03c_sl          cs_ao22n03c_sl  51 N1437 ---->{f} C2427/y
R C3+R  1086  -604  118  61  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1437 ---->
C2427/b          F C3+R  1021  -604   71  30  1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  64 N1778 ----> C2334/y          F C3+R  1021  -604   71
30  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1778 ----> C2334/a          R
C3+R  974  -604  118  71  4 cs_invvn01c_sl          cs_invvn01c_sl  47 N1119 ---->{g}
C2171/y          R C3+R  974  -604  118  71  4 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N1119 ----> C2171/b          F C3+R  909  -604   71
33  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  64 N1696 ----> C1937/y
F C3+R  909  -604   71  33  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1696 ---->
C1937/a          R C3+R  868  -604   80  19  1 cs_invvn01c_sl
cs_invvn01c_sl  41 dcd_blk_dsucc ----> dcd_blk_dsucc          R C3+R  868
-604  80  19  1 PI          0 dcd_blk_dsucc
-----

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```

-----
2 dcd_succ_last          R C3+R  1474  -545  108  1116  7
PO          0 dcd_succ_last_t1 RAT          929
0 ----> C2744/y          R C3+R  1474  -545  108  1116  7 cs_invvn01c_sl
cs_invvn01c_sl  0 dcd_succ_last_t1 ----> C2744/a          F C3+R  1415
-545  83  384  4 cs_invvn01c_sl          cs_invvn01c_sl  59 N675 ---->{a} C2738/y
F C3+R  1415  -545  83  384  4 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N675 ---->
C2738/b          R C3+R  1365  -545  118  1320  5 cs_nnd2n02c_sl
cs_nnd2n02c_sl  50 N1098 ---->{b} C2734/y          R C3+R  1365  -545  118
1320  5 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1098 ----> C2734/a
F C3+R  1304  -545  83  450  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  61 N1097 ---->{c}
C2728/y          F C3+R  1304  -545  83  450  1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N1097 ----> C2728/b          R C3+R  1255  -545  108
156  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  49 N1692 ----> C2725/y
R C3+R  1255  -545  108  156  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1692 ---->
C2725/a          F C3+R  1196  -545  83  293  2 cs_invvn01c_sl
cs_invvn01c_sl  59 N1479 ---->{d} C2721/y          F C3+R  1196  -545  83
293  2 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1479 ----> C2721/a
R C3+R  1138  -545  170  108  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  59 N1858 ---->{e}
C2550/y          R C3+R  1138  -545  170  108  1 cs_ao22n03c_sl
cs_ao22n03c_sl  0 N1858 ----> C2550/a2          F C3+R  1044  -545  83
-----

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61 1 cs_ao22n03c_sl      cs_ao22n03c_sl  94 N1437 ---->{f} C2427/y
F C3+R  1044  -545   83   61 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1437 ---->
C2427/b                      R C3+R  995  -545   108   30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  49 N1778 ----> C2334/y                      R C3+R  995  -545   108
30 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1778 ----> C2334/a                      F
C3+R  936  -545   83   71 4 cs_invvn01c_sl      cs_invvn01c_sl  59 N1119 ---->{g} C2171/y
F C3+R  936  -545   83   71 4 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1119 ---->
C2171/b                      R C3+R  887  -545   108   33 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  49 N1696 ----> C1937/y                      R C3+R  887  -545   108
33 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1696 ----> C1937/a                      F
C3+R  829  -545   80   19 1 cs_invvn01c_sl      cs_invvn01c_sl  58 dcd_blk_dsucc ---->
dcd_blk_dsucc                      F C3+R  829  -545   80   19 1 PI
dcd_blk_dsucc

```

```

-----
> report_area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
1255.610474      > cputime Used 5.71 cpu seconds or 00:00:06 wall time, used 0 bytes or 0
byte.      > echo {Custom Synzilla Report} Custom Synzilla Report      > ps -cell
Design /HISVHDL/IDCDSUC has:      1 instances 0 upcells      122 IN ports 73 OUT ports
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC)      0 buses      984 nets (0
multiply-driven; 0 undriven)      2585 pins (0 inversions)      2.63 pins per net      1528 literals
22 levels      10 max fanin      19 max fanout      Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)      PSEUDO_REG (ncount
83 : area 0)      cb_clk_32_1 (ncount 6 : area 480)
cb_mode_block (ncount 1 : area 70)      cs_ao12n03c_sl (ncount 5 : area
20)      cs_ao22n03c_sl (ncount 17 : area 102)
cs_invvn01c_sl (ncount 202 : area 404)      cs_nnd2n02c_sl (ncount 217 : area
651)      cs_nnd3n02c_sl (ncount 26 : area 104)
cs_nnd4n03c_sl (ncount 8 : area 40)      cs_nor2n02c_sl (ncount 12 : area
36)      cs_nor3n03c_sl (ncount 1 : area 4)
cs_ao21n03c_sl (ncount 2 : area 10)      cs_ao22n03c_sl (ncount 1 : area
6)      cs_xbn2n01b_sl (ncount 1 : area 8)
cs_xbo2n01b_sl (ncount 1 : area 8)      Total Area = 1943 (Comb = 1393 :
Non-Comb = 550)      > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report      for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:52:57 1999 Part : IDCDSUC Mode : Late Mode / Nominal      EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38      Max. Slack: 1.13427E+38 Sort Field: Slack      Max.
Endpoints: 2 Cause of Slack      Abbreviation Comparison/Description -----
-----      Slack Continuation      SlkCont      Slack due to a point downstream on
path Required Arrival Time      RAT      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT      ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup      ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold      ClkGHld      ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width      ClkTPW      (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup      Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold      Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
EndOfC      ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
ClockPulseWidth      ClkPW      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation      ClkSep      ( CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop      ALTest      ( DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
ATLimit      Slack discontinuity due to failed test      Num/
LimitedAT/      Delay/ Failed Test/      Test PinName
E Phase      AT      Slack      Slew      CL      FO      Cell      P Func      T.Adj      NetName

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```

-----
1 dcd_succ_last
PO
0 ----> C2744/y
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
C2728/y
cs_nnd2n02c_sl 0 N1097 ----> C2728/b
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1692 ----> C2725/y
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/y
cs_ao22n03c_sl 0 N1858 ----> C2550/a2
61 1 cs_ao22n03c_sl cs_ao22n03c_sl 51 N1437 ---->{f} C2427/y
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b
cs_nnd2n02c_sl 64 N1778 ----> C2334/y
30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
C2171/y
cs_nnd2n02c_sl 0 N1119 ----> C2171/b
33 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1696 ----> C1937/y
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc
-604 80 19 1 PI 0 dcd_blk_dsucc
-----

```

```

-----
2 dcd_succ_last
PO
0 ----> C2744/y
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
C2728/y
cs_nnd2n02c_sl 0 N1097 ----> C2728/b
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1692 ----> C2725/y
R C3+R 1255 -545 108 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
C2550/y
cs_ao22n03c_sl 0 N1858 ----> C2550/a2
-----

```

```

61 1 cs_ao22n03c_sl      cs_ao22n03c_sl  94 N1437 ---->{f} C2427/y
F C3+R 1044 -545 83 61 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1437 ---->
C2427/b                      R C3+R 995 -545 108 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1778 ----> C2334/y                      R C3+R 995 -545 108
30 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1778 ----> C2334/a                      F
C3+R 936 -545 83 71 4 cs_invvn01c_sl      cs_invvn01c_sl  59 N1119 ---->{g} C2171/y
F C3+R 936 -545 83 71 4 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1119 ---->
C2171/b                      R C3+R 887 -545 108 33 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1696 ----> C1937/y                      R C3+R 887 -545 108
33 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1696 ----> C1937/a                      F
C3+R 829 -545 80 19 1 cs_invvn01c_sl      cs_invvn01c_sl  58 dcd_blk_dsucc ---->
dcd_blk_dsucc                      F C3+R 829 -545 80 19 1 PI
dcd_blk_dsucc

```

```

-----
> report_area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
1255.610474 > cputime Used 1.20 cpu seconds or 00:00:01 wall time, used 0 bytes or 0
byte. > echo {Custom Synzilla Report} Custom Synzilla Report > ps -cell Design
/HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC) 0 buses 984 nets (0
multiply-driven; 0 undriven) 2585 pins (0 inversions) 2.63 pins per net 1528 literals
22 levels 10 max fanin 19 max fanout Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0) PSEUDO_REG (ncount
83 : area 0) cb_clk_32_1 (ncount 6 : area 480)
cb_mode_block (ncount 1 : area 70) cs_ao12n03c_sl (ncount 5 : area
20) cs_ao22n03c_sl (ncount 17 : area 102)
cs_invvn01c_sl (ncount 202 : area 404) cs_nnd2n02c_sl (ncount 217 : area
651) cs_nnd3n02c_sl (ncount 26 : area 104)
cs_nnd4n03c_sl (ncount 8 : area 40) cs_nor2n02c_sl (ncount 12 : area
36) cs_nor3n03c_sl (ncount 1 : area 4)
cs_oa21n03c_sl (ncount 2 : area 10) cs_oa22n03c_sl (ncount 1 : area
6) cs_xbn2n01b_sl (ncount 1 : area 8)
cs_xbo2n01b_sl (ncount 1 : area 8) Total Area = 1943 (Comb = 1393 :
Non-Comb = 550) > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:52:58 1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.
Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree.Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

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-----
1 dcd_succ_last          F C3+R  1483  -604   71  1116  7
PO          0 dcd_succ_last_t1 RAT          879
0 ----> C2744/y          F C3+R  1483  -604   71  1116  7 cs_invvn01c_sl
cs_invvn01c_sl  0 dcd_succ_last_t1 ----> C2744/a          R C3+R  1435
-604  118  384  4 cs_invvn01c_sl          cs_invvn01c_sl  47 N675 ---->{a} C2738/y
R C3+R  1435  -604  118  384  4 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N675 ---->
C2738/b          F C3+R  1368  -604   83  1320  5 cs_nnd2n02c_sl
cs_nnd2n02c_sl  68 N1098 ---->{b} C2734/y          F C3+R  1368  -604   83
1320  5 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1098 ----> C2734/a
R C3+R  1315  -604  118  450  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  52 N1097 ---->{c}
C2728/y          R C3+R  1315  -604  118  450  1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N1097 ----> C2728/b          F C3+R  1251  -604   71
156  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  64 N1692 ----> C2725/y
F C3+R  1251  -604   71  156  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1692 ---->
C2725/a          R C3+R  1203  -604  118  293  2 cs_invvn01c_sl
cs_invvn01c_sl  47 N1479 ---->{d} C2721/y          R C3+R  1203  -604  118
293  2 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1479 ----> C2721/a
F C3+R  1137  -604  105  108  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  67 N1858 ---->{e}
C2550/y          F C3+R  1137  -604  105  108  1 cs_ao22n03c_sl
cs_ao22n03c_sl  0 N1858 ----> C2550/a2          R C3+R  1086  -604  118
61  1 cs_ao22n03c_sl          cs_ao22n03c_sl  51 N1437 ---->{f} C2427/y
R C3+R  1086  -604  118  61  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1437 ---->
C2427/b          F C3+R  1021  -604   71  30  1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  64 N1778 ----> C2334/y          F C3+R  1021  -604   71
30  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1778 ----> C2334/a          R
C3+R  974  -604  118  71  4 cs_invvn01c_sl          cs_invvn01c_sl  47 N1119 ---->{g}
C2171/y          R C3+R  974  -604  118  71  4 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N1119 ----> C2171/b          F C3+R  909  -604   71
33  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  64 N1696 ----> C1937/y
F C3+R  909  -604   71  33  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1696 ---->
C1937/a          R C3+R  868  -604   80  19  1 cs_invvn01c_sl
cs_invvn01c_sl  41 dcd_blk_dsucc ----> dcd_blk_dsucc          R C3+R  868
-604  80  19  1 PI          0 dcd_blk_dsucc
-----

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-----
2 dcd_succ_last          R C3+R  1474  -545  108  1116  7
PO          0 dcd_succ_last_t1 RAT          929
0 ----> C2744/y          R C3+R  1474  -545  108  1116  7 cs_invvn01c_sl
cs_invvn01c_sl  0 dcd_succ_last_t1 ----> C2744/a          F C3+R  1415
-545  83  384  4 cs_invvn01c_sl          cs_invvn01c_sl  59 N675 ---->{a} C2738/y
F C3+R  1415  -545  83  384  4 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N675 ---->
C2738/b          R C3+R  1365  -545  118  1320  5 cs_nnd2n02c_sl
cs_nnd2n02c_sl  50 N1098 ---->{b} C2734/y          R C3+R  1365  -545  118
1320  5 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1098 ----> C2734/a
F C3+R  1304  -545  83  450  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  61 N1097 ---->{c}
C2728/y          F C3+R  1304  -545  83  450  1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N1097 ----> C2728/b          R C3+R  1255  -545  108
156  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  49 N1692 ----> C2725/y
R C3+R  1255  -545  108  156  1 cs_invvn01c_sl          cs_invvn01c_sl  0 N1692 ---->
C2725/a          F C3+R  1196  -545  83  293  2 cs_invvn01c_sl
cs_invvn01c_sl  59 N1479 ---->{d} C2721/y          F C3+R  1196  -545  83
293  2 cs_nnd2n02c_sl          cs_nnd2n02c_sl  0 N1479 ----> C2721/a
R C3+R  1138  -545  170  108  1 cs_nnd2n02c_sl          cs_nnd2n02c_sl  59 N1858 ---->{e}
C2550/y          R C3+R  1138  -545  170  108  1 cs_ao22n03c_sl
cs_ao22n03c_sl  0 N1858 ----> C2550/a2          F C3+R  1044  -545  83
-----

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61 1 cs_ao22n03c_sl      cs_ao22n03c_sl  94 N1437 ---->{f} C2427/y
F C3+R  1044  -545   83  61 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1437 ---->
C2427/b                      R C3+R  995  -545   108  30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  49 N1778 ----> C2334/y                      R C3+R  995  -545   108
30 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1778 ----> C2334/a                      F
C3+R  936  -545   83  71 4 cs_invvn01c_sl      cs_invvn01c_sl  59 N1119 ---->{g} C2171/y
F C3+R  936  -545   83  71 4 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1119 ---->
C2171/b                      R C3+R  887  -545   108  33 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  49 N1696 ----> C1937/y                      R C3+R  887  -545   108
33 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1696 ----> C1937/a                      F
C3+R  829  -545   80  19 1 cs_invvn01c_sl      cs_invvn01c_sl  58 dcd_blk_dsucc ---->
dcd_blk_dsucc                      F C3+R  829  -545   80  19 1 PI
dcd_blk_dsucc

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-----
> report_area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
1255.610474 > cputime Used 0.93 cpu seconds or 00:00:01 wall time, used 0 bytes or 0
byte. > echo {=== Technology mapping process finished ===} === Technology mapping process
finished === > load_update -invalidate Good names for IDCDSUC Count
User Transform New For all nets 984 537 0 447 For all nets
984 54.57% 0.00% 45.43% For I/O port nets 184 70.65% 0.00% 29.35%
For register output nets 166 100.00% 0.00% 0.00% Count
User Transform New For all boxes 763 270 0 493 For all boxes
763 35.39% 0.00% 64.61% For register boxes 83 100.00% 0.00% 0.00%
For linked boxes 763 35.39% 0.00% 64.61% > echo {Custom Synzilla
Report} Custom Synzilla Report > ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0
upcells 122 IN ports 73 OUT ports 763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763
LINKED; 0 UNLINKED; 0 DC) 0 buses 984 nets (0 multiply-driven; 0 undriven)
2585 pins (0 inversions) 2.63 pins per net 1528 literals 22 levels 10 max fanin
19 max fanout Cell Information FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area 0) PSEUDO_REG (ncount 83 : area 0)
cb_clk_32_1 (ncount 6 : area 480) cb_mode_block (ncount 1 : area
70) cs_ao12n03c_sl (ncount 5 : area 20)
cs_ao22n03c_sl (ncount 17 : area 102) cs_invvn01c_sl (ncount 202 : area
404) cs_nnd2n02c_sl (ncount 217 : area 651)
cs_nnd3n02c_sl (ncount 26 : area 104) cs_nnd4n03c_sl (ncount 8 : area
40) cs_nor2n02c_sl (ncount 12 : area 36)
cs_nor3n03c_sl (ncount 1 : area 4) cs_oa21n03c_sl (ncount 2 : area
10) cs_oa22n03c_sl (ncount 1 : area 6)
cs_xbn2n01b_sl (ncount 1 : area 8) cs_xbo2n01b_sl (ncount 1 : area
8) Total Area = 1943 (Comb = 1393 : Non-Comb = 550) >
write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report for file
/tmp/end_point_report..147522. [load_update]: Number of pin load calculations: 7541 since last stats
[load_update]: Number of pin weight calculations: 0 since last stats [ET-0019]:<End.....New Endpoint
Report. Sun Apr 18 21:52:59 1999 Part : IDCDSUC Mode : Late Mode / Nominal
EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min.
Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.
Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold

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(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
 EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
 ClockPulseWidth CkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE) ClockSeparation CkSep (CLOCK1 ARRIVAL TIME + CLOCK
 SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
 ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
 ATLimit Slack discontinuity due to failed test Num/
 LimitedAT/ Delay/ Failed Test/ Test PinName
 E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

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----- 1 dcd_succ_last F C3+R 1483 -604 71 1116 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1483 -604 71 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1368 -604 83 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y F C3+R 1368 -604 83
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
C2728/y R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b F C3+R 1251 -604 71
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1692 ----> C2725/y
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y R C3+R 1203 -604 118
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/y F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2 R C3+R 1086 -604 118
61 1 cs_ao22n03c_sl cs_ao22n03c_sl 51 N1437 ---->{f} C2427/y
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 64 N1778 ----> C2334/y F C3+R 1021 -604 71
30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a R
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
C2171/y R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1119 ----> C2171/b F C3+R 909 -604 71
33 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1696 ----> C1937/y
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a R C3+R 868 -604 80 19 1 cs_invvn01c_sl
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc R C3+R 868
-604 80 19 1 PI 0 dcd_blk_dsucc

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----- 2 dcd_succ_last R C3+R 1474 -545 108 1116 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y R C3+R 1365 -545 118
1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
C2728/y F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl

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cs_nnd2n02c_sl 0 N1097 ----> C2728/b R C3+R 1255 -545 108
156 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1692 ----> C2725/y
R C3+R 1255 -545 108 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a F C3+R 1196 -545 83 293 2 cs_invvn01c_sl
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y F C3+R 1196 -545 83
293 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
C2550/y R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2 F C3+R 1044 -545 83
61 1 cs_ao22n03c_sl cs_ao22n03c_sl 94 N1437 ---->{f} C2427/y
F C3+R 1044 -545 83 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b R C3+R 995 -545 108 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1778 ----> C2334/y R C3+R 995 -545 108
30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a F
C3+R 936 -545 83 71 4 cs_invvn01c_sl cs_invvn01c_sl 59 N1119 ---->{g} C2171/y
F C3+R 936 -545 83 71 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1119 ---->
C2171/b R C3+R 887 -545 108 33 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1696 ----> C1937/y R C3+R 887 -545 108
33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ----> C1937/a F
C3+R 829 -545 80 19 1 cs_invvn01c_sl cs_invvn01c_sl 58 dcd_blk_dsucc ---->
dcd_blk_dsucc F C3+R 829 -545 80 19 1 PI 0
dcd_blk_dsucc

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-----
> report_area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
1255.610474 > cputime Used 1.45 cpu seconds or 00:00:01 wall time, used 0 bytes or 0 byte.
[hnl_attr]: Attributes registered for copy for type: PORT. MASK_ANYTHING_MASKED_ON_PORT
[hnl_attr]: Attributes registered for copy for type: CELL. MASK_ANYTHING_MASKED_ON_CELL
MASK_USER_CELL_NOCHANGE MASK_USER_CELL_NODESTROY
MASK_USER_CELL_NOTOUCH SUGGESTED_LIBRARY_CELL SUGGESTED_PARALLEL_FANOUT
SUGGESTED_SIZE SUGGESTED_SWAP SYN_USAGE_BOX_HIDE [hnl_attr]: Attributes registered for
copy for type: PIN. MASK_ANYTHING_MASKED_ON_PIN MASK_USER_PIN_NOADD
MASK_USER_PIN_NOCHANGE MASK_USER_PIN_NONEWNET MASK_USER_PIN_NOTOUCH
SUGGESTED_SERIAL_FANOUT SYN_SAS_NAME [hnl_attr]: Attributes registered for copy for type:
NET. MASK_ANYTHING_MASKED_ON_NET MASK_USER_NET_NOTOUCH [hnl_attr]: 0 port(s) have
attribute(s) registered for copy. [hnl_attr]: 197 cell(s) have attribute(s) registered for copy. [hnl_attr]: 10
net(s) have attribute(s) registered for copy. [hnl_attr]: 1242 pin(s) have attribute(s) registered for copy.
> echo {=== CDS process ===} === CDS process === Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/cds_disc.tcl > time_units -nano
> time_units -nano > reset_timing_area > echo {Custom Synzilla Report} Custom
Synzilla Report > ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells
122 IN ports 73 OUT ports 763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0
UNLINKED; 0 DC) 0 buses 984 nets (0 multiply-driven; 0 undriven) 2585 pins (0
inversions) 2.63 pins per net 1528 literals 22 levels 10 max fanin 19 max fanout
Cell Information FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)
PSEUDO_REG (ncount 83 : area 0) cb_clk_32_1 (ncount 6 : area
480) cb_mode_block (ncount 1 : area 70)
cs_ao12n03c_sl (ncount 5 : area 20) cs_ao22n03c_sl (ncount 17 : area
102) cs_invvn01c_sl (ncount 202 : area 404)
cs_nnd2n02c_sl (ncount 217 : area 651) cs_nnd3n02c_sl (ncount 26 : area
104) cs_nnd4n03c_sl (ncount 8 : area 40)
cs_nor2n02c_sl (ncount 12 : area 36) cs_nor3n03c_sl (ncount 1 : area
4) cs_oa21n03c_sl (ncount 2 : area 10)
cs_oa22n03c_sl (ncount 1 : area 6) cs_xbn2n01b_sl (ncount 1 : area
8) cs_xbo2n01b_sl (ncount 1 : area 8) Total Area =
1943 (Comb = 1393 : Non-Comb = 550) > write_end_point_report -points 2

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[ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.
 [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:53:03 1999 Part : IDCDSUC Mode : Late
 Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
 Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
 Max. Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----

----- Slack Continuation SlkCont Slack due to a point downstream on
 path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
 Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
 Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
 GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (CLOCK
 LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
 (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
 (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
 EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
 SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
 ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
 ATLimit Slack discontinuity due to failed test Num/
 LimitedAT/ Delay/ Failed Test/ Test PinName
 E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```
----- 1 dcd_succ_last F C3+R 1483 -604 71 1172 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1483 -604 71 1172 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1435
-604 118 416 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 416 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1368 -604 83 1360 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y F C3+R 1368 -604 83
1360 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
R C3+R 1315 -604 118 458 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
C2728/y R C3+R 1315 -604 118 458 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b F C3+R 1251 -604 71
164 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1692 ----> C2725/y
F C3+R 1251 -604 71 164 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a R C3+R 1203 -604 118 309 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y R C3+R 1203 -604 118
309 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
F C3+R 1137 -604 105 116 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/y F C3+R 1137 -604 105 116 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2 R C3+R 1086 -604 118
69 1 cs_ao22n03c_sl cs_ao22n03c_sl 51 N1437 ---->{f} C2427/y
R C3+R 1086 -604 118 69 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b F C3+R 1021 -604 71 38 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 64 N1778 ----> C2334/y F C3+R 1021 -604 71
38 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a R
C3+R 974 -604 118 103 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
C2171/y R C3+R 974 -604 118 103 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1119 ----> C2171/b F C3+R 909 -604 71
41 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1696 ----> C1937/y
F C3+R 909 -604 71 41 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a R C3+R 868 -604 80 27 1 cs_invvn01c_sl
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc R C3+R 868
```


-604 80 27 1 PI

0 dcd_blk_dsucc

```
-----
2 dcd_succ_last R C3+R 1474 -545 108 1172 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1474 -545 108 1172 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1415
-545 83 416 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 416 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1365 -545 118 1360 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y R C3+R 1365 -545 118
1360 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
F C3+R 1304 -545 83 458 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
C2728/y F C3+R 1304 -545 83 458 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b R C3+R 1255 -545 108
164 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1692 ----> C2725/y
R C3+R 1255 -545 108 164 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a F C3+R 1196 -545 83 309 2 cs_invvn01c_sl
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y F C3+R 1196 -545 83
309 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1479 ----> C2721/a
R C3+R 1138 -545 170 116 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
C2550/y R C3+R 1138 -545 170 116 1 cs_ao22n03c_sl
cs_ao22n03c_sl 0 N1858 ----> C2550/a2 F C3+R 1044 -545 83
69 1 cs_ao22n03c_sl cs_ao22n03c_sl 94 N1437 ---->{f} C2427/y
F C3+R 1044 -545 83 69 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b R C3+R 995 -545 108 38 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1778 ----> C2334/y R C3+R 995 -545 108
38 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a F
C3+R 936 -545 83 103 4 cs_invvn01c_sl cs_invvn01c_sl 59 N1119 ---->{g}
C2171/y F C3+R 936 -545 83 103 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1119 ----> C2171/b R C3+R 887 -545 108
41 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1696 ----> C1937/y
R C3+R 887 -545 108 41 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a F C3+R 829 -545 80 27 1 cs_invvn01c_sl
cs_invvn01c_sl 58 dcd_blk_dsucc ----> dcd_blk_dsucc F C3+R 829
-545 80 27 1 PI 0 dcd_blk_dsucc
-----
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-----
> report_area [load_update]: Found 723 pin load values not up-to-date,
forcing queries [load_update]: Warning - Detected load inconsistencies, forcing global invalidation
[load_update]: Number of pin load calculations: 4599 since last stats [load_update]: Number of pin weight
calculations: 0 since last stats Design: /IDCDSUC - Area: 5301.955566, Area(Weight): 1255.610474
> cputime Used 3.86 cpu seconds or 00:00:04 wall time, used 0 bytes or 0 byte. > report_drc
Checking DRC for IDesign IDCDSUC INet clk1_mode7:clk1_mode7 has cap violation 1.046, load 147.5,
limit 141, multiplier 1 slack 1.134e+38 INet a_clk:a_clk has cap violation 1.046, load 147.5, limit
141, multiplier 1 slack 1.134e+38 INet b_clk:b_clk has cap violation 1.093, load 154.1, limit 141,
multiplier 1 slack 349 INet test_c1:test_c1 has cap violation 1.078, load 152.1, limit 141,
multiplier 1 slack 349 INet clkg:clkg has cap violation 1.202, load 169.5, limit 141, multiplier 1
slack 1.134e+38 INet ireg_valid:ireg_valid has cap violation 1.207, load 170.3, limit 141, multiplier
1 slack -498.7 INet clk2:clk2 has cap violation 1.202, load 169.5, limit 141, multiplier 1 slack
1.134e+38 INet scan_enable:scan_enable has cap violation 1.261, load 177.8, limit 141, multiplier
1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099, multiplier 1 RISE:
transition 500, limit 455; FALL: transition 500, limit 455 INet eu_iu_srlz_op_encode(11):a has
transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit
455 INet op_cmp_tr_q:l2_out_n has cap violation 1.009, load 249.3, limit 247, multiplier 1 slack
617 INet rcvry_reset_q:l2_out_n has cap violation 1.123, load 277.5, limit 247, multiplier 1 slack
331 INet iu_reset_op_c:y has cap violation 1.227, load 1227, limit 1000, multiplier 1 slack 133
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INet dcd_succ_last_t1:y has cap violation 1.215, load 1216, limit 1001, multiplier 1 slack -603.7
INet local_milli_q:l2_out_n has cap violation 1.138, load 281.1, limit 247, multiplier 1 slack -207.8
INet srlz_nomatch_q:l2_out_n has cap violation 1.021, load 252.2, limit 247, multiplier 1 slack
392 INet dcd_succ_dly_q:l2_out_n has cap violation 1.018, load 251.5, limit 247, multiplier 1 slack
355.4 INet iu_reset_all:y has cap violation 1.389, load 833.6, limit 600, multiplier 1 slack 322.9
INet local_milli_t1_q:l2_out_n has cap violation 1.018, load 251.5, limit 247, multiplier 1 slack
-42.98 INet local_milli_t2_q:l2_out_n has cap violation 1.018, load 251.5, limit 247, multiplier 1
slack 230.4 INet exc_cond_q:l2_out_n has cap violation 1.142, load 282.1, limit 247, multiplier 1
slack 322.9 INet slow_mode_t2_q:l2_out_n has cap violation 1.009, load 249.3, limit 247, multiplier
1 slack 617 INet iu_rstfst_q:l2_out_n has cap violation 1.02, load 251.9, limit 247, multiplier 1
slack -42.98 INet exc_info_q(0):l2_out_n has cap violation 1.028, load 254, limit 247, multiplier 1
slack 610.4 INet exc_info_q(1):l2_out_n has cap violation 1.047, load 258.7, limit 247, multiplier 1
slack -476.5 INet exc_info_q(2):l2_out_n has cap violation 1.061, load 262.2, limit 247, multiplier 1
slack 611.1 INet exc_info_q(3):l2_out_n has cap violation 1.063, load 262.6, limit 247, multiplier 1
slack 603.1 INet dcd_cyl_cnt_q(0):l2_out_n has cap violation 1.134, load 280.2, limit 247, multiplier
1 slack -351.1 INet dcd_cyl_cnt_q(1):l2_out_n has cap violation 1.145, load 282.9, limit 247,
multiplier 1 slack -346.9 INet slow_mode_blk_q:l2_out_n has cap violation 1.03, load 254.4, limit
247, multiplier 1 slack -221.5 INet br_wrongs_q:l2_out_n has cap violation 1.069, load 264.1, limit
247, multiplier 1 slack 133 INet rst_rst_q:l2_out_n has cap violation 1.065, load 263.2, limit
247, multiplier 1 slack 340.9 INet N22:y has cap violation 1.212, load 1213, limit 1001, multiplier
1 slack 617 INet N26:y has cap violation 1.224, load 1226, limit 1001, multiplier 1 slack 392
INet N36:y has cap violation 1.187, load 1188, limit 1001, multiplier 1 slack 617 INet N134:y has
cap violation 1.177, load 1178, limit 1001, multiplier 1 slack 355.4 INet N158:y has cap violation
1.116, load 1117, limit 1001, multiplier 1 slack 617 INet N1098:y has cap violation 1.403, load
1403, limit 1000, multiplier 1 slack -603.7 IDesign IDCDSUC has 38 violations
freeze_net_loads-set-limit [TIMER-6411]: Unasserted load on 369 inet(s). [TIMER-6412]: Asserted load
on 369 inet(s). > cpr_eval > tgfs_redund-effort 50 > cputime {
tgfs_rewrite-tech-$rwr_effort } > tgfs_rewrite-tech-high tgfs rewiring Area : before
5441.99 after 5359.17 (1.52 %) Slack : before -603.6691 after -543.6871 (9.94 %) Cell : before
763 after 762 (0.13 %) Time : 20.260000 Used 20.89 cpu seconds or 00:00:21 wall time, used 65536
bytes or 64 kbytes. Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/tf.dll tf.dll
version 1.0 (Apr 14 1999 18:12:48) Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/sim.dll sim.dll version 1.0 (Apr 14 1999
18:12:45) Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/tc.dll tc.dll version 1.0
(Apr 14 1999 18:12:53) > tc::trestruct-sizeless-leaf_flex 1.02 -gain 5 -load 5 >
tc::critflow-depth 3-xforms __CiType_30_30a78098 Transform: trestruct 0.1 Options: Mode=Sizeless
GainBuckets=5 LoadBuckets=5 MinInputs=2 MaxInputs=1024 PartialTree=false
SingleCell=false SlackThreshold=0.000 LeafFlexibility=1.020 GA_Wire: Load=18.000
Delay=0.000 Slew=0.000 [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
> echo {Custom Synzilla Report} Custom Synzilla Report > ps-cell Design
/HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
774 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 774 LINKED; 0 UNLINKED; 0 DC) 0 buses 995 nets (0
multiply-driven; 0 undriven) 2607 pins (0 inversions) 2.62 pins per net 1539 literals

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22 levels      10 max fanin      19 max fanout      Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)      PSEUDO_REG (ncount
83 : area 0)      cb_clk_32_1 (ncount 6 : area 480)
cb_mode_block (ncount 1 : area 70)      cs_ao12n03c_sl (ncount 6 : area
24)      cs_ao22n03c_sl (ncount 16 : area 96)
cs_invvn01c_sl (ncount 216 : area 432)      cs_nnd2n02c_sl (ncount 209 : area
627)      cs_nnd3n02c_sl (ncount 26 : area 104)
cs_nnd4n03c_sl (ncount 9 : area 45)      cs_nor2n02c_sl (ncount 14 : area
42)      cs_nor3n03c_sl (ncount 2 : area 8)
cs_oa21n03c_sl (ncount 3 : area 15)      cs_oa22n03c_sl (ncount 1 : area
6)      cs_xbn2n01b_sl (ncount 1 : area 8)
cs_xbo2n01b_sl (ncount 1 : area 8)      Total Area = 1965 (Comb = 1415 :
Non-Comb = 550)      > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report      for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:53:42 1999 Part : IDCDSUC Mode : Late Mode / Nominal      EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38      Max. Slack: 1.13427E+38 Sort Field: Slack      Max.
Endpoints: 2 Cause of Slack      Abbreviation Comparison/Description -----
----- Slack Continuation      SlkCont      Slack due to a point downstream on
path Required Arrival Time      RAT      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT      ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup      ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold      ClkGHld      ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width      ClkTPW      (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup      Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold      Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
EndOfC      ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
ClockPulseWidth      ClkPW      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation      ClkSep      ( CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop      ALTest      ( DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
ATLimit      Slack discontinuity due to failed test      Num/
LimitedAT/      Delay/ Failed Test/      Test PinName
E Phase      AT      Slack      Slew      CL      FO      Cell      P Func      T.Adj      NetName
-----
----- 1 dcd_succ_last      F C3+R      1392      -513      71      1160      7
PO      0 dcd_succ_last_t1 RAT      879
0 ----> C2744/y      F C3+R      1392      -513      71      1160      7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a      R C3+R      1345
-513 118 412 4 cs_invvn01c_sl      cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1345 -513 118 412 4 cs_nnd2n02c_sl      cs_nnd2n02c_sl 0 N675 ---->
C2738/b      F C3+R 1282 -513 66 1326 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 63 N1098 ----> C2734rwr/y      F C3+R 1282 -513 66
1326 4 cs_invvn01c_sl      cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
R C3+R 1241 -513 99 446 1 cs_invvn01c_sl      cs_invvn01c_sl 41 N1097 ---->
C2728rwr/y      R C3+R 1241 -513 99 446 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a      F C3+R 1187 -513 83
178 2 cs_invvn01c_sl      cs_invvn01c_sl 54 N1692 ---->{b} C2725rwr/y
F C3+R 1187 -513 83 178 2 cs_nnd2n02c_sl      cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a      R C3+R 1127 -513 188 314 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 60 N1479 ---->{c} C2721rwr/y      R C3+R 1127 -513
188 314 2 cs_nnd3n02c_sl      cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/b
F C3+R 1028 -513 77 174 2 cs_nnd3n02c_sl      cs_nnd3n02c_sl 98 N1497 ---->{d}
C2709/y      F C3+R 1028 -513 77 174 2 cs_nor2n02c_sl

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cs_nor2n02c_sl 0 N1497 ----> C2709/a R C3+R 977 -513 155
82 1 cs_nor2n02c_sl cs_nor2n02c_sl 51 N1986 ---->{e} C2677/y
R C3+R 977 -513 155 82 1 cs_nnd4n03c_sl cs_nnd4n03c_sl 0 N1986 ---->
C2677/a F C3+R 912 -513 71 45 1 cs_nnd4n03c_sl
cs_nnd4n03c_sl 65 N1849 ----> C2591/y F C3+R 912 -513 71
45 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1849 ----> C2591/a R
C3+R 865 -513 113 23 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1976 ---->{f}
C2579rwr_0/y R C3+R 865 -513 113 23 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1976 ----> C2579rwr_0/a F C3+R 799 -513
117 118 6 cs_nnd2n02c_sl cs_nnd2n02c_sl 66 ireg_valid ----> ireg_valid
F C3+R 799 -513 117 118 6 PI 0 ireg_valid

-----
2 dcd_succ_last R C3+R 1386 -457 108 1160 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1386 -457 108 1160 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1327
-457 83 412 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1327 -457 83 412 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1279 -457 99 1326 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 48 N1098 ----> C2734rwr/y R C3+R 1279 -457
99 1326 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
F C3+R 1229 -457 66 446 1 cs_invvn01c_sl cs_invvn01c_sl 50 N1097 ---->
C2728rwr/y F C3+R 1229 -457 66 446 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a R C3+R 1186 -457 118
178 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
R C3+R 1186 -457 118 178 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a F C3+R 1113 -457 135 314 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 73 N1479 ---->{c} C2721rwr/y F C3+R 1113 -457
135 314 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/b
R C3+R 1030 -457 134 174 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 83 N1497
---->{d} C2709/y R C3+R 1030 -457 134 174 2 cs_nor2n02c_sl
cs_nor2n02c_sl 0 N1497 ----> C2709/a F C3+R 955 -457 107
82 1 cs_nor2n02c_sl cs_nor2n02c_sl 75 N1986 ---->{e} C2677/y
F C3+R 955 -457 107 82 1 cs_nnd4n03c_sl cs_nnd4n03c_sl 0 N1986 ---->
C2677/d R C3+R 888 -457 172 62 2 cs_nnd4n03c_sl
cs_nnd4n03c_sl 68 N1719 ---->{f} C2599rwr/y R C3+R 888 -457
172 62 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1719 ----> C2599rwr/a
F C3+R 811 -457 66 42 1 cs_nor3n03c_sl cs_nor3n03c_sl 77 N1942 ---->
C2349rwr_0_0/y F C3+R 811 -457 66 42 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1942 ----> C2349rwr_0_0/a R C3+R 768 -457
118 24 1 cs_invvn01c_sl cs_invvn01c_sl 44 N288 ---->{g} C2339/y
R C3+R 768 -457 118 24 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N288 ---->
C2339/a F C3+R 706 -457 83 18 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 61 NET690 ---->{h} C2187/y F C3+R 706 -457
83 18 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 NET690 ----> C2187/a
R C3+R 656 -457 108 32 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 51 N29 ---->
C2020/y R C3+R 656 -457 108 32 2 cs_invvn01c_sl
cs_invvn01c_sl 0 N29 ----> C2020/a F C3+R 557 -457 424
19 1 cs_invvn01c_sl cs_invvn01c_sl 99 du_iu_hold_aa_req ----> du_iu_hold_aa_req
F C3+R 557 -457 424 19 1 PI 0 du_iu_hold_aa_req

-----
> report_area [load_update]: Found 620 pin load values not up-to-date,
forcing queries [load_update]: Warning - Detected load inconsistencies, forcing global invalidation
[load_update]: Number of pin load calculations: 8096 since last stats [load_update]: Number of pin weight
calculations: 0 since last stats Design: /IDCDSUC - Area: 5226.390137, Area(Weight): 1270.181396

```

```
> cputime Used 38.94 cpu seconds or 00:00:39 wall time, used 299008 bytes or 292 kbytes.
> report_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap violation 1.032, load 145.5,
limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit
141, multiplier 1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099,
multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet
eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit
455; FALL: transition 500, limit 455 INet iu_reset_op_c:y has cap violation 1.219, load 1219, limit
1000, multiplier 1 slack 133 INet dcd_succ_last_t1:y has cap violation 1.115, load 1116, limit
1001, multiplier 1 slack -513.2 INet iu_reset_all:y has cap violation 1.328, load 796.6, limit 600,
multiplier 1 slack 322.9 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1
slack 617 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier 1 slack 392
INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 617 INet N134:y has
cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 355.4 INet N158:y has cap violation
1.108, load 1109, limit 1001, multiplier 1 slack 617 INet N1098:y has cap violation 1.302, load
1303, limit 1001, multiplier 1 slack -513.2 IDesign IDCDSUC has 13 violations
cpr_eval > echo {In restructure loop} In restructure loop > echo -583.569129373
-583.569129373 > echo -513.216552734 -513.216552734 > tgfs_redund
ch -$rwr_effort } > tgfs_rewire -tech -high tgfs rewiring Area : before 5133.28 after
5092.88 (0.79 %) Slack : before -513.2166 after -506.3137 (1.35 %) Cell : before 775 after 773
(0.26 %) Time : 13.960000 Used 14.51 cpu seconds or 00:00:14 wall time, used 0 bytes or 0 byte.
> tc:trestruct -sizeless -leaf_flex 1.02 -gain 5 -load 5 > tc:critflow -depth 3 -xforms
__CiType_30_31c4d268 Transform: trestruct 0.1 Options: Mode=Sizeless GainBuckets=5
LoadBuckets=5 MinInputs=2 MaxInputs=1024 PartialTree=false
SingleCell=false SlackThreshold=0.000 LeafFlexibility=1.020 [ET-0112]:Deleting timing for
design: sub_design, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
sub_design, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design,
analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. > echo {Custom Synzilla Report} Custom Synzilla Report
> ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
773 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 772 LINKED; 0 UNLINKED; 0 DC) 0 buses 994 nets (0
multiply-driven; 0 undriven) 2604 pins (0 inversions) 2.62 pins per net 1537 literals
21 levels 10 max fanin 19 max fanout Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0) PSEUDO_REG (ncount
83 : area 0) cb_clk_32_1 (ncount 6 : area 480)
cb_mode_block (ncount 1 : area 70) cs_ao12n03c_sl (ncount 6 : area
24) cs_ao22n03c_sl (ncount 16 : area 96)
cs_invv01c_sl (ncount 213 : area 426) cs_nnd2n02c_sl (ncount 211 : area
633) cs_nnd3n02c_sl (ncount 27 : area 108)
cs_nnd4n03c_sl (ncount 8 : area 40) cs_nor2n02c_sl (ncount 13 : area
39) cs_nor3n03c_sl (ncount 2 : area 8)
cs_oa21n03c_sl (ncount 3 : area 15) cs_oa22n03c_sl (ncount 1 : area
6) cs_xbn2n01b_sl (ncount 1 : area 8)
cs_xbo2n01b_sl (ncount 1 : area 8) Total Area = 1961 (Comb = 1411 :
Non-Comb = 550) > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Report for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:54:11 1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer
EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.
```

Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----

Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup
Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold
Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```
----- 1 dcd_succ_last F C3+R 1385 -506 71 1116 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1385 -506 71 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1338
-506 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1338 -506 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1275 -506 66 1303 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 63 N1098 ----> C2734rwr/y F C3+R 1275 -506 66
1303 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
R C3+R 1234 -506 99 439 1 cs_invvn01c_sl cs_invvn01c_sl 41 N1097 ---->
C2728rwr/y R C3+R 1234 -506 99 439 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a F C3+R 1180 -506 83
171 2 cs_invvn01c_sl cs_invvn01c_sl 54 N1692 ---->{b} C2725rwr/y
F C3+R 1180 -506 83 171 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a R C3+R 1120 -506 188 306 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 60 N1479 ---->{c} C2721rwr/y R C3+R 1120 -506
188 306 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/b
F C3+R 1012 -506 110 162 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 108 N1497 ---->{d}
C2709rwr/y F C3+R 1012 -506 110 162 2 cs_nor3n03c_sl
cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a R C3+R 946 -506 129
54 1 cs_nor3n03c_sl cs_nor3n03c_sl 66 N1986 ---->{e} C2677rwr/y
R C3+R 946 -506 129 54 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1986 ---->
F C3+R 882 -506 59 49 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 64 N1094
---->{f} C2909/y F C3+R 882 -506 59 49 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1094 ----> C2909/b R C3+R 850 -506 80
78 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 32 dcd_mcr41_blk ----> dcd_mcr41_blk
R C3+R 850 -506 80 78 1 PI 0 dcd_mcr41_blk
```

```
----- 2 dcd_succ_last R C3+R 1423 -494 108 1116 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1423 -494 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1365
-494 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1365 -494 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1317 -494 99 1303 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 48 N1098 ----> C2734rwr/y R C3+R 1317 -494
99 1303 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
```

```

F C3+R 1267 -494 66 439 1 cs_invvn01c_sl cs_invvn01c_sl 50 N1097
----> C2728rwr/y F C3+R 1267 -494 66 439 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a R C3+R 1223 -494 118
171 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
R C3+R 1223 -494 118 171 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a F C3+R 1150 -494 135 306 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 73 N1479 ---->{c} C2721rwr/y F C3+R 1150 -494
135 306 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/b
R C3+R 1055 -494 247 162 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 95 N1497 ---->{d}
C2709rwr/y R C3+R 1055 -494 247 162 2 cs_nor3n03c_sl
cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a F C3+R 937 -494 90
54 1 cs_nor3n03c_sl cs_nor3n03c_sl 118 N1986 ---->{e} C2677rwr/y
F C3+R 937 -494 90 54 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1986 ---->
C2677rwr/c R C3+R 883 -494 123 49 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 54 N1719 ---->{f} C2599rwr_0/y R C3+R 883 -494
123 49 2 cs_nor2n02c_sl cs_nor2n02c_sl 0 N1719 ----> C2599rwr_0/a
F C3+R 820 -494 83 35 1 cs_nor2n02c_sl cs_nor2n02c_sl 63 N1942 ---->{g}
nd2n02c_sl cs_nnd2n02c_sl 0 N1942 ----> C2349rwr_0_0_0/a R
C3+R 768 -494 118 22 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N288 ---->{h}
C2339/y R C3+R 768 -494 118 22 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N288 ----> C2339/a F C3+R 706 -494 83
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 NET690 ---->{i} C2187/y
F C3+R 706 -494 83 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 NET690 ---->
C2187/a R C3+R 656 -494 108 32 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 51 N29 ----> C2020/y R C3+R 656 -494 108
32 2 cs_invvn01c_sl cs_invvn01c_sl 0 N29 ----> C2020/a F
C3+R 557 -494 424 19 1 cs_invvn01c_sl cs_invvn01c_sl 99 du_iu_hold_aa_req
----> du_iu_hold_aa_req F C3+R 557 -494 424 19 1 PI
0 du_iu_hold_aa_req

```

```

-----
> report_area Design: /IDCDSUC - Area: 5092.879883, Area(Weight):
1267.547363 > cputime Used 27.17 cpu seconds or 00:00:27 wall time, used 327680 bytes
or 320 kbytes. > report_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap
violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap
violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet du_iu_store_status(2):a
has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500,
limit 455 INet eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier 1 RISE:
transition 500, limit 455; FALL: transition 500, limit 455 INet iu_reset_op_c:y has cap violation
1.219, load 1219, limit 1000, multiplier 1 slack 140.6 INet dcd_succ_last_t1:y has cap violation
1.115, load 1116, limit 1001, multiplier 1 slack -506.3 INet iu_reset_all:y has cap violation 1.328,
load 796.6, limit 600, multiplier 1 slack 339 INet N22:y has cap violation 1.204, load 1205, limit
1001, multiplier 1 slack 618 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier
1 slack 394.3 INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 618
INet N134:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 357.2 INet N158:y
has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 630.3 INet N1098:y has cap
violation 1.302, load 1303, limit 1001, multiplier 1 slack -506.3 IDesign IDCDSUC has 13 violations
> cpr_eval > echo {In restructure loop} In restructure loop > echo
-493.216553684 -493.216553684 > echo -506.313720703 -506.313720703 >
freeze_net_loads -reset [TIMER-6411]: Unasserted load on 369 inet(s). > load_update
-invalidate > gbfo_assign_gain -gain 5.0 [load_update]: Number of pin load calculations: 6881
since last stats [load_update]: Number of pin weight calculations: 0 since last stats Assign Gain
Area : before 5092.88 after 4486.86 (11.90 %) Slack : before -506.3137 after -812.2559 (-60.43 %)
Cell : before 773 after 773 (0.00 %) Time : 2.590000 > check_slack_cont [cr]: (W): pin: c
in: c (cell: C2457) has invalid rise/fall slack: 1.134e+38. [cr]: (W): pin: a (cell: C2630) has invalid rise/fall
slack: 1.134e+38. [cr]: (W): pin: a (cell: C2630) has invalid rise/fall slack: 1.134e+38. >

```

gbfo_fancorr -check -use_max_load -aggressive -max_buffe... [GB-103]: noninverting buffers are absent
 Fanout Corr Area : before 4486.86 after 4502.64 (-0.35 %) Slack : before -812.2559 after -812.2559
 (0.00 %) Cell : before 773 after 787 (-1.81 %) Time : 4.870000 > report_gain_violations
 -min 1.0 -max 10.0 ----- Gain Violation Report for design IDCDSUC

Design	Type	Gain	Cell Name
> report_drc Checking DRC for IDesign IDCDSUC			
INet clkg:clkg	has cap violation	1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38	INet
clkg2:clkg2	has cap violation	1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38	INet
du_iu_store_status(2):a	has transition violation	1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit 455	INet eu_iu_srlz_op_encode(11):a
dcd_succ_last_t1:y	has cap violation	1.083, load 1084, limit 1001, multiplier 1 slack -812.3	INet
srlz_nomatch_q:l2_out_n	has cap violation	1.096, load 270.7, limit 247, multiplier 1 slack 258.2	INet
dcd_succ_dly_q:l2_out_n	has cap violation	2.503, load 618.4, limit 247, multiplier 1 slack 68.9	INet
dcd_succ_dly_q:a	has transition violation	1.094, multiplier 1 RISE: transition 497.9, limit 455; FALL: transition 400.4, limit 455	INet
slow_mode_t2_q:l2_out_n	has cap violation	1.018, load 251.4, limit 247, multiplier 1 slack 502.4	INet
N22:y	has cap violation	1.204, load 1205, limit 1001, multiplier 1 slack 502.4	INet
N26:y	has cap violation	1.216, load 1218, limit 1001, multiplier 1 slack 258.2	INet
N36:y	has cap violation	1.179, load 1180, limit 1001, multiplier 1 slack 509.2	INet
N1098:y	has cap violation	1.225, load 1227, limit 1001, multiplier 1 slack -812.3	INet
gbfonet_2:y	has cap violation	1.218, load 1219, limit 1001, multiplier 1 slack -229	INet
gbfonet_15:y	has cap violation	1.169, load 1170, limit 1001, multiplier 1 slack 68.9	INet
gbfonet_16:y	has cap violation	1.108, load 1109, limit 1001, multiplier 1 slack 467.6	IDesign
IDCDSUC has 16 violations > echo {Custom Synzilla Report} Custom Synzilla Report			

> ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0 upcells 122 IN ports 73 OUT ports
 787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC) 0 buses 1008 nets (0 multiply-driven; 0 undriven)
 2632 pins (0 inversions) 2.61 pins per net 1551 literals
 21 levels 10 max fanin 15 max fanout Cell Information

FUNC_STRAIGHT_WIRE_DESIGN (ncount 180: area 0)	PSEUDO_REG (ncount 83: area 0)
cb_clk_32_1 (ncount 70)	6: area 480
cb_mode_block (ncount 24)	cs_ao12n03c_sl (ncount 6: area 96)
cs_ao22n03c_sl (ncount 16: area 454)	cs_nnd2n02c_sl (ncount 211: area 108)
cs_invvn01c_sl (ncount 8: area 40)	cs_nnd4n03c_sl (ncount 13: area 8)
cs_nnd3n02c_sl (ncount 27: area 8)	cs_nor3n03c_sl (ncount 2: area 15)
cs_nnd4n03c_sl (ncount 3: area 8)	cs_ao22n03c_sl (ncount 1: area 8)
cs_xbn2n01b_sl (ncount 1: area 8)	
cs_xbo2n01b_sl (ncount 1: area 8)	

Total Area = 1989 (Comb = 1439: Non-Comb = 550)
 > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint 0019]:<End.....New Endpoint Report. Sun Apr 18 21:54:26 1999 Part : IDCDSUC Mode : Late Mode / Nominal
 EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
 Max. Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT		(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST) Clock Gating Hold
ClkGHld		(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width
ClkTPW		(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup
Setup		(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold
Hold		(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC		(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth
ClkPW		(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```

-----
1 eu_dsbl_aftr.reg_n.lat_0/BASE_REG/a F C3+R 2133 -812 0
27 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup eu_dsbl_aftr.reg_n.lat_0/BASE_REG/c1
F C3+R 160 60 221 13 cl_invvn 05d 1200 c1 ---->
eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 2133 -812 0 27 1 AND
AND 0 DELAY ----> eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 2181
-812 132 16 1 AND AND -48 a ----> eu_dsbl_aftr.reg_n.lat_0/a
R C3+R 2181 -812 132 16 1 PSEUDO_REG PSEUDO_REG 0 a ---->
C2874/y R C3+R 2181 -812 132 16 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N145 ----> C2874/a F C3+R 2103 -812 109
16 1 cs_invvn01c_sl cs_invvn01c_sl 78 N1013 ---->{a} C2856/y F
C3+R 2103 -812 109 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1013 ---->
C2856/b R C3+R 2033 -812 156 17 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 70 N522 ---->{b} C2833/y R C3+R 2033 -812 156
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N522 ----> C2833/b F
87 N1290 ----> C2800/y F C3+R 1945 -812 86 233 14
cs_invvn01c_sl cs_invvn01c_sl 0 N1290 ----> C2800/a R C3+R
1882 -812 156 57 1 cs_invvn01c_sl cs_invvn01c_sl 63 N1648 ---->{c} C2779/y
R C3+R 1882 -812 156 57 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1648 ---->
C2779/a F C3+R 1795 -812 109 22 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 87 NET803 ---->{d} C2759/y F C3+R 1795 -812
109 22 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 NET803 ----> C2759/a
R C3+R 1724 -812 132 1084 7 cs_nnd2n02c_sl cs_nnd2n02c_sl 71
dcd_succ_last_t1 ----> C2744/y R C3+R 1724 -812 132 1084 7
cs_invvn01c_sl cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
F C3+R 1646 -812 109 277 4 cs_invvn01c_sl cs_invvn01c_sl 78 N675 ---->{e}
C2738/y F C3+R 1646 -812 109 277 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N675 ----> C2738/b R C3+R 1578 -812 132
1227 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1098 ----> C2734rwr/y
R C3+R 1578 -812 132 1227 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ---->
C2734rwr/a F C3+R 1506 -812 86 256 1 cs_invvn01c_sl
cs_invvn01c_sl 72 N1097 ----> C2728rwr/y F C3+R 1506 -812 86
256 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1097 ----> C2728rwr/a
R C3+R 1443 -812 156 78 2 cs_invvn01c_sl cs_invvn01c_sl 63 N1692 ---->{f}
C2725rwr/y R C3+R 1443 -812 156 78 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a F C3+R 1350 -812 132
162 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 93 N1479 ---->{g} C2721rwr/y
F C3+R 1350 -812 132 162 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
C2721rwr/b R C3+R 1253 -812 295 90 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 97 N1497 ---->{h} C2709rwr/y R C3+R 1253 -812
295 90 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a
F C3+R 1102 -812 132 29 1 cs_nor3n03c_sl cs_nor3n03c_sl 151 N1986 ---->{i}
C2677rwr/y F C3+R 1102 -812 132 29 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl 0 N1986 ----> C2677rwr/c R C3+R 1019 -812
208 33 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 83 N1719 ---->{j} C2599rwr_0/y
R C3+R 1019 -812 208 33 2 cs_nor2n02c_sl cs_nor2n02c_sl 0 N1719 ---->
C2599rwr_0/a F C3+R 907 -812 109 17 1 cs_nor2n02c_sl
cs_nor2n02c_sl 112 N1942 ---->{k} C2349rwr_0_0_0/y F C3+R 907 -812
R C3+R 832 -812 156 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 75

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N288 ---->{l} C2339/y R C3+R 832 -812 156 17 1 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 0 N288 ----> C2339/a F C3+R 744 -812 109
 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 87 NET690 ---->{m} C2187/y
 F C3+R 744 -812 109 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 NET690 ---->
 C2187/a R C3+R 673 -812 132 32 2 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 71 N29 ----> C2020/y R C3+R 673 -812 132
 32 2 cs_invvn01c_sl cs_invvn01c_sl 0 N29 ----> C2020/a F
 C3+R 557 -812 424 17 1 cs_invvn01c_sl cs_invvn01c_sl 116 du_iu_hold_aa_req
 ----> du_iu_hold_aa_req F C3+R 557 -812 424 17 1 PI
 0 du_iu_hold_aa_req

----- 2 eu_frc_milli.reg_n.lat_0/BASE_REG/a F C3+R 2133 -812 0
 27 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup eu_frc_milli.reg_n.lat_0/BASE_REG/c1
 F C3- 160 60 238 14 cl_invvn 05d 1200 c1 ---->
 eu_frc_milli.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 2133 -812 0 27 1 AND
 AND 0 DELAY ----> eu_frc_milli.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 2181 -812
 132 16 1 AND AND -48 a ----> eu_frc_milli.reg_n.lat_0/a R C3+R
 2181 -812 132 16 1 PSEUDO_REG PSEUDO_REG 0 a ----> C2875/y
 R C3+R 2181 -812 132 16 1 cs_invvn01c_sl cs_invvn01c_sl 0 N101 ---->
 C2875/a F C3+R 2103 -812 109 16 1 cs_invvn01c_sl
 cs_invvn01c_sl 78 N994 ---->{a} C2857/y F C3+R 2103 -812 109
 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N994 ----> C2857/b R
 C3+R 2033 -812 156 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 70 N505 ---->{b}
 C2834/y R C3+R 2033 -812 156 17 1 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 0 N505 ----> C2834/b F C3+R 1945 -812 86
 233 14 cs_nnd2n02c_sl cs_nnd2n02c_sl 87 N1290 ----> C2800/y
 F C3+R 1945 -812 86 233 14 cs_invvn01c_sl cs_invvn01c_sl 0 N1290 ---->
 C2800/a R C3+R 1882 -812 156 57 1 cs_invvn01c_sl
 cs_invvn01c_sl 63 N1648 ---->{c} C2779/y R C3+R 1882 -812 156
 57 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1648 ----> C2779/a
 F C3+R 1795 -812 109 22 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 87 NET803 ---->{d}
 C2759/y F C3+R 1795 -812 109 22 1 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 0 NET803 ----> C2759/a R C3+R 1724 -812
 nnd2n02c_sl 71 dcd_succ_last_t1 ----> C2744/y R C3+R 1724 -812
 132 1084 7 cs_invvn01c_sl cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
 F C3+R 1646 -812 109 277 4 cs_invvn01c_sl cs_invvn01c_sl 78 N675 ---->{e}
 C2738/y F C3+R 1646 -812 109 277 4 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 0 N675 ----> C2738/b R C3+R 1578 -812 132
 1227 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1098 ----> C2734rwr/y
 R C3+R 1578 -812 132 1227 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ---->
 C2734rwr/a F C3+R 1506 -812 86 256 1 cs_invvn01c_sl
 cs_invvn01c_sl 72 N1097 ----> C2728rwr/y F C3+R 1506 -812 86
 256 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1097 ----> C2728rwr/a
 R C3+R 1443 -812 156 78 2 cs_invvn01c_sl cs_invvn01c_sl 63 N1692 ---->{f}
 C2725rwr/y R C3+R 1443 -812 156 78 2 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a F C3+R 1350 -812 132
 162 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 93 N1479 ---->{g} C2721rwr/y
 F C3+R 1350 -812 132 162 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
 C2721rwr/b R C3+R 1253 -812 295 90 2 cs_nnd3n02c_sl
 cs_nnd3n02c_sl 97 N1497 ---->{h} C2709rwr/y R C3+R 1253 -812
 295 90 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a
 F C3+R 1102 -812 132 29 1 cs_nor3n03c_sl cs_nor3n03c_sl 151 N1986 ---->{i}
 C2677rwr/y F C3+R 1102 -812 132 29 1 cs_nnd3n02c_sl
 cs_nnd3n02c_sl 0 N1986 ----> C2677rwr/c R C3+R 1019 -812
 208 33 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 83 N1719 ---->{j} C2599rwr_0/y

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R C3+R 1019 -812 208 33 2 cs_nor2n02c_sl cs_nor2n02c_sl 0 N1719 ---->
C2599rwr_0/a F C3+R 907 -812 109 17 1 cs_nor2n02c_sl
cs_nor2n02c_sl 112 N1942 ---->{k} C2349rwr_0_0_0/y F C3+R 907 -812
109 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1942 ----> C2349rwr_0_0_0/a
R C3+R 832 -812 156 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 75 N288 ---->{l}
C2339/y R C3+R 832 -812 156 17 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N288 ----> C2339/a F C3+R 744 -812 109
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 87 NET690 ---->{m} C2187/y
F C3+R 744 -812 109 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 NET690 ---->
C2187/a R C3+R 673 -812 132 32 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 71 N29 ----> C2020/y R C3+R 673 -812 132
F C3+R 557 -812 424 17 1 cs_inwn01c_sl cs_inwn01c_sl 116
du_iu_hold_aa_req ----> du_iu_hold_aa_req F C3+R 557 -812 424 17
1 PI 0 du_iu_hold_aa_req

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> report_area Design: /IDCDSUC - Area: 4502.641602, Area(Weight):
1284.131592 > cputime Used 14.86 cpu seconds or 00:00:15 wall time, used 0 bytes or 0
byte. > gbfo_tune_gain -target_frac 1.0 -gain_incr 0.03 -gain_de... Tune Gain Area : before
4502.64 after 4352.61 (3.33 %) Slack : before -812.2559 after -680.5689 (16.21 %) Cell : before
787 after 787 (0.00 %) Time : 46.970000 > gbfo_tune_gain -target_frac 0.95 -gain_incr
0.05 -gain_d... C2734rwr new rep load 319.6 greater than max 300.2: set to max: FREEZE SIZEUP
C2738 new rep load 101.9 greater than max 96.3: set to max: FREEZE SIZEUP C2721rwr new rep load
62.36 greater than max 61.93: set to max: FREEZE SIZEUP C2709rwr new rep load 43.54 greater than
max 42.11: set to max: FREEZE SIZEUP C2550 new rep load 42.06 greater than max 39.67: set to
max: FREEZE SIZEUP C2906 new rep load 69.02 greater than max 64.9: set to max: FREEZE SIZEUP
Tune Gain Area : before 4352.61 after 4474.51 (-2.80 %) Slack : before -680.5689 after -446.0240
(34.46 %) Cell : before 787 after 787 (0.00 %) Time : 20.930000 > cpr_eval
> resize -examine 5 -trace 10 -local -mincut -inc -sequent... resize Area : before 4474.51 after
4474.51 (0.00 %) Slack : before -446.0240 after -446.0240 (0.00 %) Cell : before 787 after 787
(0.00 %) Time : 1.780000 > load_update -invalidate > swap_pins
-examine 5 -est -ana 10000 -exe 1000 -per 10 -... [load_update]: Number of pin load calculations: 57353
since last stats [load_update]: Number of pin weight calculations: 0 since last stats [SWAP-8603]:
Swapping pins (mode=BACK) for: IDESIGN:/IDCDSUC Note: Swapped 16 pins on 8 cells in 1 Passes.
swap Area : before 4474.51 after 4475.36 (-0.02 %) Slack : before -446.0240 after -441.6489
(0.98 %) Cell : before 787 after 787 (0.00 %) Time : 2.560000 > reset_timing_area
> tgfs_redund -effort 50 > cputime { tgfs_rewire -tech -$rwr_effort } >
tgfs_rewire -tech -medium tgfs rewiring Area : before 4475.36 after 4531.42 (-1.25 %)
Slack : before -441.6489 after -441.6489 (0.00 %) Cell : before 787 after 787 (0.00 %) Time :
14.330000 Used 17.42 cpu seconds or 00:00:18 wall time, used 0 bytes or 0 byte. >
report_drc Checking DRC for IDesign IDCDSUC INet op_mcend_raw:op_mcend_raw has cap violation
1.08, load 152.2, limit 141, multiplier 1 slack -419.7 INet clkg:clkg has cap violation 1.032, load
145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5,
limit 141, multiplier 1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099,
multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet
eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit
455; FALL: transition 500, limit 455 INet dcd_succ_last_t1:y has cap violation 1.078, load 1079,
limit 1001, multiplier 1 slack -441.6 INet frc_blk_1cyc_q:l2_out_n has cap violation 1.097, load
270.9, limit 247, multiplier 1 slack -198.7 INet N22:y has cap violation 1.204, load 1205, limit
1001, multiplier 1 slack 614.7 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier
0, limit 1001, multiplier 1 slack 616.3 INet N1098:y has cap violation 1.26, load 1261, limit 1001,
multiplier 1 slack -441.6 INet gbfontet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier
1 slack 28.61 INet gbfontet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack
343.9 INet gbfontet_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 477.9
IDesign IDCDSUC has 14 violations > write_end_point_report -points 3
[ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.

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[ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:56:11 1999 Part : IDCDSUC Mode : Late
 Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
 Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
 Max. Endpoints: 3 Cause of Slack Abbreviation Comparison/Description -----

----- Slack Continuation SlkCont Slack due to a point downstream on
 path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
 Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
 Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
 GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
 CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
 (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
 (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
 EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
 SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
 ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
 ATLimit Slack discontinuity due to failed test Num/
 LimitedAT/ Delay/ Failed Test/ Test PinName
 E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

----- 1 dcd_succ_last F C3+R 1321 -442 81 1079 7
 PO 0 dcd_succ_last_t1 RAT 879
 0 ----> C2744/y F C3+R 1321 -442 81 1079 7 cs_invvn01c_sl
 cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1266
 -442 121 301 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ----> {a} C2738/y
 R C3+R 1266 -442 121 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
 C2738/b F C3+R 1198 -442 79 1261 4 cs_nnd2n02c_sl
 cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y F C3+R 1198 -442 79
 c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a R C3+R 1151
 -442 87 306 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1097 ----> C2728rwr/y
 R C3+R 1151 -442 87 306 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1097 ---->
 C2728rwr/a F C3+R 1107 -442 70 165 2 cs_invvn01c_sl
 cs_invvn01c_sl 44 N1692 ----> {b} C2725rwr/y F C3+R 1107 -442 70
 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a
 R C3+R 1060 -442 140 161 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 46 N1479 ----> {c}
 C2721rwr/y R C3+R 1060 -442 140 161 2 cs_nnd3n02c_sl
 cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/b F C3+R 980 -442 100
 65 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 81 N1858 ----> {d} C2550/y
 F C3+R 980 -442 100 65 1 cs_ao22n03c_sl cs_ao22n03c_sl 0 N1858 ---->
 C2550/a2 R C3+R 935 -442 86 48 1 cs_ao22n03c_sl
 cs_ao22n03c_sl 44 N1437 ----> C2427rwr/y R C3+R 935 -442 86
 48 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1437 ----> C2427rwr/a F
 C3+R 893 -442 62 32 1 cs_invvn01c_sl cs_invvn01c_sl 42 N1717 ----> C1982/y
 F C3+R 893 -442 62 32 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1717 ---->
 C1982/a R C3+R 858 -442 80 87 3 cs_invvn01c_sl
 cs_invvn01c_sl 35 op_cmp_raw ----> op_cmp_raw R C3+R 858 -442
 80 87 3 PI 0 op_cmp_raw

----- 2 dcd_succ_last R C3+R 1353 -424 123 1079 7
 PO 0 dcd_succ_last_t1 RAT 929
 0 ----> C2744/y R C3+R 1353 -424 123 1079 7 cs_invvn01c_sl
 cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1286
 -424 85 301 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ----> {a} C2738/y

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F C3+R 1286 -424 85 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1234 -424 120 1261 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 52 N1098 ----> C2734rwr/y R C3+R 1234 -424
120 1261 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
F C3+R 1175 -424 59 306 1 cs_invvn01c_sl cs_invvn01c_sl 59 N1097 ---->
C2728rwr/y F C3+R 1175 -424 59 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a R C3+R 1139 -424 101
R C3+R 1139 -424 101 165 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a F C3+R 1084 -424 98
161 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 55 N1479 ---->{c} C2721rwr/y
F C3+R 1084 -424 98 161 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
C2721rwr/a R C3+R 1017 -424 184 127 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 67 N1497 ---->{d} C2709rwr/y R C3+R 1017 -424
184 127 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1497 ----> C2709rwr/b
F C3+R 916 -424 97 80 2 cs_nor3n03c_sl cs_nor3n03c_sl 101 N1781
---->{e} C2885/y F C3+R 916 -424 97 80 2 cs_nnd4n03c_sl
cs_nnd4n03c_sl 0 N1781 ----> C2885/c R C3+R 850 -424 224
52 1 cs_nnd4n03c_sl cs_nnd4n03c_sl 66 N1999 ---->{f} C2889/y
R C3+R 850 -424 224 52 1 cs_oa21n03c_sl cs_oa21n03c_sl 0 N1999 ---->
C2889/b F C3+R 749 -424 57 19 1 cs_oa21n03c_sl
cs_oa21n03c_sl 101 N2000 ----> C2890rwr/y F C3+R 749 -424 57
19 1 cs_invvn01c_sl cs_invvn01c_sl 0 N2000 ----> C2890rwr/a R
C3+R 716 -424 91 20 1 cs_invvn01c_sl cs_invvn01c_sl 33 N2005 ---->{g}
C2891rwr/y R C3+R 716 -424 91 20 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N2005 ----> C2891rwr/b F C3+R 670 -424 53
114 6 cs_nnd2n02c_sl cs_nnd2n02c_sl 46 NET981 ----> C2077/y
F C3+R 670 -424 53 114 6 cs_invvn01c_sl cs_invvn01c_sl 0 NET981 ---->
C2077/a R C3+R 637 -424 116 137 3 cs_invvn01c_sl
cs_invvn01c_sl 33 iq_empty ----> iq_empty R C3+R 637 -424
116 137 3 PI 0 iq_empty

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3 slow_mode_blk.reg_n.lat_0/BASE_REG/a F C3+R 1729 -408
0 29 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3+R 160 60 238 14 cl_invvn
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1729
-408 0 29 1 AND AND 0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1777 -408 105 16 1 AND
AND -48 a ----> slow_mode_blk.reg_n.lat_0/a R C3+R 1777 -408 105 16
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y R C3+R
1777 -408 105 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N95 ----> C2841/a
F C3+R 1725 -408 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b}
cs_nnd2n02c_sl 0 N935 ----> C2821/b R C3+R 1681 -408
107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 45 N512 ---->{c} C2798/y
R C3+R 1681 -408 107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N512 ---->
C2798/a F C3+R 1624 -408 89 35 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 57 N1527 ----> C2778/y F C3+R 1624 -408 89
35 2 cs_invvn01c_sl cs_invvn01c_sl 0 N1527 ----> C2778/a R
C3+R 1554 -408 192 67 4 cs_invvn01c_sl cs_invvn01c_sl 70 N931 ---->{d}
C2754/y R C3+R 1554 -408 192 67 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N931 ----> C2754/b F C3+R 1445 -408 101
86 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 109 N1555 ----> C2588/y
F C3+R 1445 -408 101 86 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1555 ---->
C2588/a R C3+R 1378 -408 117 23 1 cs_invvn01c_sl
cs_invvn01c_sl 67 N1730 ---->{e} C2554/y R C3+R 1378 -408 117
23 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1730 ----> C2554/b

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F C3+R 1313 -408 77 84 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 66 N1652 ---->
C2464/y F C3+R 1313 -408 77 84 5 cs_invvn01c_sl
cs_invvn01c_sl 0 N1652 ----> C2464/a R C3+R 1261 -408 120
30 1 cs_invvn01c_sl cs_invvn01c_sl 52 N1749 ---->{f} C2412/y R
C3+R 1261 -408 120 30 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1749 ---->
C2412/a F C3+R 1211 -408 56 27 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl 50 N1713 ----> C1954/y F C3+R 1211 -408 56
27 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1713 ----> C1954/a R
C3+R 1171 -408 175 45 2 cs_invvn01c_sl cs_invvn01c_sl 40 br_wrong_targ ---->
br_wrong_targ R C3+R 1171 -408 175 45 2 PI
0 br_wrong_targ

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> gbfo_tune_gain -target_frac 0.97 -gain_incr 0.05 -gain_d... C2734rwr
new rep load 313.2 greater than max 300.2: set to max: FREEZE SIZEUP C2738 new rep load 99.96
greater than max 96.3: set to max: FREEZE SIZEUP C2909 new rep load 98.53 greater than max
96.3: set to max: FREEZE SIZEUP C2721rwr new rep load 64.15 greater than max 61.93: set to max:
FREEZE SIZEUP C2917 new rep load 99.33 greater than max 96.3: set to max: FREEZE SIZEUP
Tune Gain Area : before 4531.42 after 4432.62 (2.18 %) Slack : before -441.6489 after -433.9434
(1.74 %) Cell : before 787 after 787 (0.00 %) Time : 12.060000 >
write_end_point_report -points 3 [ET-0018]:>Begin...New EndPoint Report for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:56:25
1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA Einstimer EndPoint Report
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 3 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName
-----

```

```

-----
1 dcd_succ_last F C3+R 1313 -434 81 1078 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1313 -434 81 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1259
-434 121 301 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
R C3+R 1259 -434 121 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1191 -434 79 1260 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y F C3+R 1191 -434 79
1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
R C3+R 1143 -434 87 306 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1097 ---->
C2728rwr/y R C3+R 1143 -434 87 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a F C3+R 1099 -434 70
165 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y

```

```

F C3+R 1099 -434 70 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a R C3+R 1053 -434 133 157 2 cs_nnd2n02c_sl
79 ---->{c} C2721rwr/y R C3+R 1053 -434 133 157 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/c F C3+R 979 -434 65
118 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 74 N892 ---->{d} C2338/y
F C3+R 979 -434 65 118 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N892 ---->
C2338/a R C3+R 943 -434 81 125 3 cs_nnd2n02c_sl
cs_nnd2n02c_sl 36 N1119 ----> C2905/y R C3+R 943 -434 81
125 3 cs_invvn01c_sl cs_invvn01c_sl 0 N1119 ----> C2905/a F
C3+R 903 -434 68 92 1 cs_invvn01c_sl cs_invvn01c_sl 41 N2010 ---->{e}
C2906/y F C3+R 903 -434 68 92 1 cs_nor2n02c_sl
cs_nor2n02c_sl 0 N2010 ----> C2906/a R C3+R 868 -434 80
74 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc ----> dcd_blk_dsucc
R C3+R 868 -434 80 74 1 PI 0 dcd_blk_dsucc

```

```

----- 2 slow_mode_blk.reg_n.lat_0/BASE_REG/a F C3+R 1741 -421
0 29 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3- 160 60 238 14 cl_invvn
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1741
-421 0 29 1 AND AND 0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1789 -421 105 16 1 AND
AND -48 a ----> slow_mode_blk.reg_n.lat_0/a R C3+R 1789 -421 105 16
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y R C3+R
1789 -421 105 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N95 ----> C2841/a
F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b}
C2821/y F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N935 ----> C2821/b R C3+R 1693 -421 107
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 45 N512 ---->{c} C2798/y
R C3+R 1693 -421 107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N512 ---->
C2798/a F C3+R 1636 -421 92 35 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 57 N1527 ----> C2778/y F C3+R 1636 -421 92
35 2 cs_invvn01c_sl cs_invvn01c_sl 0 N1527 ----> C2778/a R
C3+R 1563 -421 198 67 4 cs_invvn01c_sl cs_invvn01c_sl 72 N931 ---->{d}
C2754/y R C3+R 1563 -421 198 67 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N931 ----> C2754/b F C3+R 1450 -421 104
86 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 113 N1555 ----> C2588/y
cs_invvn01c_sl cs_invvn01c_sl 0 N1555 ----> C2588/a R C3+R
1381 -421 120 23 1 cs_invvn01c_sl cs_invvn01c_sl 69 N1730 ---->{e} C2554/y
R C3+R 1381 -421 120 23 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1730 ---->
C2554/b F C3+R 1313 -421 79 84 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1652 ----> C2464/y F C3+R 1313 -421 79
84 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1652 ----> C2464/a R
C3+R 1260 -421 120 29 1 cs_invvn01c_sl cs_invvn01c_sl 53 N1749
---->{f} C2412/y R C3+R 1260 -421 120 29 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl 0 N1749 ----> C2412/a F C3+R 1210 -421 55
27 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 50 N1713 ----> C1954/y
F C3+R 1210 -421 55 27 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1713 ---->
C1954/a R C3+R 1171 -421 175 46 2 cs_invvn01c_sl
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ R C3+R 1171
-421 175 46 2 PI 0 br_wrong_targ

```

```

----- 3 dcd_succ_last R C3+R 1349 -420 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1349 -420 123 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1282

```

```

-420 85 301 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
F C3+R 1282 -420 85 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1230 -420 120 1260 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 52 N1098 ----> C2734rwr/y R C3+R 1230 -420
120 1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
F C3+R 1171 -420 59 306 1 cs_invvn01c_sl cs_invvn01c_sl 59 N1097 ---->
C2728rwr/y F C3+R 1171 -420 59 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a R C3+R 1135 -420 101
165 2 cs_invvn01c_sl cs_invvn01c_sl 36 N1692 ---->{b} C2725rwr/y
R C3+R 1135 -420 101 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a F C3+R 1081 -420 93 157 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 54 N1479 ---->{c} C2721rwr/y F C3+R 1081 -420
93-157-2-cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/a
->{d} C2709rwr/y R C3+R 1015 -420 214 120 2 cs_nor3n03c_sl
cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a F C3+R 920 -420 59
51 1 cs_nor3n03c_sl cs_nor3n03c_sl 95 N1986 ---->{e} C2677rwr_0/y
F C3+R 920 -420 59 51 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1986 ---->
C2677rwr_0/b R C3+R 887 -420 90 97 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 33 N1094 ---->{f} C2909/y R C3+R 887 -420 90
97 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1094 ----> C2909/b
F C3+R 835 -420 80 90 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 dcd_mcr41_blk
----> dcd_mcr41_blk F C3+R 835 -420 80 90 1 PI
0 dcd_mcr41_blk

```

```

-----
> report_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has
cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap
violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet du_iu_store_status(2):a
has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500,
limit 455 INet eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier 1 RISE:
transition 500, limit 455; FALL: transition 500, limit 455 INet dcd_succ_last_t1:y has cap violation
1.077, load 1078, limit 1001, multiplier 1 slack -433.9 INet frc_blk_1cyc_q:l2_out_n has cap
violation 1.008, load 248.9, limit 247, multiplier 1 slack -224.9 INet N22:y has cap violation 1.204,
load 1205, limit 1001, multiplier 1 slack 604.5 INet N26:y has cap violation 1.216, load 1218,
limit 1001, multiplier 1 slack 370.7 INet N36:y has cap violation 1.179, load 1180, limit 1001,
multiplier 1 slack 606.1 INet N1098:y has cap violation 1.258, load 1260, limit 1001, multiplier
1 slack -433.9 INet gbfonet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier 1 slack
27.29 INet gbfonet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 337.3
INet gbfonet_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 477.9 IDesign
IDCDSUC has 13 violations
> report_gain_violations -min 1.0 -max 10.0

```

Gain Violation Report for design IDCDSUC

Design	Type	Gain	Cell Name
0.672053 C2894	cs_nnd2n02c_sl Max	10.196948 C2194	cs_invvn01c_sl Min
12.994584 C2907	cs_invvn01c_sl Max	13.197469 C2895	cs_invvn01c_sl Max
0.719591 C2677rwr_0	cs_nnd2n02c_sl	12.966053 C2918	cs_nor2n02c_sl Min

```

> trace::set -group critflow -how_many
> trace::set -group trestruct -where_what > tc::trestruct -sizeless -leaf_flex 1.02 -gain 5
-load 5 GA_Tree: MinLoad=5.672 MaxLoad=300.341 > tc::critflow -depth 3 -xforms
_CiType_30_31e1e638 Transform: trestruct 0.1 Options: Mode=Sizeless GainBuckets=5
LoadBuckets=5 MinInputs=2 MaxInputs=1024 PartialTree=false
SingleCell=false SlackThreshold=0.000 LeafFlexibility=1.020 Critical Slack = -433.943
GA_Tree: Considering net: dcd_blk_dsucc GA_Tree: Considering net: N2010 GA_Tree: Considering net:
putSlack=-433.943 Area=0.000 Delta Evaluate: A=-11.954|-12.462 S=32.916|21.555 Implementing best
tree. Delta Results: Slack=-21.268 InputSlack=-21.268 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: N892 Working on tree: 'N892' Inputs=2 A=962.086|979.016 S=93.872|65.062

```


Slack=-433.943 InputSlack=-433.943 Area=0.000 Delta Evaluate: A=-36.531|-30.189 S=-34.489|-18.359
Implementing best tree. Delta Results: Slack=-44.750 InputSlack=-44.750 Area=0.000 Restoring
original tree. [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
GA_Tree: Considering net: N1479 Working on tree: 'N1479' Inputs=6 A=1053.450|1081.162
S=133.481|92.901 Slack=-433.943 InputSlack=-433.943 Area=0.000 Delta Evaluate: A=-12.015|5.378
S=33.067|28.576 Implementing best tree. Delta Results: Slack=-12.047 InputSlack=-12.047 Area=0.000
Restoring original tree. [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP,
and below. GA_Tree: Considering net: N1692 Working on tree: 'N1692' Inputs=2 A=1135.031|1098.978
S=100.648|70.117 Slack=-433.943 InputSlack=-433.943 Area=0.000 Delta Evaluate:
A=-55.608|-48.063 S=-72.414|-41.996 Implementing best tree. Delta Results: Slack=-63.178
InputSlack=-63.178 Area=0.000 Restoring original tree. [ET-0112]:Deleting timing for design:
sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N1097 GA_Tree:
Considering net: N1098 Working on tree: 'N1098' Inputs=1 A=1229.972|1190.680 S=119.887|78.756
Slack=-433.943 InputSlack=-433.943 Area=0.000 Restoring original tree. [ET-0112]:Deleting timing for
design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N675 Working
on tree: 'N675' Inputs=7 A=1258.629|1281.562 S=121.113|84.932 Slack=-433.943
InputSlack=-433.943 Area=0.000 Delta Evaluate: A=0.072|0.060 S=35.518|32.435 Implementing best
tree. Delta Results: Slack=0.092 InputSlack=0.091 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: dcd_succ_last_t1 Working on tree: 'dcd_succ_last_t1' Inputs=1 A=1348.840|1312.943
S=123.248|80.835 Slack=-433.943 InputSlack=-433.943 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: dcd_mcr41_blk GA_Tree: Considering net: N1094 Working on tree: 'N1094' Inputs=3
A=887.225|884.198 S=90.491|62.574 Slack=-429.858 InputSlack=-429.858 Area=0.000 Delta
Evaluate: A=0.750|0.595 S=37.597|31.491 Implementing best tree. Delta Results: Slack=0.833
InputSlack=0.833 Area=0.000 Restoring original tree. [ET-0112]:Deleting timing for design: sub_design,
analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N1986 GA_Tree: Considering net:
N1497 Working on tree: 'N1497' Inputs=6 A=1015.222|981.022 S=213.506|99.542 Slack=-429.858
InputSlack=-429.858 Area=0.000 Delta Evaluate: A=-23.138|-11.666 S=28.044|53.449 Implementing
best tree. Delta Results: Slack=-32.589 InputSlack=-32.588 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: op_cmp_raw Restoring original tree. [ET-0112]:Deleting timing for design: sub_design,
analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N1717 GA_Tree: Considering net:
N1437 GA_Tree: Considering net: N1858 > reset_timing_area > report_drc
Checking DRC for IDesign IDCDSUC INet clk1:clk1 has cap violation 1.032, load 145.5, limit 141,
multiplier 1 slack 1.134e+38 INet clk2:clk2 has cap violation 1.032, load 145.5, limit 141,
multiplier 1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099, multiplier
1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet eu_iu_srlz_op_encode(11):a
transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit
455 INet dcd_succ_last_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack
-433.9 INet frc_blk_1cyc_q:l2_out_n has cap violation 1.008, load 248.9, limit 247, multiplier 1
slack -203.7 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 614.9
INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier 1 slack 381.3 INet N36:y has
cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 616.2 INet N1098:y has cap violation
1.258, load 1260, limit 1001, multiplier 1 slack -433.9 INet gbfonet_2:y has cap violation 1.218,
load 1219, limit 1001, multiplier 1 slack 27.29 INet gbfonet_15:y has cap violation 1.169, load
1170, limit 1001, multiplier 1 slack 349.9 INet gbfonet_16:y has cap violation 1.108, load 1109,
limit 1001, multiplier 1 slack 478 IDesign IDCDSUC has 13 violations > echo
{Custom Synzilla Report} Custom Synzilla Report > ps -cell Design /HISVHDL/IDCDSUC
has: 1 instances 0 upcells 122 IN ports 73 OUT ports 787 cells (1 AND; 0 XOR; 0
SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC) 0 buses 1008 nets (0 multiply-driven; 0 undriven)
2632 pins (0 inversions) 2.61 pins per net 1551 literals 21 levels 10 max fanin
15 max fanout Cell Information FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area 0) PSEUDO_REG (ncount 83 : area 0)
cb_clk_32_1 (ncount 6 : area 480) cb_mode_block (ncount 1 : area

```

70) cs_ao12n03c_sl (ncount 6 : area 24)
cs_ao22n03c_sl (ncount 16 : area 96) cs_invvn01c_sl (ncount 228 : area
456) cs_nnd2n02c_sl (ncount 208 : area 624)
cs_nnd3n02c_sl (ncount 30 : area 120) cs_nnd4n03c_sl (ncount 7 : area
35) cs_nor2n02c_sl (ncount 13 : area 39)
cs_nor3n03c_sl (ncount 2 : area 8) cs_oa21n03c_sl (ncount 3 : area
15) cs_oa22n03c_sl (ncount 1 : area 6)
cs_xbn2n01b_sl (ncount 1 : area 8) cs_xbo2n01b_sl (ncount 1 : area
8) Total Area = 1989 (Comb = 1439 : Non-Comb = 550)

```

```

write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:56:39

```

```

1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

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```

Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38

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```

Max. Slack: 1.13427E+38 Sort Field: Slack

```

```

Max. Endpoints: 2 Cause of Slack

```

```

Abbreviation Comparison/Description ----- Slack
Continuation SlkCont Slack due to a point downstream on path Required Arrival Time
RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet (
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST) Clock Gating
Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
+ ADJUST) Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH <
CLOCK TRAILING EDGE) Setup Setup (DATA ARRIVAL TIME + SETUP <
CLOCK ARRIVAL TIME + ADJUST) Hold Hold (DATA ARRIVAL TIME - HOLD
> CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC (DATA ARRIVAL TIME
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth ClkPW (CLOCK
(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```

```

----- 1 dcd_succ_last F C3+R 1313 -434 81 1078 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1313 -434 81 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1259
-434 121 301 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
R C3+R 1259 -434 121 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1191 -434 79 1260 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y F C3+R 1191 -434 79
1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
R C3+R 1143 -434 87 306 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1097 ---->
C2728rwr/y R C3+R 1143 -434 87 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a F C3+R 1099 -434 70
165 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
F C3+R 1099 -434 70 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a R C3+R 1053 -434 133 157 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y R C3+R 1053 -434
133 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/c
F C3+R 979 -434 65 118 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 74 N892 ---->{d}
C2338/y F C3+R 979 -434 65 118 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N892 ----> C2338/a R C3+R 943 -434 81
125 3 cs_nnd2n02c_sl cs_nnd2n02c_sl 36 N1119 ----> C2905/y
R C3+R 943 -434 81 125 3 cs_invvn01c_sl cs_invvn01c_sl 0 N1119 ---->
C2905/a F C3+R 903 -434 68 92 1 cs_invvn01c_sl
cs_invvn01c_sl 41 N2010 ---->{e} C2906/y F C3+R 903 -434 68

```

```

92 1 cs_nor2n02c_sl      cs_nor2n02c_sl  0 N2010 ----> C2906/a      R
C3+R   868  -434   80  74 1 cs_nor2n02c_sl      cs_nor2n02c_sl  35 dcd_blk_dsucc ---->
0 dcd_blk_dsucc

```

```

-----
2 slow_mode_blk.reg_n.lat_0/BASE_REG/a      F C3+R   1741  -421
0  29 1 cl_invvn      05d cl_invvn05d  39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1      F C3-   160      60  238 14 cl_invvn
05d      1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT      F C3+R   1741
-421   0  29 1 AND      AND      0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1      R C3+R   1789  -421  105  16 1 AND
AND      -48 a ----> slow_mode_blk.reg_n.lat_0/a      R C3+R   1789  -421  105  16
1 PSEUDO_REG      PSEUDO_REG  0 a ----> {a} C2841/y      R C3+R
1789 -421  105  16 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N95 ----> C2841/a
F C3+R   1738  -421  75  17 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  52 N935 ----> {b}
C2821/y      F C3+R   1738  -421  75  17 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N935 ----> C2821/b      R C3+R   1693  -421  107
17 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  45 N512 ----> {c} C2798/y
R C3+R   1693  -421  107  17 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N512 ---->
C2798/a      F C3+R   1636  -421  92  35 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl  57 N1527 ----> C2778/y      F C3+R   1636  -421  92
35 2 cs_invvn01c_sl      cs_invvn01c_sl  0 N1527 ----> C2778/a      R
C3+R   1563  -421  198  67 4 cs_invvn01c_sl      cs_invvn01c_sl  72 N931 ----> {d}
C2754/y      R C3+R   1563  -421  198  67 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N931 ----> C2754/b      F C3+R   1450  -421  104
86 5 cs_nnd2n02c_sl      cs_nnd2n02c_sl  113 N1555 ----> C2588/y
F C3+R   1450  -421  104  86 5 cs_invvn01c_sl      cs_invvn01c_sl  0 N1555 ---->
C2588/a      R C3+R   1381  -421  120  23 1 cs_invvn01c_sl
cs_invvn01c_sl  69 N1730 ----> {e} C2554/y      R C3+R   1381  -421  120
23 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1730 ----> C2554/b
F C3+R   1313  -421  79  84 5 cs_nnd2n02c_sl      cs_nnd2n02c_sl  68 N1652 ---->
C2464/y      F C3+R   1313  -421  79  84 5 cs_invvn01c_sl
cs_invvn01c_sl  0 N1652 ----> C2464/a      R C3+R   1260  -421  120
29 1 cs_invvn01c_sl      cs_invvn01c_sl  53 N1749
----> {f} C2412/y      R C3+R   1260  -421  120  29 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl  0 N1749 ----> C2412/a      F C3+R   1210  -421  55
27 1 cs_nnd3n02c_sl      cs_nnd3n02c_sl  50 N1713 ----> C1954/y
F C3+R   1210  -421  55  27 1 cs_invvn01c_sl      cs_invvn01c_sl  0 N1713 ---->
C1954/a      R C3+R   1171  -421  175  46 2 cs_invvn01c_sl
cs_invvn01c_sl  39 br_wrong_targ ----> br_wrong_targ      R C3+R   1171
-421  175  46 2 PI      0 br_wrong_targ

```

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-----
> report_area Design: /IDCDSUC - Area: 4432.619141,
Area(Weight): 1283.903442      > cputime Used 129.23 cpu seconds or 00:02:13 wall time,
used 262144 bytes or 256 kbytes.      > cpr_eval      > echo {In gain tuning loop} In
gain tuning loop      > echo -425.923987771 -425.923987771      > echo
-433.943389893 -433.943389893      > report_drc Checking DRC for IDesign IDCDSUC INet
clk1:clk1 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet
clk2:clk2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet
du_iu_store_status(2):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455;
FALL: transition 500, limit 455 INet eu_iu_srlz_op_encode(11):a has transition violation 1.099,
multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet
dcd_succ_last_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -433.9 INet
frb_blk_1cyc_q:l2_out_n has cap violation 1.008, load 248.9, limit 247, multiplier 1 slack -203.7
INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 614.9 INet N26:y has
cap violation 1.216, load 1218, limit 1001, multiplier 1 slack 381.3 INet N36:y has cap violation

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1.179, load 1180, limit 1001, multiplier 1 slack 616.2 INet N1098:y has cap violation 1.258, load 1260, limit 1001, multiplier 1 slack -433.9 INet gbffonet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier 1 slack 27.29 INet gbffonet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 349.9 INet gbffonet_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 478 IDesign IDCDSUC has 13 violations > write_end_point_report

-points 3 [ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:56:42 1999 Part : IDCDSUC Mode : Late
Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 3 Cause of Slack Abbreviation Comparison/Description -----

----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (CLOCK
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
DGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ClkSep (CLOCK1
ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```
-----
1 dcd_succ_last F C3+R 1313 -434 81 1078 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1313 -434 81 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1259
-434 121 301 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
R C3+R 1259 -434 121 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1191 -434 79 1260 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y F C3+R 1191 -434 79
1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
R C3+R 1143 -434 87 306 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1097 ---->
C2728rwr/y R C3+R 1143 -434 87 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a F C3+R 1099 -434 70
165 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
F C3+R 1099 -434 70 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a R C3+R 1053 -434 133 157 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y R C3+R 1053 -434
133 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/c
F C3+R 979 -434 65 118 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 74 N892 ---->{d}
C2338/y F C3+R 979 -434 65 118 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N892 ----> C2338/a R C3+R 943 -434 81
125 3 cs_nnd2n02c_sl cs_nnd2n02c_sl 36 N1119 ----> C2905/y
R C3+R 943 -434 81 125 3 cs_invvn01c_sl cs_invvn01c_sl 0 N1119 ---->
C2905/a F C3+R 903 -434 68 92 1 cs_invvn01c_sl
cs_invvn01c_sl 41 N2010 ---->{e} C2906/y F C3+R 903 -434 68
92 1 cs_nor2n02c_sl cs_nor2n02c_sl 0 N2010 ----> C2906/a R
C3+R 868 -434 80 74 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc ---->
succ R C3+R 868 -434 80 74 1 PI 0
dcd_blk_dsucc
```

```

-----
2 slow_mode_blk.reg_n.lat_0/BASE_REG/a          F C3+R 1741 -421
0 29 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1          F C3- 160 60 238 14 cl_invvn
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1741
-421 0 29 1 AND AND 0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1789 -421 105 16 1 AND
AND -48 a ----> slow_mode_blk.reg_n.lat_0/a R C3+R 1789 -421 105 16
1 PSEUDO_REG PSEUDO_REG 0 a ----> {a} C2841/y R C3+R
1789 -421 105 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N95 ----> C2841/a
F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ----> {b}
C2821/y F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N935 ----> C2821/b R C3+R 1693 -421 107
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 45 N512 ----> {c} C2798/y
R C3+R 1693 -421 107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N512 ---->
C2798/a F C3+R 1636 -421 92 35 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 57 N1527 ----> C2778/y F C3+R 1636 -421 92
35 2 cs_invvn01c_sl cs_invvn01c_sl 0 N1527 ----> C2778/a R
C3+R 1563 -421 198 67 4 cs_invvn01c_sl cs_invvn01c_sl 72 N931 ----> {d}
C2754/y R C3+R 1563 -421 198 67 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N931 ----> C2754/b F C3+R 1450 -421 104
86 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 113 N1555 ----> C2588/y
F C3+R 1450 -421 104 86 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1555 ---->
C2588/a R C3+R 1381 -421 120 23 1 cs_invvn01c_sl
cs_invvn01c_sl 69 N1730 ----> {e} C2554/y R C3+R 1381 -421 120
23 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1730 ----> C2554/b
F C3+R 1313 -421 79 84 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 68 N1652 ---->
C2464/y F C3+R 1313 -421 79 84 5 cs_invvn01c_sl
cs_invvn01c_sl 0 N1652 ----> C2464/a R C3+R 1260 -421 120
29 1 cs_invvn01c_sl cs_invvn01c_sl 53 N1749
----> {f} C2412/y R C3+R 1260 -421 120 29 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl 0 N1749 ----> C2412/a F C3+R 1210 -421 55
27 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 50 N1713 ----> C1954/y
F C3+R 1210 -421 55 27 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1713 ---->
C1954/a R C3+R 1171 -421 175 46 2 cs_invvn01c_sl
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ R C3+R 1171
-421 175 46 2 PI 0 br_wrong_targ
-----

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```

-----
3 dcd_succ_last R C3+R 1349 -420 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1349 -420 123 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1282
-420 85 301 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ----> {a} C2738/y
F C3+R 1282 -420 85 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1230 -420 120 1260 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 52 N1098 ----> C2734rwr/y R C3+R 1230 -420
120 1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
F C3+R 1171 -420 59 306 1 cs_invvn01c_sl cs_invvn01c_sl 59 N1097 ---->
C2728rwr/y F C3+R 1171 -420 59 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a R C3+R 1135 -420 101
165 2 cs_invvn01c_sl cs_invvn01c_sl 36 N1692 ----> {b} C2725rwr/y
R C3+R 1135 -420 101 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a F C3+R 1081 -420 93 157 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 54 N1479 ----> {c} C2721rwr/y F C3+R 1081 -420
93 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/a
-----

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```

R C3+R 1015 -420 214 120 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 66 N1497 ---->{d}
C2709rwr/y R C3+R 1015 -420 214 120 2 cs_nor3n03c_sl
cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a F C3+R 920 -420 59
51 1 cs_nor3n03c_sl cs_nor3n03c_sl 95 N1986 ---->{e} C2677rwr_0/y
F C3+R 920 -420 59 51 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1986 ---->
C2677rwr_0/b R C3+R 887 -420 90 97 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 33 N1094 ---->{f} C2909/y R C3+R 887 -420 90
97 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1094 ----> C2909/b
F C3+R 835 -420 80 90 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 dcd_mcr41_blk
----> dcd_mcr41_blk F C3+R 835 -420 80 90 1 PI
0 dcd_mcr41_blk

```

```

> tgfs_redund -effort 50 > cputime { tgfs_rewire -tech -$rwr_effort } >
tgfs_rewire -tech -high tgfs rewiring Area : before 4432.62 after 4434.25 (-0.04 %) Slack : before
-433.9434 after -433.9434 (0.00 %) Cell : before 787 after 787 (0.00 %) Time : 10.200000 Used
11.55 cpu seconds or 00:00:11 wall time, used 0 bytes or 0 byte. > write_end_point_report
-points 3 [ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.
[ET-0019]:<End....New Endpoint Report. Sun Apr 18 21:56:57 1999 Part : IDCDSUC Mode : Late
Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 3 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

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```

----- 1 dcd_succ_last F C3+R 1313 -434 81 1078 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1313 -434 81 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1259
-434 121 305 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
R C3+R 1259 -434 121 305 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b F C3+R 1191 -434 79 1261 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y F C3+R 1191 -434 79
R C3+R 1143 -434 87 306 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1097 ---->
C2728rwr/y R C3+R 1143 -434 87 306 1 cs_invvn01c_sl
cs_invvn01c_sl 0 N1097 ----> C2728rwr/a F C3+R 1099 -434 70
165 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
F C3+R 1099 -434 70 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
C2725rwr/a R C3+R 1053 -434 133 157 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y R C3+R 1053 -434
133 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ----> C2721rwr/c

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```

F C3+R 979 -434 65 118 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 74 N892 ---->{d}
C2338/y F C3+R 979 -434 65 118 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N892 ----> C2338/a R C3+R 943 -434 81
125 3 cs_nnd2n02c_sl cs_nnd2n02c_sl 36 N1119 ----> C2905/y
R C3+R 943 -434 81 125 3 cs_invvn01c_sl cs_invvn01c_sl 0 N1119 ---->
C2905/a F C3+R 903 -434 68 92 1 cs_invvn01c_sl
cs_invvn01c_sl 41 N2010 ---->{e} C2906/y F C3+R 903 -434 68
92 1 cs_nor2n02c_sl cs_nor2n02c_sl 0 N2010 ----> C2906/a R
C3+R 868 -434 80 74 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc ---->
dcd_blk_dsucc R C3+R 868 -434 80 74 1 PI 0
dcd_blk_dsucc

```

```

-----
2 slow_mode_blk.reg_n.lat_0/BASE_REG/a F C3+R 1741 -421
0 29 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3- 160 60 238 14 cl_invvn
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1741
-421 0 29 1 AND AND 0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1789 -421 105 16 1 AND
AND -48 a ----> slow_mode_blk.reg_n.lat_0/a R C3+R 1789 -421 105 16
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y R C3+R
1789 -421 105 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N95 ----> C2841/a
F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b}
C2821/y F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N935 ----> C2821/b R C3+R 1693 -421 107
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 45 N512 ---->{c} C2798/y
R C3+R 1693 -421 107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N512 ---->
C2798/a F C3+R 1636 -421 92 35 2 cs_nnd2n02c_sl
> C2778/y F C3+R 1636 -421 92 35 2 cs_invvn01c_sl
cs_invvn01c_sl 0 N1527 ----> C2778/a R C3+R 1563 -421 198
67 4 cs_invvn01c_sl cs_invvn01c_sl 72 N931 ---->{d} C2754/y R
C3+R 1563 -421 198 67 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N931 ---->
C2754/b F C3+R 1450 -421 104 86 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 113 N1555 ----> C2588/y F C3+R 1450 -421 104
86 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1555 ----> C2588/a R
C3+R 1381 -421 120 23 1 cs_invvn01c_sl cs_invvn01c_sl 69 N1730 ---->{e}
C2554/y R C3+R 1381 -421 120 23 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1730 ----> C2554/b F C3+R 1313 -421 79
88 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 68 N1652 ----> C2464/y
F C3+R 1313 -421 79 88 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1652 ---->
C2464/a R C3+R 1260 -421 120 30 1 cs_invvn01c_sl
cs_invvn01c_sl 53 N1749
---->{f} C2412/y R C3+R 1260 -421 120 30 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl 0 N1749 ----> C2412/a F C3+R 1210 -421 55
27 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 50 N1713 ----> C1954/y
F C3+R 1210 -421 55 27 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1713 ---->
C1954/a R C3+R 1171 -421 175 47 2 cs_invvn01c_sl
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ R C3+R 1171
-421 175 47 2 PI 0 br_wrong_targ

```

```

-----
3 dcd_succ_last R C3+R 1349 -420 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1349 -420 123 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1282
-420 85 305 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
F C3+R 1282 -420 85 305 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->

```

```

C2738/b          R C3+R 1230 -420 120 1261 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 52 N1098 ----> C2734rwr/y          R C3+R 1230 -420
120 1261 4 cs_invvn01c_sl      cs_invvn01c_sl 0 N1098 ----> C2734rwr/a
F C3+R 1171 -420 59 306 1 cs_invvn01c_sl      cs_invvn01c_sl 59 N1097 ---->
C2728rwr/y          F C3+R 1171 -420 59 306 1 cs_invvn01c_sl
R 1135 -420 101 165 2 cs_invvn01c_sl      cs_invvn01c_sl 36 N1692 ---->{b}
C2725rwr/y          R C3+R 1135 -420 101 165 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a          F C3+R 1081 -420 93
157 2 cs_nnd2n02c_sl      cs_nnd2n02c_sl 54 N1479 ---->{c} C2721rwr/y
F C3+R 1081 -420 93 157 2 cs_nnd3n02c_sl      cs_nnd3n02c_sl 0 N1479 ---->
C2721rwr/a          R C3+R 1015 -420 214 120 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 66 N1497 ---->{d} C2709rwr/y          R C3+R 1015 -420
214 120 2 cs_nor3n03c_sl      cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a
F C3+R 920 -420 59 51 1 cs_nor3n03c_sl      cs_nor3n03c_sl 95 N1986 ---->{e}
C2677rwr_0/y          F C3+R 920 -420 59 51 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1986 ----> C2677rwr_0/b          R C3+R 887 -420
90 97 2 cs_nnd2n02c_sl      cs_nnd2n02c_sl 33 N1094 ---->{f} C2909/y
R C3+R 887 -420 90 97 2 cs_nnd2n02c_sl      cs_nnd2n02c_sl 0 N1094 ---->
C2909/b          F C3+R 835 -420 80 90 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 52 dcd_mcr41_blk ----> dcd_mcr41_blk          F C3+R 835
-420 80 90 1 PI          0 dcd_mcr41_blk

```

```

-----
> report_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap
violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap
violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet du_iu_store_status(2):a
has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500,
limit 455 INet eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier 1 RISE:
transition 500, limit 455; FALL: transition 500, limit 455 INet dcd_succ_last_t1:y has cap violation
1.077, load 1078, limit 1001, multiplier 1 slack -433.9 INet frc_blk_1cyc_q:l2_out_n has cap
violation 1.008, load 248.9, limit 247, multiplier 1 slack -203.8 INet N22:y has cap violation 1.204,
load 1205, limit 1001, multiplier 1 slack 614.9 INet N26:y has cap violation 1.216, load 1218,
limit 1001, multiplier 1 slack 381.3 INet N36:y has cap violation 1.179, load 1180, limit 1001,
multiplier 1 slack 616.2 INet N1098:y has cap violation 1.26, load 1261, limit 1001, multiplier 1
slack -433.9 INet gbfonet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier 1 slack
27.29 INet gbfonet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 349.9
INet gbfonet_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 478 IDesign
IDCDSUC has 13 violations
> reset_timing_area
> report_drc Checking DRC for
IDesign IDCDSUC INet clkg:clkg has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack
1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack
1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099, multiplier 1 RISE: transition
1):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition
500, limit 455 INet dcd_succ_last_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier 1
slack -433.9 INet frc_blk_1cyc_q:l2_out_n has cap violation 1.008, load 248.9, limit 247, multiplier
1 slack -203.8 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 614.9
INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier 1 slack 381.3 INet N36:y has
cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 616.2 INet N1098:y has cap violation
1.26, load 1261, limit 1001, multiplier 1 slack -433.9 INet gbfonet_2:y has cap violation 1.218, load
1219, limit 1001, multiplier 1 slack 27.29 INet gbfonet_15:y has cap violation 1.169, load 1170,
limit 1001, multiplier 1 slack 349.9 INet gbfonet_16:y has cap violation 1.108, load 1109, limit
1001, multiplier 1 slack 478 IDesign IDCDSUC has 13 violations
> gbfo_fancorr-check
-use_max_load-aggressive-enforce_p... [GB-103]: noninverting buffers are absent Fanout Corr
Area : before 4434.25 after 4434.25 (0.00 %) Slack : before -433.9434 after -433.9434 (0.00 %)
Cell : before 787 after 787 (0.00 %) Time : 4.680000
> gbfo_tune_gain-target_frac 0.98
-gain_incr 0.05 -gain_d... C2906 new rep load 66.5 greater than max 64.9: set to max: FREEZE
SIZEUP C2721rwr new rep load 62.36 greater than max 61.93: set to max: FREEZE SIZEUP C2734rwr

```


new rep load 307.3 greater than max 300.2: set to max: FREEZE SIZEUP C2738 new rep load 99.28
greater than max 96.3: set to max: FREEZE SIZEUP C2709rwr new rep load 43.14 greater than max
42.11: set to max: FREEZE SIZEUP Tune Gain Area : before 4434.25 after 4385.96 (1.09 %)
Slack : before -433.9434 after -433.0000 (0.22 %) Cell : before 787 after 787 (0.00 %) Time :
11.630000 > attribute_gain -to > report_gain_violations -min 1.0 -max 10.0

----- Gain Violation Report for design IDCDSUC

Design		Type	Gain	Cell Name
0.777985	C2894	cs_nnd2n02c_sl Max	10.230905 C2194	cs_invvn01c_sl Min
13.073235	C2907	cs_invvn01c_sl Min	10.629883 C2895	cs_invvn01c_sl Max
12.189666	C2918	cs_nor2n02c_sl Min	0.963504 C2911	cs_nnd2n02c_sl Max
			0.681414 C2677rwr_0	cs_nnd2n02c_sl
> cds_acc -slack resize Area : before 2731.15 after 2731.15 (0.00 %) Slack : before -1475.6755				
after -1475.6755 (0.00 %) Cell : before 722 after 722 (0.00 %) Time : 0.750000 resize				
Area : before 2731.15 after 2731.15 (0.00 %) Slack : before -1475.6755 after -1475.6755 (0.00 %)				
Cell : before 722 after 722 (0.00 %) Time : 1.520000 resize Area : before 5081.39 after 5081.39				
(0.00 %) Slack : before -603.6691 after -603.6691 (0.00 %) Cell : before 763 after 763 (0.00 %)				
Time : 1.750000 tgfs rewiring Area : before 5441.99 after 5359.17 (1.52 %) Slack : before				
-603.6691 after -543.6871 (9.94 %) Cell : before 763 after 762 (0.13 %) Time : 20.260000 tgfs				
rewiring Area : before 5133.28 after 5092.88 (0.79 %) Slack : before -513.2166 after -506.3137				
(1.35 %) Cell : before 775 after 773 (0.26 %) Time : 13.960000 Assign Gain Area : before				
5092.88 after 4486.86 (11.90 %) Slack : before -506.3137 after -812.2559 (-60.43 %)				
Cell : before 773 after 773 (0.00 %) Time : 2.590000 Fanout Corr Area : before 4486.86 after				
4502.64 (-0.35 %) Slack : before -812.2559 after -812.2559 (0.00 %) Cell : before 773 after 787				
(-1.81 %) Time : 4.870000 Tune Gain Area : before 4502.64 after 4352.61 (3.33 %)				
Slack : before -812.2559 after -680.5689 (16.21 %) Cell : before 787 after 787 (0.00 %) Time :				
46.970000 Tune Gain Area : before 4352.61 after 4474.51 (-2.80 %) Slack : before -680.5689				
787 (0.00 %) Time : 20.930000 resize Area : before 4474.51 after 4474.51				
(0.00 %) Slack : before -446.0240 after -446.0240 (0.00 %) Cell : before 787 after 787 (0.00 %)				
Time : 1.780000 swap Area : before 4474.51 after 4475.36 (-0.02 %) Slack : before -446.0240				
after -441.6489 (0.98 %) Cell : before 787 after 787 (0.00 %) Time : 2.560000 tgfs rewiring				
Area : before 4475.36 after 4531.42 (-1.25 %) Slack : before -441.6489 after -441.6489 (0.00 %)				
Cell : before 787 after 787 (0.00 %) Time : 14.330000 Tune Gain Area : before 4531.42 after				
4432.62 (2.18 %) Slack : before -441.6489 after -433.9434 (1.74 %) Cell : before 787 after 787				
(0.00 %) Time : 12.060000 tgfs rewiring Area : before 4432.62 after 4434.25 (-0.04 %)				
Slack : before -433.9434 after -433.9434 (0.00 %) Cell : before 787 after 787 (0.00 %) Time :				
10.200000 Fanout Corr Area : before 4434.25 after 4434.25 (0.00 %) Slack : before -433.9434				
after -433.9434 (0.00 %) Cell : before 787 after 787 (0.00 %) Time : 4.680000 Tune Gain				
Area : before 4434.25 after 4385.96 (1.09 %) Slack : before -433.9434 after -433.0000 (0.22 %)				
Cell : before 787 after 787 (0.00 %) Time : 11.630000 CDS Effectiveness Report: Trafo				
SI/call	Tot SI	SI/Deg	#calls	#time:
Tune Gain	93.720207	374.880829	0.000000	4
66.884827	0.000000	4	58.75	swap
2.56	Legalization	0.000000	0.000000	0
0.000000	0.000000	0.000000	0	Apportion FO-
0.000000	0.000000	0	0	Assign Gain
2.59	Fanout Corr	0.000000	0.000000	2
0.000000	0.000000	0.000000	0	Stretch Delay
0.000000	0.000000	0	0	Streect Mincut
0.000000	0	0	0	phantom
Buffering	0.000000	0.000000	0.000000	0
0.000000	0.000000	0	0	spltless
0	bmove	0.000000	0.000000	0
0.000000	0.000000	0.000000	0	resize
0.000000	4	5.8	0.000000	0
spltp	0.000000	0.000000	0.000000	0
				phase

```

0.000000 0.000000 0 0 > cds_acc -runtime -no_full CDS Effectiveness
Report: Trafo SI/call Tot SI SIDeg
#calls #time: Tune Gain 93.720207 374.880829 0.000000 4 91.59
tgfs rewiring 16.721207 66.884827 0.000000 4 58.75 Fanout Corr 0.000000
0.000000 0.000000 2 9.55 resize 0.000000 0.000000 0.000000 4
5.8 Assign Gain 0.000000 0.000000 -305.942200 1 2.59 swap
4.375061 4.375061 0.000000 1 2.56 Legalization 0.000000 0.000000
0.000000 0 0 Buffering 0.000000 0.000000 0.000000 0
Beta Assign 0.000000 0.000000 0.000000 0 0 Stretch Delay
0.000000 0.000000 0.000000 0 0 Strect Mincut 0.000000
0.000000 0.000000 0 0 phantom 0.000000 0.000000 0.000000 0
0 Stretch Area 0.000000 0.000000 0.000000 0 0 phantomless
0.000000 0.000000 0.000000 0 0 spltless 0.000000 0.000000
0.000000 0 0 bmove 0.000000 0.000000 0.000000 0
pmove 0.000000 0.000000 0.000000 0 0 Apportion FO
0.000000 0.000000 0.000000 0 0 bftm 0.000000 0.000000
0.000000 0 0 spltp 0.000000 0.000000 0.000000 0
phase 0.000000 0.000000 0.000000 0 0 > echo {Custom Synzilla
Report} Custom Synzilla Report > ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0
upcells 122 IN ports 73 OUT ports 787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786
LINKED; 0 UNLINKED; 0 DC) 0 buses 1008 nets (0 multiply-driven; 0 undriven)
2632 pins (0 inversions) 2.61 pins per net 1551 literals 21 levels 10 max fanin
15 max fanout Cell Information FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area 0) PSEUDO_REG (ncount 83 : area 0)
cb_clk_32_1 (ncount 6 : area 480) cb_mode_block (ncount 1 : area
70) cs_ao12n03c_sl (ncount 6 : area 24)
cs_ao22n03c_sl (ncount 16 : area 96) cs_invvn01c_sl (ncount 229 : area
458) cs_nnd2n02c_sl (ncount 206 : area 618)
ount 31 : area 124) cs_nnd4n03c_sl (ncount 7 : area 35)
cs_nor2n02c_sl (ncount 13 : area 39) cs_nor3n03c_sl (ncount 2 : area
8) cs_oa21n03c_sl (ncount 3 : area 15)
cs_oa22n03c_sl (ncount 1 : area 6) cs_xbn2n01b_sl (ncount 1 : area
8) cs_xbo2n01b_sl (ncount 1 : area 8) Total Area =
1989 (Comb = 1439 : Non-Comb = 550) > write_end_point_report -points 2
[ET-0018]:>Begin...New EndPoint Report for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:57:21 1999 Part : IDCDSUC Mode : Late
Mode / Nominal EDA EinsTimer EndPoint Report Release Level : 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack Abbreviation Comparison/Description -----
----- Slack Continuation SlkCont Slack due to a point downstream on
path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST) Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST) Clock Tree Pulse Width ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop ALTest (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST) Arrival Time Limiting
ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName

```

E Phase	AT	Slack	Slew	CL	FO Cell	P Func	T.Adj	NetName
-----	1 dcd_succ_last					F C3+R	1312	-433 81 1078 7
PO	0 dcd_succ_last_t1 RAT							879
0 ---->	C2744/y				F C3+R	1312	-433 81 1078 7	cs_invvn01c_sl
cs_invvn01c_sl	0 dcd_succ_last_t1 ---->	C2744/a			R C3+R			1258
-433 121 304 4	cs_invvn01c_sl	cs_invvn01c_sl	54	N675 ---->	{a} C2738/y			
R C3+R	1258 -433 121 304 4	cs_nnd2n02c_sl	cs_nnd2n02c_sl	0	N675 ---->			
C2738/b		F C3+R	1190	-433 79	1260 4	cs_nnd2n02c_sl		
cs_nnd2n02c_sl	68 N1098 ---->	C2734rwr/y			F C3+R	1190	-433 79	
	R C3+R	1143 -433 86	306 1	cs_invvn01c_sl	cs_invvn01c_sl	47		
N1097 ---->	C2728rwr/y			R C3+R	1143 -433 86	306 1		
cs_invvn01c_sl	cs_invvn01c_sl	0	N1097 ---->	C2728rwr/a				F
C3+R	1099 -433 71	171 2	cs_invvn01c_sl	cs_invvn01c_sl	44	N1692 ---->	{b}	
C2725rwr/y		F C3+R	1099	-433 71	171 2	cs_nnd2n02c_sl		
cs_nnd2n02c_sl	0 N1692 ---->	C2725rwr/a			R C3+R	1053	-433	
134 157 2	cs_nnd2n02c_sl	cs_nnd2n02c_sl	46	N1479 ---->	{c} C2721rwr/y			
R C3+R	1053 -433 134 157 2	cs_nnd3n02c_sl	cs_nnd3n02c_sl	0	N1479 ---->			
C2721rwr/c		F C3+R	978	-433 64	109 2	cs_nnd3n02c_sl		
cs_nnd3n02c_sl	74 N892 ---->	{d} C2338/y			F C3+R	978	-433 64	
109 2	cs_nnd2n02c_sl	cs_nnd2n02c_sl	0	N892 ---->	C2338/a			
R C3+R	943 -433 81	126 3	cs_nnd2n02c_sl	cs_nnd2n02c_sl	35	N1119 ---->		
C2905/y		R C3+R	943	-433 81	126 3	cs_invvn01c_sl		
cs_invvn01c_sl	0 N1119 ---->	C2905/a			F C3+R	903	-433 68	
91 1	cs_invvn01c_sl	cs_invvn01c_sl	41	N2010 ---->	{e} C2906/y			F
C3+R	903 -433 68	91 1	cs_nor2n02c_sl	cs_nor2n02c_sl	0	N2010 ---->	C2906/a	
R C3+R	868 -433 80	73 1	cs_nor2n02c_sl	cs_nor2n02c_sl	35	dcd_blk_dsucc		
---->	dcd_blk_dsucc		R C3+R	868	-433 80	73 1	PI	
0 dcd_blk_dsucc								
-----	2 dcd_succ_last					R C3+R	1353	-424 123 1078 7
PO	0 dcd_succ_last_t1 RAT							929
0 ---->	C2744/y				R C3+R	1353	-424 123 1078 7	cs_invvn01c_sl
cs_invvn01c_sl	0 dcd_succ_last_t1 ---->	C2744/a			F C3+R			1286
-424 85 304 4	cs_invvn01c_sl	cs_invvn01c_sl	67	N675 ---->	{a} C2738/y			
F C3+R	1286 -424 85 304 4	cs_nnd2n02c_sl	cs_nnd2n02c_sl	0	N675 ---->			
C2738/b		R C3+R	1234	-424 120	1260 4	cs_nnd2n02c_sl		
cs_nnd2n02c_sl	52 N1098 ---->	C2734rwr/y			R C3+R	1234	-424	
120 1260 4	cs_invvn01c_sl	cs_invvn01c_sl	0	N1098 ---->	C2734rwr/a			
F C3+R	1175 -424 58	306 1	cs_invvn01c_sl	cs_invvn01c_sl	59	N1097 ---->		
C2728rwr/y		F C3+R	1175	-424 58	306 1	cs_invvn01c_sl		
cs_invvn01c_sl	0 N1097 ---->	C2728rwr/a			R C3+R	1140	-424 101	
171 2	cs_invvn01c_sl	cs_invvn01c_sl	35	N1692 ---->	{b} C2725rwr/y			
2	cs_nnd2n02c_sl	cs_nnd2n02c_sl	0	N1692 ---->	C2725rwr/a			F
C3+R	1086 -424 93	157 2	cs_nnd2n02c_sl	cs_nnd2n02c_sl	54	N1479 ---->	{c}	
C2721rwr/y		F C3+R	1086	-424 93	157 2	cs_nnd3n02c_sl		
cs_nnd3n02c_sl	0 N1479 ---->	C2721rwr/a			R C3+R	1020	-424	
204 111 2	cs_nnd3n02c_sl	cs_nnd3n02c_sl	65	N1497 ---->	{d} C2709rwr/y			
R C3+R	1020 -424 204 111 2	cs_nor3n03c_sl	cs_nor3n03c_sl	0	N1497 ---->			
C2709rwr/c		F C3+R	905	-424 115	50 1	cs_nor3n03c_sl		
cs_nor3n03c_sl	115 N1976 ---->	{e} C2579rwr_0_0/y			F C3+R	905	-424	
115 50 1	cs_nnd3n02c_sl	cs_nnd3n02c_sl	0	N1976 ---->	C2579rwr_0_0/c			
R C3+R	834 -424 162	39 2	cs_nnd3n02c_sl	cs_nnd3n02c_sl	71	N1719 ---->	{f}	
C2599rwr_0_0_0/y		R C3+R	834	-424 162	39 2	cs_nor2n02c_sl		
cs_nor2n02c_sl	0 N1719 ---->	C2599rwr_0_0_0/a			F C3+R	754	-424	

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72 22 1 cs_nor2n02c_sl      cs_nor2n02c_sl 80 N1942 ---->{g} C2349rwr_0_0_0_0/y
F C3+R 754 -424 72 22 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl 0 N1942 ---->
C2349rwr_0_0_0_0/a          R C3+R 712 -424 99 20 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 42 N288 ---->{h} C2339/y          R C3+R 712 -424 99
20 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl 0 N288 ----> C2339/a          F
C3+R 665 -424 65 20 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl 46 NET690 ---->{i}
C2187/y          F C3+R 665 -424 65 20 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 NET690 ----> C2187/a          R C3+R 630 -424 78
39 2 cs_nnd2n02c_sl      cs_nnd2n02c_sl 35 N29 ----> C2020/y          R
C3+R 630 -424 78 39 2 cs_invvn01c_sl      cs_invvn01c_sl 0 N29 ----> C2020/a
F C3+R 557 -424 424 40 1 cs_invvn01c_sl      cs_invvn01c_sl 73 du_iu_hold_aa_req
----> du_iu_hold_aa_req          F C3+R 557 -424 424 40 1 PI
0 du_iu_hold_aa_req

```

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-----
> report_area Design: /IDCDSUC - Area: 4385.956543, Area(Weight):
1283.882935 > cputime Used 40.74 cpu seconds or 00:00:41 wall time, used 0 bytes or 0
byte. > echo {=== CDS process finished ===} === CDS process finished === Good names for
IDCDSUC Count User Transform New For all nets 1008
556 0 452 For all nets 1008 55.16% 0.00% 44.84% For I/O port nets
179 71.51% 0.00% 28.49% For register output nets 166 100.00% 0.00%
0.00% Count User Transform New For all boxes 787
290 22 475 For all boxes 787 36.85% 2.80% 60.36% For register boxes
% 0.00% For linked boxes 786 36.90% 2.80% 60.31% > echo
{Custom Synzilla Report} Custom Synzilla Report > ps -cell Design /HISVHDL/IDCDSUC has:
1 instances 0 upcells 122 IN ports 73 OUT ports 787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI;
786 LINKED; 0 UNLINKED; 0 DC) 0 buses 1008 nets (0 multiply-driven; 0 undriven)
2632 pins (0 inversions) 2.61 pins per net 1551 literals 21 levels 10 max fanin
15 max fanout Cell Information FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area 0) PSEUDO_REG (ncount 83 : area 0)
cb_clk_32_1 (ncount 6 : area 480) cb_mode_block (ncount 1 : area
70) cs_ao12n03c_sl (ncount 6 : area 24)
cs_ao22n03c_sl (ncount 16 : area 96) cs_invvn01c_sl (ncount 229 : area
458) cs_nnd2n02c_sl (ncount 206 : area 618)
cs_nnd3n02c_sl (ncount 31 : area 124) cs_nnd4n03c_sl (ncount 7 : area
35) cs_nor2n02c_sl (ncount 13 : area 39)
cs_nor3n03c_sl (ncount 2 : area 8) cs_ao21n03c_sl (ncount 3 : area
15) cs_ao22n03c_sl (ncount 1 : area 6)
cs_xbn2n01b_sl (ncount 1 : area 8) cs_xbo2n01b_sl (ncount 1 : area
8) Total Area = 1989 (Comb = 1439 : Non-Comb = 550) >
write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:57:23
1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description ----- Slack
Continuation SlkCont Slack due to a point downstream on path Required Arrival Time
RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet (
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST) Clock Gating
Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
+ ADJUST) Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH <
CLOCK TRAILING EDGE) Setup Setup (DATA ARRIVAL TIME + SETUP <
CLOCK ARRIVAL TIME + ADJUST) Hold Hold (DATA ARRIVAL TIME - HOLD
> CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC (DATA ARRIVAL TIME
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth ClkPW (CLOCK

```

LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ClkSep
 (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
 ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
 LimitedAT/ Delay/ Failed Test/ Test PinName
 E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```
----- 1 dcd_succ_last F C3+R 1312 -433 81 1078 7
0 ----> C2744/y F C3+R 1312
-433 81 1078 7 cs_invvn01c_sl cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
R C3+R 1258 -433 121 304 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a}
C2738/y R C3+R 1258 -433 121 304 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N675 ----> C2738/b F C3+R 1190 -433 79
1260 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y
F C3+R 1190 -433 79 1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ---->
C2734rwr/a R C3+R 1143 -433 86 306 1 cs_invvn01c_sl
cs_invvn01c_sl 47 N1097 ----> C2728rwr/y R C3+R 1143 -433 86
306 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1097 ----> C2728rwr/a
F C3+R 1099 -433 71 171 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b}
C2725rwr/y F C3+R 1099 -433 71 171 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a R C3+R 1053 -433
134 157 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y
R C3+R 1053 -433 134 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
C2721rwr/c F C3+R 978 -433 64 109 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 74 N892 ---->{d} C2338/y F C3+R 978 -433 64
109 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N892 ----> C2338/a
R C3+R 943 -433 81 126 3 cs_nnd2n02c_sl cs_nnd2n02c_sl 35 N1119 ---->
C2905/y R C3+R 943 -433 81 126 3 cs_invvn01c_sl
cs_invvn01c_sl 0 N1119 ----> C2905/a F C3+R 903 -433 68
91 1 cs_invvn01c_sl cs_invvn01c_sl 41 N2010 ---->{e} C2906/y F
C3+R 903 -433 68 91 1 cs_nor2n02c_sl cs_nor2n02c_sl 0 N2010 ----> C2906/a
R C3+R 868 -433 80 73 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc
----> dcd_blk_dsucc R C3+R 868 -433 80 73 1 PI
0 dcd_blk_dsucc
```

```
----- 2 dcd_succ_last R C3+R 1353 -424 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1353 -424 123 1078 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1286
-424 85 304 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
0 N675 ----> C2738/b R C3+R 1234 -424 120 1260 4
cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1098 ----> C2734rwr/y R
C3+R 1234 -424 120 1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ---->
C2734rwr/a F C3+R 1175 -424 58 306 1 cs_invvn01c_sl
cs_invvn01c_sl 59 N1097 ----> C2728rwr/y F C3+R 1175 -424 58
306 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1097 ----> C2728rwr/a
R C3+R 1140 -424 101 171 2 cs_invvn01c_sl cs_invvn01c_sl 35 N1692 ---->{b}
C2725rwr/y R C3+R 1140 -424 101 171 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1692 ----> C2725rwr/a F C3+R 1086 -424 93
157 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 54 N1479 ---->{c} C2721rwr/y
F C3+R 1086 -424 93 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
C2721rwr/a R C3+R 1020 -424 204 111 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 65 N1497 ---->{d} C2709rwr/y R C3+R 1020 -424
204 111 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1497 ----> C2709rwr/c
F C3+R 905 -424 115 50 1 cs_nor3n03c_sl cs_nor3n03c_sl 115 N1976 ---->{e}
```

```

C2579rwr_0_0/y          F C3+R  905  -424  115  50 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl  0 N1976 ----> C2579rwr_0_0/c          R C3+R  834  -424
162  39 2 cs_nnd3n02c_sl      cs_nnd3n02c_sl  71 N1719 ---->{f} C2599rwr_0_0_0/y
R C3+R  834  -424  162  39 2 cs_nor2n02c_sl      cs_nor2n02c_sl  0 N1719 ---->
C2599rwr_0_0_0/a          F C3+R  754  -424  72  22 1 cs_nor2n02c_sl
cs_nor2n02c_sl  80 N1942 ---->{g} C2349rwr_0_0_0_0_0/y          F C3+R  754  -424
72  22 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 N1942 ----> C2349rwr_0_0_0_0_0/a
R C3+R  712  -424  99  20 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  42 N288 ---->{h}
C2339/y          R C3+R  712  -424  99  20 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl  0 N288 ----> C2339/a          F C3+R  665  -424  65
20 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  46 NET690 ---->{i} C2187/y
F C3+R  665  -424  65  20 1 cs_nnd2n02c_sl      cs_nnd2n02c_sl  0 NET690 ---->
C2187/a          R C3+R  630  -424  78  39 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl  35 N29 ----> C2020/y          R C3+R  630  -424  78
39 2 cs_invvn01c_sl      cs_invvn01c_sl  0 N29 ----> C2020/a          F
C3+R  557  -424  424  40 1 cs_invvn01c_sl      cs_invvn01c_sl  73 du_iu_hold_aa_req
----> du_iu_hold_aa_req          F C3+R  557  -424  424  40 1 PI
0 du_iu_hold_aa_req

```

```

IDCDSUC - Area: 4385.956543, Area(Weight): 1283.882935          > cputime Used 2.05 cpu
seconds or 00:00:02 wall time, used 0 bytes or 0 byte.          > echo {=== Discretization process ===}
=== Discretization process ===          > time_units -nano          > time_units -nano          >
cds_discrete -no_slew_violation          > echo {Custom Synzilla Report} Custom Synzilla Report
> ps -cell Design /HISVHDL/IDCDSUC has:          1 instances  0 upcells  122 IN ports 73 OUT ports
787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC)  0 buses  1008 nets (0
multiply-driven; 0 undriven)          2632 pins (0 inversions)  2.61 pins per net  1551 literals
21 levels  10 max fanin  15 max fanout          Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area  0)          PSEUDO_REG (ncount
83 : area  0)          cb_clk_32_1 (ncount  6 : area  480)
cb_mode_block (ncount  1 : area  70)          cs_ao12n03c (ncount  6 : area
24)          cs_ao22n03c (ncount  15 : area  90)          cs_ao22n10c
(ncount  1 : area  18)          cs_invvn01c (ncount 130 : area  260)
cs_invvn02c (ncount  7 : area  14)          cs_invvn04c (ncount  5 : area  10)
          cs_invvn05c (ncount 13 : area  26)          cs_invvn06c (ncount  9
: area  18)          cs_invvn07c (ncount  9 : area  18)
cs_invvn08c (ncount  3 : area  12)          cs_invvn09c (ncount  7 : area  28)
          cs_invvn10c (ncount  6 : area  24)          cs_invvn11c (ncount  5
: area  30)          cs_invvn12c (ncount 21 : area 126)
cs_invvn13c (ncount  4 : area  32)          cs_invvn14c (ncount  1 : area  8)
          cs_invvn15c (ncount  4 : area  40)          cs_invvn16c (ncount  3
: area  42)          cs_invvn18c (ncount  1 : area  20)
cs_invvn19c (ncount  1 : area  25)          cs_nnd2n02c (ncount 185 : area
555)          cs_nnd2n03c (ncount  3 : area  9)          cs_nnd2n04c
(ncount  3 : area  9)          cs_nnd2n05c (ncount  3 : area  12)
cs_nnd2n06c (ncount  2 : area  8)          cs_nnd2n07c (ncount  2 : area
8)          cs_nnd2n11c (ncount  1 : area 11)          cs_nnd2n12c
(ncount  1 : area 12)          cs_nnd2n13c (ncount  4 : area  60)
cs_nnd2n14c (ncount  2 : area  38)          cs_nnd3n02c (ncount 27 : area
108)          cs_nnd3n05c (ncount  1 : area  6)          cs_nnd3n06c
(ncount  1 : area  6)          cs_nnd3n09c (ncount  1 : area 12)
cs_nnd3n12c (ncount  1 : area  22)          cs_nnd4n03c (ncount  6 : area
30)          cs_nnd4n09c (ncount  1 : area 16)          cs_nor2n02c
(ncount 10 : area  30)          cs_nor2n04c (ncount  2 : area  6)
cs_nor2n12c (ncount  1 : area 12)          cs_nor3n03c (ncount  1 : area  4)
          cs_nor3n10c (ncount  1 : area 12)          cs_ao21n03c (ncount

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1 : area 5) cs_oa21n04c (ncount 1 : area 5)
cs_oa21n05c (ncount 1 : area 8) cs_oa22n03c (ncount 1 : area
6) cs_xbn2n01b (ncount 1 : area 8) cs_xbo2n01d
(ncount 1 : area 8) Total Area = 2441 (Comb = 1891 : Non-Comb = 550)
> write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:57:29
1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description ----- Slack
Continuation SlkCont Slack due to a point downstream on path Required Arrival Time
EQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME <
ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet (DATA ARRIVAL
TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST) Clock Gating Hold
ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK
ARRIVAL TIME + ADJUST) Hold Hold (DATA ARRIVAL TIME - HOLD >
CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC (DATA ARRIVAL TIME +
CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth ClkPW (CLOCK
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ClkSep
(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

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```

----- 1 slow_mode_blk.reg_n.lat_0/BASE_REG/a F C3+R 1745 -424
0 29 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3- 160 60 238 14 cl_invvn
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1745
-424 0 29 1 AND AND 0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1793 -424 106 16 1 AND
AND -48 a ----> slow_mode_blk.reg_n.lat_0/a R C3+R 1793 -424 106 16
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y R C3+R
1793 -424 106 16 1 cs_nnd2n 02c cs_nnd2n02c 0 N95 ----> C2841/a
F C3+R 1740 -424 77 17 1 cs_nnd2n 02c cs_nnd2n02c 53 N935 ---->{b}
C2821/y F C3+R 1740 -424 77 17 1 cs_nnd2n 02c
cs_nnd2n02c 0 N935 ----> C2821/b R C3+R 1694 -424 109
17 1 cs_nnd2n 02c cs_nnd2n02c 46 N512 ---->{c} C2798/y R
C3+R 1694 -424 109 17 1 cs_nnd2n 02c cs_nnd2n02c 0 N512 ----> C2798/a
F C3+R 1634 -424 103 35 2 cs_nnd2n 02c cs_nnd2n02c 61 N1527 ---->
C2778/y F C3+R 1634 -424 103 35 2 cs_invvn 01c
cs_invvn01c 0 N1527 ----> C2778/a R C3+R 1552 -424 215
66 4 cs_invvn 01c cs_invvn01c 82 N931 ---->{d} C2754/y R
C3+R 1552 -424 215 66 4 cs_nnd2n 03c cs_nnd2n03c 0 N931 ----> C2754/b
F C3+R 1431 -424 99 85 5 cs_nnd2n 03c cs_nnd2n03c 121 N1555 ---->
F C3+R 1431 -424 99 85 5 cs_invvn 05c cs_invvn05c
0 N1555 ----> C2588/a R C3+R 1366 -424 115 24 1 cs_invvn
05c cs_invvn05c 66 N1730 ---->{e} C2554/y R C3+R 1366 -424
115 24 1 cs_nnd2n 03c cs_nnd2n03c 0 N1730 ----> C2554/b
F C3+R 1300 -424 78 87 5 cs_nnd2n 03c cs_nnd2n03c 66 N1652 ---->
C2464/y F C3+R 1300 -424 78 87 5 cs_invvn 07c
cs_invvn07c 0 N1652 ----> C2464/a R C3+R 1248 -424 117
31 1 cs_invvn 07c cs_invvn07c 52 N1749 ---->{f} C2412/y R

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C3+R 1248 -424 117 31 1 cs_nnd3n 06c cs_nnd3n06c 0 N1749 ----> C2412/a
F C3+R 1202 -424 45 27 1 cs_nnd3n 06c cs_nnd3n06c 46 N1713 ---->
C1954/y F C3+R 1202 -424 45 27 1 cs_invvn 07c
cs_invvn07c 0 N1713 ----> C1954/a R C3+R 1171 -424 175
49 2 cs_invvn 07c cs_invvn07c 31 br_wrong_targ ----> br_wrong_targ
R C3+R 1171 -424 175 49 2 PI 0 br_wrong_targ

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```

-----
2 dcd_succ_last R C3+R 1351 -422 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1351 -422 123 1078 7 cs_invvn
18c cs_invvn18c 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1285
-422 83 302 4 cs_invvn 18c cs_invvn18c 66 N675 ----> {a} C2738/y
F C3+R 1285 -422 83 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---->
C2738/b R C3+R 1235 -422 118 1261 4 cs_nnd2n 14c
cs_nnd2n14c 50 N1098 ----> C2734rwr/y R C3+R 1235 -422 118
1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a F
C3+R 1178 -422 54 310 1 cs_invvn 19c cs_invvn19c 56 N1097 ---->
C2728rwr/y F C3+R 1178 -422 54 310 1 cs_invvn 16c
cs_invvn16c 0 N1097 ----> C2728rwr/a R C3+R 1145 -422 104
181 2 cs_invvn 16c cs_invvn16c 33 N1692 ----> {b} C2725rwr/y R
C3+R 1145 -422 104 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
C2725rwr/a F C3+R 1090 -422 91 161 2 cs_nnd2n 13c
cs_nnd2n13c 56 N1479 ----> {c} C2721rwr/y F C3+R 1090 -422 91
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479
----> C2721rwr/a R C3+R 1025 -422 199 115 2 cs_nnd3n
12c cs_nnd3n12c 65 N1497 ----> {d} C2709rwr/y R C3+R 1025 -422
199 115 2 cs_nor3n 10c cs_nor3n10c 0 N1497 ----> C2709rwr/c
F C3+R 912 -422 115 52 1 cs_nor3n 10c cs_nor3n10c 113 N1976 ----> {e}
C2579rwr_0_0/y F C3+R 912 -422 115 52 1 cs_nnd3n 05c
cs_nnd3n05c 0 N1976 ----> C2579rwr_0_0/c R C3+R 840 -422 171
40 2 cs_nnd3n 05c cs_nnd3n05c 72 N1719 ----> {f} C2599rwr_0_0_0/y
R C3+R 840 -422 171 40 2 cs_nor2n 04c cs_nor2n04c 0 N1719 ---->
C2599rwr_0_0_0/b F C3+R 747 -422 109 21 1 cs_nor2n 04c
cs_nor2n04c 93 N1956 ----> {g} C2440rwr/y F C3+R 747 -422 109
21 1 cs_nnd4n 03c cs_nnd4n03c 0 N1956 ----> C2440rwr/b R
C3+R 679 -422 144 18 1 cs_nnd4n 03c cs_nnd4n03c 68 N283 ----> {h} C2318/y
R C3+R 679 -422 144 18 1 cs_oa21n 04c cs_oa21n04c 0 N283 ---->
C2318/a1 F C3+R 598 -422 81 37 2 cs_oa21n 04c
cs_oa21n04c 81 three_branches ----> three_branches F C3+R 598
-422 81 37 2 PI 0 three_branches

```

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-----
> report_area Design: /IDCDSUC - Area: 4516.000000, Area(Weight):
2441.000000 > cputime Used 5.56 cpu seconds or 00:00:05 wall time, used 0 bytes or 0 byte.
> report_drc Checking DRC for IDesign IDCDSUC INet eu_iu_enter_slow_md:a has transition violation
1.214, multiplier 1 RISE: transition 352, limit 290; FALL: transition 346, limit 290 INet
eu_iu_mmode:a has transition violation 1.124, multiplier 1 RISE: transition 326, limit 290; FALL:
transition 326, limit 290 INet du_iu_hold_aa_req:a has transition violation 1.462, multiplier 1
RISE: transition 424, limit 290; FALL: transition 424, limit 290 INet eu_iu_fpu_end_op:a has
transition violation 1.169, multiplier 1 RISE: transition 339, limit 290; FALL: transition 338, limit
290 INet eu_iu_misc_hold:c has transition violation 1.145, multiplier 1 RISE: transition 332, limit
290; FALL: transition 310, limit 290 INet clkg:clkg has cap violation 1.032, load 145.5, limit 141,
multiplier 1 slack 1.134e+38 INet du_iu_quiesced:a has transition violation 1.166, multiplier 1
RISE: transition 338, limit 290; FALL: transition 338, limit 290 INet iq_empty:iq_empty has cap
violation 1.019, load 143.6, limit 141, multiplier 1 slack -383.8 INet clkg2:clkg2 has cap violation
1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet eu_iu_fxu_exc_cond:a has transition

```


[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

290 INet N1781:a has transition violation 1.002, multiplier 1 RISE: transition 290.7, limit 290;
 FALL: transition 217, limit 290 INet N1781:b has transition violation 1.002, multiplier 1 RISE:
 transition 290.7, limit 290; FALL: transition 217, limit 290 resize Area : before 4516.00 after
 4516.00 (0.00 %) Slack : before -424.3224 after -415.6229 (2.05 %) Cell : before 787 after 787
 (0.00 %) Time : 5.610000 > write_end_point_report -points 3 [ET-0018]:>Begin...New
 EndPoint Report for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
 Sun Apr 18 21:57:39 1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer
 EndPoint Report Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
 -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max.

Endpoints:	3	Cause of Slack	Abbreviation	Comparison/Description	-----
Slack Continuation	SlkCont	Slack due to a point downstream on path	Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)	Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)	Clock Gating Hold
ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)	Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)	Setup
Setup	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)	EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)	ClockPulseWidth
ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)	ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)	Loop
ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)	Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test Num/	LimitedAT/
Failed Test/	Test PinName	E Phase	AT	Slack	Slew
P Func	T Adj	NetName		CL	FO Cell

```

----- 1 dcd_succ_last ----- R C3+R 1345 -416 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1345 -416 123 1078 7 cs_invn
18c cs_invn18c 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1279
-416 83 302 4 cs_invn 18c cs_invn18c 66 N675 ----> {a} C2738/y
F C3+R 1279 -416 83 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---->
C2738/b R C3+R 1228 -416 118 1261 4 cs_nnd2n 14c
cs_nnd2n14c 50 N1098 ----> C2734rwr/y R C3+R 1228 -416 118
1261 4 cs_invn 19c cs_invn19c 0 N1098 ----> C2734rwr/a F
C3+R 1172 -416 54 310 1 cs_invn 19c cs_invn19c 56 N1097 ---->
C2728rwr/y F C3+R 1172 -416 54 310 1 cs_invn 16c
cs_invn16c 0 N1097 ----> C2728rwr/a R C3+R 1139 -416 104
181 2 cs_invn 16c cs_invn16c 33 N1692 ----> {b} C2725rwr/y R
C3+R 1139 -416 104 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
C2725rwr/a F C3+R 1083 -416 91 161 2 cs_nnd2n 13c
cs_nnd2n13c 56 N1479 ----> {c} C2721rwr/y F C3+R 1083 -416 91
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ----> C2721rwr/a
R C3+R 1019 -416 199 115 2 cs_nnd3n 12c cs_nnd3n12c 65 N1497 ----> {d}
C2709rwr/y R C3+R 1019 -416 199 115 2 cs_nor3n 10c
cs_nor3n10c 0 N1497 ----> C2709rwr/c F C3+R 907 -416 92
52 1 cs_nor3n 10c cs_nor3n10c 111 N1976 ----> {e} C2579rwr_0_0/y
F C3+R 907 -416 92 52 1 cs_nnd3n 07c cs_nnd3n07c 0 N1976 ---->
C2579rwr_0_0/c R C3+R 849 -416 189 47 2 cs_nnd3n 07c
R C3+R 849 -416 189 47 2 cs_nor2n 04c cs_nor2n04c 0
N1719 ----> C2599rwr_0_0_0/b F C3+R 747 -416 109 21 1 cs_nor2n
04c cs_nor2n04c 102 N1956 ----> {g} C2440rwr/y F C3+R 747 -416
109 21 1 cs_nnd4n 03c cs_nnd4n03c 0 N1956 ----> C2440rwr/b

```


R C3+R 679 -416 144 18 1 cs_nnd4n 03c cs_nnd4n03c 68 N283 ---->{h}
 C2318/y R C3+R 679 -416 144 18 1 cs_oa21n 04c
 cs_oa21n04c 0 N283 ----> C2318/a1 F C3+R 598 -416 81 37
 2 cs_oa21n 04c cs_oa21n04c 81 three_branches ----> three_branches
 F C3+R 598 -416 81 37 2 PI 0 three_branches

----- 2 dcd_succ_last F C3+R 1294 -415 79 1078 7
 PO 0 dcd_succ_last_t1 RAT 879
 0 ----> C2744/y F C3+R 1294 -415 79 1078 7 cs_invvn
 18c cs_invvn18c 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1241
 -415 119 302 4 cs_invvn 18c cs_invvn18c 53 N675 ---->{a} C2738/y
 R C3+R 1241 -415 119 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---->
 C2738/b F C3+R 1175 -415 76 1261 4 cs_nnd2n 14c
 cs_nnd2n14c 66 N1098 ----> C2734rwr/y F C3+R 1175 -415 76
 1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a R
 C3+R 1130 -415 80 310 1 cs_invvn 19c cs_invvn19c 45 N1097 ---->
 C2728rwr/y R C3+R 1130 -415 80 310 1 cs_invvn 16c
 cs_invvn16c 0 N1097 ----> C2728rwr/a F C3+R 1089 -415 72
 181 2 cs_invvn 16c cs_invvn16c 41 N1692 ---->{b} C2725rwr/y F
 C3+R 1089 -415 72 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
 C2725rwr/a R C3+R 1041 -415 132 161 2 cs_nnd2n 13c
 cs_nnd2n13c 48 N1479 ---->{c} C2721rwr/y R C3+R 1041 -415 132
 161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ----> C2721rwr/c F
 C3+R 969 -415 60 113 2 cs_nnd3n 12c cs_nnd3n12c 72 N892 ---->{d} C2338/y
 F C3+R 969 -415 60 113 2 cs_nnd2n 13c cs_nnd2n13c 0 N892 ----> C2338/a
 R C3+R 937 -415 72 124 3 cs_nnd2n 13c cs_nnd2n13c 32 N1119 ---->
 C2905/y R C3+R 937 -415 72 124 3 cs_invvn 13c
 cs_invvn13c 0 N1119 ----> C2905/a F C3+R 901 -415 63- 90
 13c cs_invvn13c 36 N2010 ---->{e} C2906/y F C3+R 901 -415
 63 90 1 cs_nor2n 12c cs_nor2n12c 0 N2010 ----> C2906/a
 R C3+R 868 -415 80 76 1 cs_nor2n 12c cs_nor2n12c 33 dcd_blk_dsucc ---->
 dcd_blk_dsucc R C3+R 868 -415 80 76 1 PI 0
 dcd_blk_dsucc

----- 3 eu_dsbl_aftr.reg_n.lat_0/BASE_REG/a F C3+R 1721 -401 0
 29 1 cl_invvn 05d cl_invvn05d 39 DELAY Setup eu_dsbl_aftr.reg_n.lat_0/BASE_REG/c1
 F C3- 160 60 221 13 cl_invvn 05d 1200 c1 ---->
 eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1721 -401 0 29 1 AND
 AND 0 DELAY ----> eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1769
 -401 98 16 1 AND AND -48 a ----> eu_dsbl_aftr.reg_n.lat_0/a
 R C3+R 1769 -401 98 16 1 PSEUDO_REG PSEUDO_REG 0 a ----> C2874/y
 R C3+R 1769 -401 98 16 1 cs_invvn 01c cs_invvn01c 0 N145 ----> C2874/a
 F C3+R 1718 -401 74 16 1 cs_invvn 01c cs_invvn01c 51 N1013 ---->{a}
 C2856/y F C3+R 1718 -401 74 16 1 cs_nnd2n 02c
 cs_nnd2n02c 0 N1013 ----> C2856/b R C3+R 1674 -401 109
 17 1 cs_nnd2n 02c cs_nnd2n02c 44 N522 ---->{b} C2833/y R
 C3+R 1674 -401 109 17 1 cs_nnd2n 02c cs_nnd2n02c 0 N522 ----> C2833/b
 F C3+R 1601 -401 124 234 14 cs_nnd2n 02c cs_nnd2n02c 73 N1290 ---->
 C2800/y F C3+R 1601 -401 124 234 14 cs_invvn 08c
 cs_invvn08c 0 N1290 ----> C2800/a R C3+R 1510 -401 166
 37 1 cs_invvn 08c cs_invvn08c 92 N1648 ---->{c} C2779/y R
 C3+R 1510 -401 166 37 1 cs_nnd2n 02c cs_nnd2n02c 0 N1648 ----> C2779/b
 F C3+R 1403 -401 134 107 6 cs_nnd2n 02c cs_nnd2n02c 106 N1645 ---->
 C2646/y F C3+R 1403 -401 134 107 6 cs_invvn 04c
 cs_invvn04c 0 N1645 ----> C2646/a R C3+R 1315 -401 122

```

21 1 cs_invvn          04c cs_invvn04c  89 N1746 ---->{d} C2620/y          R
C3+R 1315 -401 122 21 1 cs_nnd2n          02c cs_nnd2n02c  0 N1746 ----> C2620/b
F C3+R 1232 -401 134 67 4 cs_nnd2n          02c cs_nnd2n02c  83 N1740 ---->
C2602/y          F C3+R 1232 -401 134 67 4 cs_invvn          02c
cs_invvn02c  0 N1740 ----> C2602/a          R C3+R 1132 -401 168
37 2 cs_invvn          02c cs_invvn02c  100 N905 ---->{e} C2546/y          R
-401 168 37 2 cs_nnd2n          02c cs_nnd2n02c  0 N905 ----> C2546/b
F C3+R 1044 -401 68 17 1 cs_nnd2n          02c cs_nnd2n02c  88 N1647 ---->
C1928/y          F C3+R 1044 -401 68 17 1 cs_invvn          01c
cs_invvn01c  0 N1647 ----> C1928/a          R C3+R 988 -401 390
16 1 cs_invvn          01c cs_invvn01c  56 eu_iu_fxu_exc_cond ----> eu_iu_fxu_exc_cond
R C3+R 988 -401 390 16 1 PI          0 eu_iu_fxu_exc_cond

```

```

-----
> resize -trace 0 -examine 10 -local -critical -inc -rank ... INet N1692:b
has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9,
limit 290 INet N1692:a has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit
290; FALL: transition 381.9, limit 290 INet N1692:b has transition violation 1.904, multiplier 1
RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:a has transition
violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290
INet N1692:b has transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL:
transition 306.4, limit 290 INet N1692:a has transition violation 1.539, multiplier 1 RISE: transition
446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:b has transition violation 1.539,
multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:a has
transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit
290 INet N1692:b has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290;
FALL: transition 241.3, limit 290 INet N1692:a has transition violation 1.189, multiplier 1 RISE:
transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:b has transition violation
1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet
N1692:a has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition
241.3, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1,
limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier
1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition
violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290
INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL:
transition 513.2, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition
571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.97,
multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has
transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit
290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL:
transition 414.1, limit 290 INet N1479:a has transition violation 1.51, multiplier 1 RISE: transition
437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51,
ALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51, multiplier 1 RISE:
transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation
1.51, multiplier 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a
has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259,
limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290;
FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE:
transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation
1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a
has transition violation 1.006, multiplier 1 RISE: transition 291.7, limit 290; FALL: transition 210.4,
limit 290 INet N1479:a has transition violation 1.006, multiplier 1 RISE: transition 291.7, limit
290; FALL: transition 210.4, limit 290 INet N1479:a has transition violation 1.006, multiplier 1
RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition
violation 1.006, multiplier 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290
INet N1497:b has transition violation 2.291, multiplier 1 RISE: transition 664.4, limit 290; FALL:

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[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

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md:a has transition violation 1.214, multiplier 1 RISE: transition 352, limit 290; FALL: transition
346, limit 290 INet eu_iu_mmode:a has transition violation 1.124, multiplier 1 RISE: transition
326, limit 290; FALL: transition 326, limit 290 INet du_iu_hold_aa_req:a has transition violation
1.462, multiplier 1 RISE: transition 424, limit 290; FALL: transition 424, limit 290 INet
eu_iu_fpu_end_op:a has transition violation 1.169, multiplier 1 RISE: transition 339, limit 290;
FALL: transition 338, limit 290 INet eu_iu_misc_hold:c has transition violation 1.145, multiplier 1
RISE: transition 332, limit 290; FALL: transition 310, limit 290 INet clkg:clkg has cap violation
1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet du_iu_quiesced:a has transition
violation 1.166, multiplier 1 RISE: transition 338, limit 290; FALL: transition 338, limit 290 INet
iq_empty:iq_empty has cap violation 1.019, load 143.6, limit 141, multiplier 1 slack -383.8 INet
clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet
eu_iu_fxu_exc_cond:a has transition violation 1.345, multiplier 1 RISE: transition 390, limit 290;
FALL: transition 390, limit 290 INet du_iu_store_status(2):a has transition violation 1.724, multiplier
1 RISE: transition 500, limit 290; FALL: transition 500, limit 290 INet eu_iu_srlz_op_actn(0):a has
transition violation 1.29, multiplier 1 RISE: transition 366, limit 290; FALL: transition 374, limit
290 INet eu_iu_srlz_op_actn(1):a has transition violation 1.176, multiplier 1 RISE: transition 341,
limit 290; FALL: transition 341, limit 290 INet eu_iu_srlz_op_encode(0):a has transition violation
1.383, multiplier 1 RISE: transition 401, limit 290; FALL: transition 401, limit 290 INet
eu_iu_srlz_op_encode(1):a has transition violation 1.379, multiplier 1 RISE: transition 400, limit
290; FALL: transition 399, limit 290 INet eu_iu_srlz_op_encode(2):a has transition violation 1.448,
multiplier 1 RISE: transition 420, limit 290; FALL: transition 420, limit 290 INet
eu_iu_srlz_op_encode(3):a has transition violation 1.041, multiplier 1 RISE: transition 302, limit
290; FALL: transition 295, limit 290 INet eu_iu_srlz_op_encode(4):a has transition violation 1.4,
multiplier 1 RISE: transition 406, limit 290; FALL: transition 405, limit 290 INet
eu_iu_srlz_op_encode(5):a has transition violation 1.286, multiplier 1 RISE: transition 373, limit
290; FALL: transition 373, limit 290 INet eu_iu_srlz_op_encode(6):a has transition violation 1.221,
multiplier 1 RISE: transition 354, limit 290; FALL: transition 336, limit 290 INet
eu_iu_srlz_op_encode(7):a has transition violation 1.372, multiplier 1 RISE: transition 398, limit
290; FALL: transition 395, limit 290 INet eu_iu_srlz_op_encode(8):a has transition violation 1.266,
multiplier 1 RISE: transition 367, limit 290; FALL: transition 367, limit 290 INet
eu_iu_srlz_op_encode(9):a has transition violation 1.114, multiplier 1 RISE: transition 323, limit
290; FALL: transition 319, limit 290 INet eu_iu_srlz_op_encode(11):a has transition violation 1.724,
multiplier 1 RISE: transition 500, limit 290; FALL: transition 500, limit 290 INet
dcd_succ_last_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -415.6 INet
N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 611.4 INet N26:y has cap
violation 1.216, load 1218, limit 1001, multiplier 1 slack 377.5 INet N36:y has cap violation 1.179,
load 1180, limit 1001, multiplier 1 slack 613.3 INet N1098:y has cap violation 1.26, load 1261,
multiplier 1 slack -415.6 INet N2016:b has transition violation 1.023, multiplier 1 RISE: transition 296.8,
limit 290; FALL: transition 142.2, limit 290 INet gbfonet_2:y has cap violation 1.218, load 1219,
limit 1001, multiplier 1 slack 20.51 INet gbfonet_15:y has cap violation 1.169, load 1170, limit
1001, multiplier 1 slack 354.5 INet gbfonet_16:y has cap violation 1.108, load 1109, limit 1001,
multiplier 1 slack 480 IDesign IDCDSUC has 33 violations
> echo {Custom Synzilla
Report} Custom Synzilla Report
> ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0
upcells 122 IN ports 73 OUT ports 787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786
LINKED; 0 UNLINKED; 0 DC) 0 buses 1008 nets (0 multiply-driven; 0 undriven)
2632 pins (0 inversions) 2.61 pins per net 1551 literals 21 levels 10 max fanin
15 max fanout Cell Information FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area 0) PSEUDO_REG (ncount 83 : area 0)
cb_clk_32_1 (ncount 6 : area 480) cb_mode_block (ncount 1 : area
70) cs_ao12n03c (ncount 6 : area 24) cs_ao22n03c
(ncount 15 : area 90) cs_ao22n10c (ncount 1 : area 18)
cs_invvn01c (ncount 129 : area 258) cs_invvn02c (ncount 7 : area 14)
cs_invvn04c (ncount 5 : area 10) cs_invvn05c (ncount 13
: area 26) cs_invvn06c (ncount 9 : area 18)
cs_invvn07c (ncount 10 : area 20) cs_invvn08c (ncount 3 : area 12)

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cs_invvn09c (ncount 7:area 28)
:area 24) cs_invvn11c (ncount 5:area 30)
cs_invvn12c (ncount 21:area 126) cs_invvn13c (ncount 4:area 32)
cs_invvn14c (ncount 1:area 8) cs_invvn15c (ncount 4
:area 40) cs_invvn16c (ncount 3:area 42)
cs_invvn18c (ncount 1:area 20) cs_invvn19c (ncount 1:area 25)
cs_nnd2n02c (ncount 185:area 555) cs_nnd2n03c (ncount
3:area 9) cs_nnd2n04c (ncount 3:area 9)
cs_nnd2n05c (ncount 3:area 12) cs_nnd2n06c (ncount 1:area
4) cs_nnd2n07c (ncount 3:area 12) cs_nnd2n11c
(ncount 1:area 11) cs_nnd2n12c (ncount 1:area 12)
cs_nnd2n13c (ncount 4:area 60) cs_nnd2n14c (ncount 2:area
38) cs_nnd3n02c (ncount 27:area 108) cs_nnd3n07c
(ncount 2:area 12) cs_nnd3n09c (ncount 1:area 12)
cs_nnd3n12c (ncount 1:area 22) cs_nnd4n03c (ncount 6:area
30) cs_nnd4n09c (ncount 1:area 16) cs_nor2n02c
(ncount 10:area 30) cs_nor2n04c (ncount 2:area 6)
cs_nor2n12c (ncount 1:area 12) cs_nor3n03c (ncount 1:area 4)
cs_nor3n10c (ncount 1:area 12) cs_oa21n03c (ncount
1:area 5) cs_oa21n04c (ncount 1:area 5)
cs_oa21n05c (ncount 1:area 8) cs_oa22n03c (ncount 1:area
6) cs_xbn2n01b (ncount 1:area 8) cs_xbo2n01d
(ncount 1:area 8) Total Area = 2441 (Comb = 1891 : Non-Comb = 550)

```

```

> write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:57:44
1999 Part : IDCDSUC Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack Max. Endpoints: 2 Cause of Slack

```

```

Abbreviation Comparison/Description ----- Slack
Slack due to a point downstream on path Required Arrival Time RAT (ARRIVAL TIME <
REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME <
ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet (DATA ARRIVAL
TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST) Clock Gating Hold
ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK
ARRIVAL TIME + ADJUST) Hold Hold (DATA ARRIVAL TIME - HOLD >
CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC (DATA ARRIVAL TIME +
CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth ClkPW (CLOCK
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ClkSep
(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
LimitedAT/ Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```

```

----- 1 dcd_succ_last R C3+R 1345 -416 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
0 ----> C2744/y R C3+R 1345 -416 123 1078 7 cs_invvn
18c cs_invvn18c 0 dcd_succ_last_t1 ----> C2744/a F C3+R 1279
-416 83 302 4 cs_invvn 18c cs_invvn18c 66 N675 ---->{a} C2738/y
F C3+R 1279 -416 83 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---->
C2738/b R C3+R 1228 -416 118 1261 4 cs_nnd2n 14c
cs_nnd2n14c 50 N1098 ----> C2734rwr/y R C3+R 1228 -416 118
1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a F

```

```

C3+R 1172 -416 54 310 1 cs_invvn 19c cs_invvn19c 56 N1097 ---->
C2728rwr/y F C3+R 1172 -416 54 310 1 cs_invvn 16c
cs_invvn16c 0 N1097 ----> C2728rwr/a R C3+R 1139 -416 104
181 2 cs_invvn 16c cs_invvn16c 33 N1692 ---->{b} C2725rwr/y R
C3+R 1139 -416 104 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
C2725rwr/a F C3+R 1083 -416 91 161 2 cs_nnd2n 13c
cs_nnd2n13c 56 N1479 ---->{c} C2721rwr/y F C3+R 1083 -416 91
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ----> C2721rwr/a
R C3+R 1019 -416 199 115 2 cs_nnd3n 12c cs_nnd3n12c 65 N1497 ---->{d}
R C3+R 1019 -416 199 115 2 cs_nor3n 10c cs_nor3n10c 0
N1497 ----> C2709rwr/c F C3+R 907 -416 92 52 1 cs_nor3n
10c cs_nor3n10c 111 N1976 ---->{e} C2579rwr_0_0/y F C3+R 907 -416
92 52 1 cs_nnd3n 07c cs_nnd3n07c 0 N1976 ----> C2579rwr_0_0/c
R C3+R 849 -416 189 47 2 cs_nnd3n 07c cs_nnd3n07c 58 N1719 ---->{f}
C2599rwr_0_0_0/y R C3+R 849 -416 189 47 2 cs_nor2n 04c
cs_nor2n04c 0 N1719 ----> C2599rwr_0_0_0/b F C3+R 747 -416 109
21 1 cs_nor2n 04c cs_nor2n04c 102 N1956 ---->{g} C2440rwr/y F
C3+R 747 -416 109 21 1 cs_nnd4n 03c cs_nnd4n03c 0 N1956 ---->
C2440rwr/b R C3+R 679 -416 144 18 1 cs_nnd4n 03c
cs_nnd4n03c 68 N283 ---->{h} C2318/y R C3+R 679 -416 144
18 1 cs_oa21n 04c cs_oa21n04c 0 N283 ----> C2318/a1 F
C3+R 598 -416 81 37 2 cs_oa21n 04c cs_oa21n04c 81 three_branches ---->
three_branches F C3+R 598 -416 81 37 2 PI 0
three_branches

```

```

----- 2 dcd_succ_last F C3+R 1294 -415 79 1078 7
PO 0 dcd_succ_last_t1 RAT 879
0 ----> C2744/y F C3+R 1294 -415 79 1078 7 cs_invvn
18c cs_invvn18c 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1241
-415 119 302 4 cs_invvn 18c cs_invvn18c 53 N675 ---->{a} C2738/y
R C3+R 1241 -415 119 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---->
C2738/b F C3+R 1175 -415 76 1261 4 cs_nnd2n 14c
cs_nnd2n14c 66 N1098 ----> C2734rwr/y F C3+R 1175 -415 76
1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a R
C3+R 1130 -415 80 310 1 cs_invvn 19c cs_invvn19c 45 N1097 ---->
C2728rwr/y R C3+R 1130 -415 80 310 1 cs_invvn 16c
cs_invvn16c 0 N1097 ----> C2728rwr/a F C3+R 1089 -415 72
181 2 cs_invvn 16c cs_invvn16c 41 N1692 ---->{b} C2725rwr/y F
C3+R 1089 -415 72 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
C2725rwr/a R C3+R 1041 -415 132 161 2 cs_nnd2n 13c
cs_nnd2n13c 48 N1479 ---->{c} C2721rwr/y R C3+R 1041 -415 132
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ----> C2721rwr/c F
12c cs_nnd3n12c 72 N892 ---->{d} C2338/y F C3+R 969
-415 60 113 2 cs_nnd2n 13c cs_nnd2n13c 0 N892 ----> C2338/a
R C3+R 937 -415 72 124 3 cs_nnd2n 13c cs_nnd2n13c 32 N1119 ---->
C2905/y R C3+R 937 -415 72 124 3 cs_invvn 13c
cs_invvn13c 0 N1119 ----> C2905/a F C3+R 901 -415 63 90
1 cs_invvn 13c cs_invvn13c 36 N2010 ---->{e} C2906/y F C3+R
901 -415 63 90 1 cs_nor2n 12c cs_nor2n12c 0 N2010 ----> C2906/a
R C3+R 868 -415 80 76 1 cs_nor2n 12c cs_nor2n12c 33 dcd_blk_dsucc ---->
dcd_blk_dsucc R C3+R 868 -415 80 76 1 PI 0
dcd_blk_dsucc

```

```

-----
> report_area Design: /IDCDSUC - Area: 4516.000000, Area(Weight):
2441.000000 > cputime Used 14.14 cpu seconds or 00:00:15 wall time, used 0 bytes or 0

```

```

byte.      > echo {=== Discretization process finished ===} === Discretization process finished ===
Good names for IDCDSUC      Count      User      Transform      New For all nets
1008      556      0      452 For all nets      1008      55.16%      0.00%      44.84% For I/O
port nets      195      68.72%      0.00%      31.28% For register output nets      166      100.00%
0.00%      0.00%      Count      User      Transform      New For all boxes
787      290      22      475 For all boxes      787      36.85%      2.80%      60.36% For
register boxes      83      100.00%      0.00%      0.00% For linked boxes      786
36.90%      2.80%      60.31%      > echo {Custom Synzilla Report} Custom Synzilla Report
> ps -cell Design /HISVHDL/IDCDSUC has:      1 instances      0 upcells      122 IN ports      73 OUT ports
787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC)      0 buses      1008 nets (0
multiply-driven; 0 undriven)      2632 pins (0 inversions)      2.61 pins per net      1551 literals
21 levels      10 max fanin      15 max fanout      Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)      PSEUDO_REG (ncount
83 : area 0)      cb_clk_32_1 (ncount 6 : area 480)
cb_mode_block (ncount 1 : area 70)      cs_ao12n03c (ncount 6 : area
24)      cs_ao22n03c (ncount 15 : area 90)      cs_ao22n10c
(ncount 1 : area 18)      cs_invvn01c (ncount 129 : area 258)
cs_invvn02c (ncount 7 : area 14)      cs_invvn04c (ncount 5 : area 10)
: area 18)      cs_invvn05c (ncount 13 : area 26)      cs_invvn06c (ncount 9
: area 18)      cs_invvn07c (ncount 10 : area 20)
cs_invvn08c (ncount 3 : area 12)      cs_invvn09c (ncount 7 : area 28)
: area 30)      cs_invvn10c (ncount 6 : area 24)      cs_invvn11c (ncount 5
: area 30)      cs_invvn12c (ncount 21 : area 126)
cs_invvn13c (ncount 4 : area 32)      cs_invvn14c (ncount 1 : area 8)
: area 42)      cs_invvn15c (ncount 4 : area 40)      cs_invvn16c (ncount 3
: area 42)      cs_invvn18c (ncount 1 : area 20)
cs_invvn19c (ncount 1 : area 25)      cs_nnd2n02c (ncount 185 : area
555)      cs_nnd2n03c (ncount 3 : area 9)      cs_nnd2n04c
rea 9)      cs_nnd2n05c (ncount 3 : area 12)      cs_nnd2n06c
(ncount 1 : area 4)      cs_nnd2n07c (ncount 3 : area 12)
cs_nnd2n11c (ncount 1 : area 11)      cs_nnd2n12c (ncount 1 : area
12)      cs_nnd2n13c (ncount 4 : area 60)      cs_nnd2n14c
(ncount 2 : area 38)      cs_nnd3n02c (ncount 27 : area 108)
cs_nnd3n07c (ncount 2 : area 12)      cs_nnd3n09c (ncount 1 : area
12)      cs_nnd3n12c (ncount 1 : area 22)      cs_nnd4n03c
(ncount 6 : area 30)      cs_nnd4n09c (ncount 1 : area 16)
cs_nor2n02c (ncount 10 : area 30)      cs_nor2n04c (ncount 2 : area 6)
: area 4)      cs_nor2n12c (ncount 1 : area 12)      cs_nor3n03c (ncount 1
(ncount 1 : area 5)      cs_oa21n04c (ncount 1 : area 5)      cs_oa21n03c
cs_oa21n05c (ncount 1 : area 8)      cs_oa22n03c (ncount 1 : area
6)      cs_xbn2n01b (ncount 1 : area 8)      cs_xbo2n01d
(ncount 1 : area 8)      Total Area = 2441 (Comb = 1891 : Non-Comb = 550)
> write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report      for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.      Sun Apr 18 21:57:46
1999 Part : IDCDSUC Mode : Late Mode / Nominal      EDA EinsTimer EndPoint Report
Release Level : 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack      Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description -----
Continuation      SlkCont      Slack due to a point downstream on path      Required Arrival Time
RAT      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)      Asserted Required Arrival Time AssrtRAT
( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)      Clock Gating Setup      ClkGSet      (
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST )      Clock Gating
Hold      ClkGHld      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
+ ADJUST )      Clock Tree Pulse Width      ClkTPW      ( CLOCK LEADING EDGE + PULSE WIDTH <

```

CLOCK TRAILING EDGE) Setup (DATA ARRIVAL TIME + SETUP <
 CLOCK ARRIVAL TIME + ADJUST) Hold (DATA ARRIVAL TIME - HOLD
 > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC (DATA ARRIVAL TIME
 + CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth ClkPW (CLOCK
 LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ClkSep
 (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
 ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
 LimitedAT/ Delay/ Failed Test/ Test PinName
 E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName

```

----- 1 dcd_succ_last R C3+R 1345 -416 123 1078 7
PO 0 dcd_succ_last_t1 RAT 929
1345 -416 123 1078 7 cs_invvn 18c cs_invvn18c 0 dcd_succ_last_t1 ---->
C2744/a F C3+R 1279 -416 83 302 4 cs_invvn 18c
cs_invvn18c 66 N675 ---->{a} C2738/y F C3+R 1279 -416 83
302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ----> C2738/b R
C3+R 1228 -416 118 1261 4 cs_nnd2n 14c cs_nnd2n14c 50 N1098 ---->
C2734rwr/y R C3+R 1228 -416 118 1261 4 cs_invvn 19c
cs_invvn19c 0 N1098 ----> C2734rwr/a F C3+R 1172 -416 54
310 1 cs_invvn 19c cs_invvn19c 56 N1097 ----> C2728rwr/y F
C3+R 1172 -416 54 310 1 cs_invvn 16c cs_invvn16c 0 N1097 ---->
C2728rwr/a R C3+R 1139 -416 104 181 2 cs_invvn 16c
cs_invvn16c 33 N1692 ---->{b} C2725rwr/y R C3+R 1139 -416 104
181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ----> C2725rwr/a
F C3+R 1083 -416 91 161 2 cs_nnd2n 13c cs_nnd2n13c 56 N1479 ---->{c}
C2721rwr/y F C3+R 1083 -416 91 161 2 cs_nnd3n 12c
cs_nnd3n12c 0 N1479 ----> C2721rwr/a R C3+R 1019 -416 199
115 2 cs_nnd3n 12c cs_nnd3n12c 65 N1497 ---->{d} C2709rwr/y
R C3+R 1019 -416 199 115 2 cs_nor3n 10c cs_nor3n10c 0 N1497 ---->
C2709rwr/c F C3+R 907 -416 92 52 1 cs_nor3n 10c
cs_nor3n10c 111 N1976 ---->{e} C2579rwr_0_0/y F C3+R 907 -416 92
52 1 cs_nnd3n 07c cs_nnd3n07c 0 N1976 ----> C2579rwr_0_0/c
R C3+R 849 -416 189 47 2 cs_nnd3n 07c cs_nnd3n07c 58 N1719 ---->{f}
C2599rwr_0_0_0/y R C3+R 849 -416 189 47 2 cs_nor2n 04c
cs_nor2n04c 0 N1719 ----> C2599rwr_0_0_0/b F C3+R 747 -416 109
21 1 cs_nor2n 04c cs_nor2n04c 102 N1956 ---->{g} C2440rwr/y F
C3+R 747 -416 109 21 1 cs_nnd4n 03c cs_nnd4n03c 0 N1956 ---->
C2440rwr/b R C3+R 679 -416 144 18 1 cs_nnd4n 03c
cs_nnd4n03c 68 N283 ---->{h} C2318/y R C3+R 679 -416 144
18 1 cs_oa21n 04c cs_oa21n04c 0 N283 ----> C2318/a1 F
C3+R 598 -416 81 37 2 cs_oa21n 04c cs_oa21n04c 81 three_branches ---->
three_branches F C3+R 598 -416 81 37 2 PI 0
three_branches

```

```

----- 2 dcd_succ_last F C3+R 1294 -415 79 1078 7
0 ----> C2744/y F C3+R 1294 -415 79 1078 7 cs_invvn
18c cs_invvn18c 0 dcd_succ_last_t1 ----> C2744/a R C3+R 1241
-415 119 302 4 cs_invvn 18c cs_invvn18c 53 N675 ---->{a} C2738/y
R C3+R 1241 -415 119 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---->
C2738/b F C3+R 1175 -415 76 1261 4 cs_nnd2n 14c
cs_nnd2n14c 66 N1098 ----> C2734rwr/y F C3+R 1175 -415 76
1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a R
C3+R 1130 -415 80 310 1 cs_invvn 19c cs_invvn19c 45 N1097 ---->
C2728rwr/y R C3+R 1130 -415 80 310 1 cs_invvn 16c

```

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cs_invvn16c 0 N1097 ----> C2728rwr/a F C3+R 1089 -415 72
181 2 cs_invvn 16c cs_invvn16c 41 N1692 ---->{b} C2725rwr/y F
C3+R 1089 -415 72 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
C2725rwr/a R C3+R 1041 -415 132 161 2 cs_nnd2n 13c
cs_nnd2n13c 48 N1479 ---->{c} C2721rwr/y R C3+R 1041 -415 132
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ----> C2721rwr/c F
C3+R 969 -415 60 113 2 cs_nnd3n 12c cs_nnd3n12c 72 N892 ---->{d} C2338/y
F C3+R 969 -415 60 113 2 cs_nnd2n 13c cs_nnd2n13c 0 N892 ----> C2338/a
R C3+R 937 -415 72 124 3 cs_nnd2n 13c cs_nnd2n13c 32 N1119 ---->
C2905/y R C3+R 937 -415 72 124 3 cs_invvn 13c
cs_invvn13c 0 N1119 ----> C2905/a F C3+R 901 -415 63 90
1 cs_invvn 13c cs_invvn13c 36 N2010 ---->{e} C2906/y F C3+R
901 -415 63 90 1 cs_nor2n 12c cs_nor2n12c 0 N2010 ----> C2906/a
R C3+R 868 -415 80 76 1 cs_nor2n 12c cs_nor2n12c 33 dcd_blk_dsucc ---->
dcd_blk_dsucc R C3+R 868 -415 80 76 1 PI 0
dcd_blk_dsucc

```

```

-----
> report_area Design: /IDCDSUC - Area: 4516.000000, Area(Weight):
2441.000000 > cputime Used 1.71 cpu seconds or 00:00:01 wall time, used 0 bytes or 0 byte.
[hnl_attr]: Attributes registered for copy for type: PORT. MASK_ANYTHING_MASKED_ON_PORT
[hnl_attr]: Attributes registered for copy for type: CELL. MASK_ANYTHING_MASKED_ON_CELL
MASK_USER_CELL_NOCHANGE MASK_USER_CELL_NODESTROY
MASK_USER_CELL_NOTOUCH SUGGESTED_LIBRARY_CELL SUGGESTED_PARALLEL_FANOUT
SUGGESTED_SIZE SUGGESTED_SWAP SYN_USAGE_BOX_HIDE [hnl_attr]: Attributes registered for
copy for type: PIN. MASK_ANYTHING_MASKED_ON_PIN MASK_USER_PIN_NOADD
MASK_USER_PIN_NOCHANGE MASK_USER_PIN_NONEWNET MASK_USER_PIN_NOTOUCH
SUGGESTED_SERIAL_FANOUT SYN_SAS_NAME [hnl_attr]: Attributes registered for copy for type:
nl_attr]: 0 port(s) have attribute(s) registered for copy. [hnl_attr]: 197 cell(s) have attribute(s) registered for
copy. [hnl_attr]: 10 net(s) have attribute(s) registered for copy. [hnl_attr]: 1242 pin(s) have attribute(s)
registered for copy. [hnl_attr]: Attributes registered for copy for type: PORT.
MASK_ANYTHING_MASKED_ON_PORT [hnl_attr]: Attributes registered for copy for type: CELL.
MASK_ANYTHING_MASKED_ON_CELL MASK_USER_CELL_NOCHANGE
MASK_USER_CELL_NODESTROY MASK_USER_CELL_NOTOUCH SUGGESTED_LIBRARY_CELL
SUGGESTED_PARALLEL_FANOUT SUGGESTED_SIZE SUGGESTED_SWAP
SYN_USAGE_BOX_HIDE [hnl_attr]: Attributes registered for copy for type: PIN.
MASK_ANYTHING_MASKED_ON_PIN MASK_USER_PIN_NOADD MASK_USER_PIN_NOCHANGE
MASK_USER_PIN_NONEWNET MASK_USER_PIN_NOTOUCH SUGGESTED_SERIAL_FANOUT
SYN_SAS_NAME [hnl_attr]: Attributes registered for copy for type: NET.
MASK_ANYTHING_MASKED_ON_NET MASK_USER_NET_NOTOUCH [hnl_attr]: 0 port(s) have
attribute(s) registered for copy. [hnl_attr]: 197 cell(s) have attribute(s) registered for copy. [hnl_attr]: 10
net(s) have attribute(s) registered for copy. [hnl_attr]: 1242 pin(s) have attribute(s) registered for copy.
> add_reg -idesign __CiType_13_30da5570 -cloning 100 [SYNZ_MAP-2]: Inserting an inverter, instead of
cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and

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[illegible]

PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-1]: Cloning gate 'C2622' of type
'cs_nor2n02c' [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
T-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-1]: Cloning gate 'C1959' of type
'cs_invvn01c' [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. add_reg processed 83 register cells-Inserted
22 inverters: Pls or reg driven or brkpt 5 Instead of cloning 16
No matching register input 1.Cloned gates 4 Unmapped registers 0 ***** end Synzilla *****
SYNZPROMPT

□[10Creturn_to_bdz > hnl::hnl_nets_preserve -restore > write_vim -dir
/data/lacey/synztmp/IDCDSUC/IDCDSUC -r -... [VIM-7701]: Design: IDCDSUC :: Writing DEF:
/data/lacey/synztmp/IDCDSUC/IDCDSUC/DEF/IDCDSUC, View:
/data/lacey/synztmp/IDCDSUC/IDCDSUC/HISVHDL/IDCDSUC. [VIM-7721]: Unmapped constant cell(s)
skipped: 1. [VIM-7722]: BRKPT cell(s) processed: 180. > echo NORMAL_RETURN >
use_cds
> read_vim -library /data/lacey/synztmp/IDCDSUC/IDCDSUC -...
[ET-112]: Deleting timing for design: IDCDSUC, analysis mode:default, and below.

Reading proto IDCDSUC...

> padnet
> msg::set_level -msgid ICM-23 -hidden
> read_timer_parms -file /data/lacey/synztmp/IDCDSUC/IDCD...
[ICM-15]: >Begin...Parm Reader
for file /data/lacey/synztmp/IDCDSUC/IDCDSUC.tparms.
[ICM-16]: <End.....Parm Reader.

> msg::set_level -msgid ICM-23 -error
> hide_clock_tree -hierarchy
[ET-203]: Timing top level created for design: IDCDSUC, analysis mode: default.

[ET-415]: Timer/Delay computation has been triggered.

[ET-27]: No subsequent messages of this type will be reported.

Increase timing debug level for complete set of these messages.
[ET-601]: (W) The model build for block: gptr_latch, cell name: cb_mode_block failed.
Default modelling will be used for this block.
0 gates were hidden.

> is_parm no_tech_redund
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/rm_tech_redund.tcl

> EMarkOriginalBoxes
> str_parm tgfs_effort
> is_parm remove_redundant_regs
> make_constants_in nonreg_only
> ignore_trivial_expansions EQNVIEW

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/ECgenexp.tcl

> expansions_from_tib EQNVIEW
> expansions_from_eqn EQNVIEW
> copy_def_to_proto EQNVIEW
> apply_decide_boolean(EQNVIEW)

generated 1 paths in 70 milliseconds

> apply_Hstructure(EQNVIEW)

generated 1 paths in 40 milliseconds

> gen_nonreg_tib_expns TIB_EXPANSIONS
> apply_Hunstructure()
> expandable_name

> set_nochange
> constmod mark_modified_boxes
> is_parm keep_bad_pgroups
> bad_pgroups_expandable
> nextbox_with_test {test_key(SYN_H_modified_box) simpl...
> nextbox_with_test {test_key(SYN_H_modified_box) simpl...
> headless
> cleanse1
> nochange
> set_nochange
> constmod mark_modified_boxes
> is_parm keep_bad_pgroups
> bad_pgroups_expandable
> nextbox_with_test {test_key(SYN_H_modified_box) simpl...
> nextbox_with_test {test_key(SYN_H_modified_box) simpl...
> headless
> cleanse1
> nochange

> set_nochange
> apply {Hstructure(EQNVIEW TIB_EXPANSIONS)}

generated 1 paths in 60 milliseconds

> rtoibox {Htgfsredund(100)}
> apply_Hunstructure()
> nochange
> DeleteAllProtosUnderView TIB_EXPANSIONS

[SRULE-17175]: Deleted 5 Proto Boxes

> randsim q
> randsim q
> is_parm keep_bad_pgroups
> copyinfo
> fix_bad_pgroups
> basetype
> copyinfo

- > nextbox {mapprim, mapterm}
- > cleanse
- > nextbox tchname(NOERR)
- > cleanse
- > copyinfo
- > has_children CONSTANT
 - > tiegen FOLIM(8)
- > nextbox {EChideBoxes(ALL OLD HIDE)}
- > nextbox {EChideBoxes(PERI OLD RESTORE)}
- > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...
- > compare_key_slack_limit TIME_REDUND

[ET-1301]: (W) Applied default arrival time for
boundary pin clk.

[ET-27]: No subsequent messages of this type will be reported.
Increase timing debug level for complete set of these messages.

[ET-413]: (W) Using default pin capacitance 0.200000 for boundary output pin scan_out.

[ET-27]: No subsequent messages of this type will be reported.
Increase timing debug level for complete set of these messages.

[ET-1302]: (W) Applied default required arrival time for
boundary pin scan_out.

[ET-27]: No subsequent messages of this type will be reported.
Increase timing debug level for complete set of these messages.

- > reset_key_slack_limit TIME_REDUND
- > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
- > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS)}
- > compare_key_slack_limit TIME_REDUND
- > delete_key_slack_limit TIME_REDUND
- > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
- > quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
- > nextbox {EChideBoxes(ALL OLD RESTORE)}
- > ECdeleteAllKeys

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_setup_timer.tcl

> ::setup_timer

[make_feedthru_boxes]: IOPADs, BRKPTs, etc. set to FEEDTHRU boxes.

[set_slew_prop]: Setting slew propagation to 0 (OFF)

[setup_timer]: ETE_CAP_LIMIT_MODE parm or env.var. was not set.

[setup_timer]: Default cap limit formula will be used.

[setup_timer]: GLOBAL_SLEW_LIMIT parm or env.var. was not set.

[setup_timer]: Delay-rule limits will be used.

[ET-110]: License obtained for EinsTimer_Statistics 1.1

[set_LM_and_EM_delay_combinations]: Global linear combination box delay (LCD) multipliers have been set:

[set_LM_and_EM_delay_combinations]: Linear combination box delay (LCD) multipliers have been set for default amode:

[set_LM_and_EM_delay_combinations]: LM_WC = 1, LM_BC = 0, LM_NOM = 0

[set_LM_and_EM_delay_combinations]: EM_WC = 1, EM_BC = 0, EM_NOM = 0

[setup_timer]: BOX_DELAY_MULTIPLIER parm or env.var. was not set.

[setup_timer]: Box dly multiplier will not be set. Default = 1.0

[use_clock_overrides]: Clock override usage has been set to NO.

[set_timer_msg_function]: EinsTimer message handler was set to synmsg.

[set_timer_good_reg_function]: EinsTimer good-reg-function was set to the default (good_reg_name).

[set_tib_timing_coefficients]: Asserting TIB delays:

[set_tib_timing_coefficients]: TIB_GATE_DLY = 100, TIB_FANIN_DLY = 10, TIB_FANOUT_DLY = 0,

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[set_tib_timing_coefficients]: TIB_R_OUT = 0.3, TIB_PINCAP = 20,
[set_tib_timing_coefficients]: TIB_SETUP = 0, TIB_HOLD = 0
[set_clock_gate_constraints]: Clock gate constraints set: SETUP=100, HOLD=100, PW=0.
[setup_timer]: Setting up the cap and RC subsystem.
[set_cap_calc]: ETE-style net cap estimation turned ON.
[set_cap_calc]: ETE techEST rule will be used for wire cap estimation.
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll-rs6000/pdlink.dll
pdlink.dll version 4.1 (Apr 14 1999 17:21:59)
[set_rc_calc]: ETE-style RC estimation turned ON.
[set_rc_calc]: ETE RCN rule will be used.
[set_rc_calc]: RC delays and slew effects turned OFF!.
[setup_timer]: ETE ESTRULE parm or env.var. was not set.
[setup_timer]: ETE wire ESTimation rule will not be read.
[setup_timer]: ETE RCN parm or env.var. was not set.
[setup_timer]: ETE RCN rule will not be read.
[setup_timer]: ETEPATH environment variable not set
> read_timer_parms -file /afs/apd/func/vlsi/alliance00/tim...
[ICM-15]: >Begin...Parm Reader
for file /afs/apd/func/vlsi/alliance00/timing/parms/cpsynz.parms.
[ICM-16]: <End.....Parm Reader.

> set_cap_limit_formula TYPE0
> set_slew_prop ON
[set_slew_prop]: Setting slew propagation to 1 (ON)
> set_net_delay_calc -mode_noest
[CTE::gp390_setup_timer]: setting nominal delay mode
> set_delay_mode -nominal
> set_vdd -vdd_best 1.7 -vdd_worst 1.45 -vdd_nominal 1.45
> set_temp -temp_best -10 -temp_worst 10 -temp_nominal 10
> use_clock_overrides YES
[use_clock_overrides]: Clock override usage has been set to YES.
> read_phase_file -file /afs/apd/func/vlsi/alliance00/bssc...
[ET-0018]: >Begin...PHASE reader
for file /afs/apd/func/vlsi/alliance00/bssc8/v4/ndr/a00.phase.
[ET-0019]: <End.....PHASE reader.

> set_default_slew -slew 151
> idm::all_inputs
> set_max_capacitance -cap 141 -ports {op_dsbl_after eu_iu...
> set_default_pincap -value 1001
> idm::all_outputs
> set_max_transition -time 301 -ports {iu_eu_opcode_cmp iu...
> read_assertions -path /afs/apd/func/vlsi/alliance00/timi...
[ET-0018]: >Begin...PIS reader
for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pis.
[ET-0016]: (E) Pin/Net: aa_blk_dcd_prt! not found on line no: 31.

[ET-0016]: (E) Pin/Net: clkg0 not found on line no: 132.

[ET-0016]: (E) Pin/Net: clkg_0 not found on line no: 133.

[ET-0016]: (E) Pin/Net: clkg_00 not found on line no: 134.

[ET-0016]: (E) Pin/Net: clkg1 not found on line no: 135.

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[ET-0016]: (E) Pin/Net: clkg_1 not found on line no: 136.

[ET-0016]: (E) Pin/Net: clkg_01 not found on line no: 137.

[ET-0016]: (E) Pin/Net: clkg_2 not found on line no: 139.

[ET-0016]: (E) Pin/Net: clkg_02 not found on line no: 140.

[ET-0016]: (E) Pin/Net: clkg3 not found on line no: 141.

[ET-0016]: (E) Pin/Net: clkg_3 not found on line no: 142.

[ET-0016]: (E) Pin/Net: clkg_03 not found on line no: 143.

[ET-0016]: (E) Pin/Net: clkg4 not found on line no: 144.

[ET-0016]: (E) Pin/Net: clkg_4 not found on line no: 145.

[ET-0016]: (E) Pin/Net: clkg_04 not found on line no: 146.

[ET-0016]: (E) Pin/Net: clkg5 not found on line no: 147.

[ET-0016]: (E) Pin/Net: clkg_5 not found on line no: 148.

[ET-0016]: (E) Pin/Net: clkg_05 not found on line no: 149.

[ET-0016]: (E) Pin/Net: clkg6 not found on line no: 150.

[ET-0016]: (E) Pin/Net: clkg_6 not found on line no: 151.

[ET-0016]: (E) Pin/Net: clkg_06 not found on line no: 152.

[ET-0016]: (E) Pin/Net: clkg7 not found on line no: 153.

[ET-0016]: (E) Pin/Net: clkg_7 not found on line no: 154.

[ET-0016]: (E) Pin/Net: clkg_07 not found on line no: 155.

[ET-0016]: (E) Pin/Net: clkg8 not found on line no: 156.

[ET-0016]: (E) Pin/Net: clkg_8 not found on line no: 157.

[ET-0016]: (E) Pin/Net: clkg_08 not found on line no: 158.

[ET-0016]: (E) Pin/Net: clkg9 not found on line no: 159.

[ET-0016]: (E) Pin/Net: clkg_9 not found on line no: 160.

[ET-0016]: (E) Pin/Net: clkg_09 not found on line no: 161.

[ET-0016]: (E) Pin/Net: clkg11 not found on line no: 162.

[ET-0016]: (E) Pin/Net: clkg22 not found on line no: 163.

[ET-0016]: (E) Pin/Net: clkg33 not found on line no: 164.

[ET-0019]: <End.....PIS reader.

[ET-0018]: >Begin...ETA reader

for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.eta.

[ET-0019]: <End.....ETA reader.

[ET-0018]: >Begin...POS reader

for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pos.

[ET-0019]: <End.....POS reader.

> idm::all_inputs

- > get_asserted_phases -pin op_dsbl_after -at
- > get_asserted_phases -pin eu_iu_spare1 -at
- > get_asserted_phases -pin second_op_lat -at
- > get_asserted_phases -pin mcr41_trap -at
- > get_asserted_phases -pin ifet_xcptn -at
- > get_asserted_phases -pin iu_eu_xcpt_pend -at
- > get_asserted_phases -pin iq_blk_d1 -at
- > get_asserted_phases -pin clk1_mode7 -at

Pin: NO PHASES for clk1_mode7: asserting default C3+R

- > set_arrival -time 401 -phase C3+R -ports clk1_mode7 -late
- > set_arrival -time 101 -phase C3+R -ports clk1_mode7 -early
- > get_asserted_phases -pin dcd_op_44 -at
- > get_asserted_phases -pin ru_write_in_iq -at
- > get_asserted_phases -pin a_clk -at

Pin: NO PHASES for a_clk: asserting default C3+R

- > set_arrival -time 401 -phase C3+R -ports a_clk -late
- > set_arrival -time 101 -phase C3+R -ports a_clk -early
- > get_asserted_phases -pin b_clk -at

Pin: NO PHASES for b_clk: asserting default C3+R

- > set_arrival -time 401 -phase C3+R -ports b_clk -late
- > set_arrival -time 101 -phase C3+R -ports b_clk -early
- > get_asserted_phases -pin ru_iu_rcvy_rst -at
- > get_asserted_phases -pin eu_iu_enter_slow_md -at
- > get_asserted_phases -pin id_instr_stores -at
- > get_asserted_phases -pin op_inq_stores -at
- > get_asserted_phases -pin test_c1 -at

Pin: NO PHASES for test_c1: asserting default C3+R

- > set_arrival -time 401 -phase C3+R -ports test_c1 -late
- > set_arrival -time 101 -phase C3+R -ports test_c1 -early
- > get_asserted_phases -pin iq_blk_aa -at
- > get_asserted_phases -pin aa_ofc_available -at
- > get_asserted_phases -pin eu_iu_mmode -at
- > get_asserted_phases -pin eu_iu_mcset_e1 -at
- > get_asserted_phases -pin aa_ofc_hold -at
- > get_asserted_phases -pin ru_98_43 -at
- > get_asserted_phases -pin srlz_op_match -at
- > get_asserted_phases -pin first_op_lat -at
- > get_asserted_phases -pin zero_branches -at
- > get_asserted_phases -pin dcd_mcr41_blk -at
- > get_asserted_phases -pin xu_iu_xlat_busy -at
- > get_asserted_phases -pin du_iu_hold_aa_req -at
- > get_asserted_phases -pin eu_iu_fpu_end_op -at
- > get_asserted_phases -pin eu_iu_misc_hold -at
- > get_asserted_phases -pin op_cmp_raw -at

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> get_asserted_phases -pin op_dsbl_before -at
> get_asserted_phases -pin op_drain -at
> get_asserted_phases -pin eu_iu_fxu_end_op -at
> get_asserted_phases -pin op_mcend_raw -at
> get_asserted_phases -pin eu_iu_br_wrong -at
> get_asserted_phases -pin need_opnd_req -at
> get_asserted_phases -pin legal_bht_br -at
> get_asserted_phases -pin clkg -at
> get_asserted_phases -pin bht_branch_req -at
Pin: NO PHASES for bht_branch_req: asserting default C3+R
  > set_arrival -time 401 -phase C3+R -ports bht_branch_req ...
  > set_arrival -time 101 -phase C3+R -ports bht_branch_req ...
> get_asserted_phases -pin id_ex_in_mm -at
> get_asserted_phases -pin du_iu_quiesced -at
> get_asserted_phases -pin iu_op_cmp_hit_a -at
> get_asserted_phases -pin iu_op_cmp_hit_b -at
> get_asserted_phases -pin iu_op_cmp_hit_c -at
> get_asserted_phases -pin iu_op_cmp_hit_d -at
> get_asserted_phases -pin dcd_frc_milli -at
> get_asserted_phases -pin iq_empty -at
> get_asserted_phases -pin op_serialize -at
> get_asserted_phases -pin gp_tr_scan_in -at
Pin: NO PHASES for gp_tr_scan_in: asserting default C3+R
  > set_arrival -time 401 -phase C3+R -ports gp_tr_scan_in -late
  > set_arrival -time 101 -phase C3+R -ports gp_tr_scan_in -e...
> get_asserted_phases -pin aa_agi_lat -at
> get_asserted_phases -pin branch_request -at
> get_asserted_phases -pin ru_9a_52 -at
> get_asserted_phases -pin bu_iu_quiesced -at
> get_asserted_phases -pin dcd_blk_dsucc -at
> get_asserted_phases -pin op_eim_dcd -at
> get_asserted_phases -pin iqrcode_mod_390gr -at
> get_asserted_phases -pin scan_in -at
Pin: NO PHASES for scan_in: asserting default C3+R
  > set_arrival -time 401 -phase C3+R -ports scan_in -late
  > set_arrival -time 101 -phase C3+R -ports scan_in -early
> get_asserted_phases -pin eu_iu_e1_exc_cond -at
> get_asserted_phases -pin aa_ofc_block_req -at
> get_asserted_phases -pin eu_iu_fpu_excptn -at
> get_asserted_phases -pin block_aa_branch -at
> get_asserted_phases -pin ru_iu_rq_blk -at
> get_asserted_phases -pin op_chkpt_synch -at
> get_asserted_phases -pin ireg_valid -at
> get_asserted_phases -pin ru_9a_36 -at
> get_asserted_phases -pin three_branches -at
> get_asserted_phases -pin bht_block_dcd -at
Pin: NO PHASES for bht_block_dcd: asserting default C3+R
  > set_arrival -time 401 -phase C3+R -ports bht_block_dcd -...
  > set_arrival -time 101 -phase C3+R -ports bht_block_dcd -...
> get_asserted_phases -pin ru_9a_20 -at
> get_asserted_phases -pin iu_eu_data_blocked -at
> get_asserted_phases -pin gp_tr_a_clk -at
Pin: NO PHASES for gp_tr_a_clk: asserting default C3+R
  > set_arrival -time 401 -phase C3+R -ports gp_tr_a_clk -late

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> set_arrival -time 101 -phase C3+R -ports gptra_a_clk -early
> get_asserted_phases -pin gptra_b_clk -at
Pin: NO PHASES for gptra_b_clk: asserting default C3+R
> set_arrival -time 401 -phase C3+R -ports gptra_b_clk -late
> set_arrival -time 101 -phase C3+R -ports gptra_b_clk -early
> get_asserted_phases -pin op_is_44 -at
> get_asserted_phases -pin inst_fetches -at
> get_asserted_phases -pin clk2 -at
> get_asserted_phases -pin eu_iu_fxu_exc_cond -at
> get_asserted_phases -pin ru_9a_04 -at
> get_asserted_phases -pin br_wrong_targ -at
> get_asserted_phases -pin scan_enable -at
> get_asserted_phases -pin du_iu_store_status(0) -at
> get_asserted_phases -pin du_iu_store_status(1) -at
> get_asserted_phases -pin du_iu_store_status(2) -at
> get_asserted_phases -pin eu_iu_srlz_op_actn(0) -at
> get_asserted_phases -pin eu_iu_srlz_op_actn(1) -at
> get_asserted_phases -pin ru_9a_0001(0) -at
> get_asserted_phases -pin ru_9a_0001(1) -at
> get_asserted_phases -pin ireg_0_1(0) -at
> get_asserted_phases -pin ireg_0_1(1) -at
> get_asserted_phases -pin num_dcd_cyl(0) -at
> get_asserted_phases -pin num_dcd_cyl(1) -at
> get_asserted_phases -pin ru_9a_3233(32) -at
> get_asserted_phases -pin ru_9a_3233(33) -at
> get_asserted_phases -pin eu_iu_interrupt_info(0) -at
> get_asserted_phases -pin eu_iu_interrupt_info(1) -at
> get_asserted_phases -pin eu_iu_interrupt_info(2) -at
> get_asserted_phases -pin eu_iu_interrupt_info(3) -at
> get_asserted_phases -pin ru_9a_1617(16) -at
> get_asserted_phases -pin ru_9a_1617(17) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(0) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(1) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(2) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(3) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(4) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(5) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(6) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(7) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(8) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(9) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(10) -at
> get_asserted_phases -pin eu_iu_srlz_op_encode(11) -at
> get_asserted_phases -pin ru_9a_4849(48) -at
> get_asserted_phases -pin ru_9a_4849(49) -at
> get_asserted_phases -pin ireg_1631(22) -at
> get_asserted_phases -pin ireg_1631(23) -at
> get_asserted_phases -pin ireg_1631(24) -at
> get_asserted_phases -pin ireg_1631(25) -at
> get_asserted_phases -pin ireg_1631(26) -at
> get_asserted_phases -pin ireg_1631(27) -at
> get_asserted_phases -pin ireg_1631(28) -at
> get_asserted_phases -pin ireg_1631(29) -at
> get_asserted_phases -pin ireg_1631(30) -at
> idm::all_outputs

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- > get_asserted_phases -pin iu_eu_opcode_cmp -rat
- > get_asserted_phases -pin iu_rcvry_reset -rat
- > get_asserted_phases -pin iu_reset_op_c -rat
- > get_asserted_phases -pin dcd_succ_last_t1 -rat

Pin: NO PHASES for dcd_succ_last_t1:

- > set_required -time 999 -phase C3+R -ports dcd_succ_last_...
- > set_required -time -999 -phase C3+R -ports dcd_succ_last...
- > get_asserted_phases -pin iu_milli_mode -rat
- > get_asserted_phases -pin iu_reset_op_c_t1 -rat

Pin: NO PHASES for iu_reset_op_c_t1:

- > set_required -time 999 -phase C3+R -ports iu_reset_op_c_...
- > set_required -time -999 -phase C3+R -ports iu_reset_op_c....
- > get_asserted_phases -pin dcd_succ_last -rat
- > get_asserted_phases -pin iu_eu_op_nomatch -rat
- > get_asserted_phases -pin ds_1st_maybe -rat
- > get_asserted_phases -pin id_xcute_targ -rat
- > get_asserted_phases -pin xc_frc_ia_to_if_t1 -rat
- > get_asserted_phases -pin dcd_success_tr -rat
- > get_asserted_phases -pin dsucc_or_agi_n -rat
- > get_asserted_phases -pin dsucc_or_agi -rat
- > get_asserted_phases -pin iu_slow_mode -rat
- > get_asserted_phases -pin slwmd_blk_n -rat
- > get_asserted_phases -pin xc_frc_milli -rat
- > get_asserted_phases -pin dcd_succ_first_t1 -rat
- > get_asserted_phases -pin iu_reset_all -rat
- > get_asserted_phases -pin iu_milli_mode_t1 -rat
- > get_asserted_phases -pin iu_milli_mode_t2 -rat
- > get_asserted_phases -pin iu_milli_mode_t3 -rat
- > get_asserted_phases -pin xc_frc_milli_t1 -rat
- > get_asserted_phases -pin iu_exc_cond -rat
- > get_asserted_phases -pin slow_mode_tr -rat
- > get_asserted_phases -pin iu_eu_slow_mode -rat
- > get_asserted_phases -pin dcd_success -rat
- > get_asserted_phases -pin iu_milli_mode_tr -rat
- > get_asserted_phases -pin iu_reset_if -rat
- > get_asserted_phases -pin exc_cond_tr -rat
- > get_asserted_phases -pin dcd_succ_first -rat
- > get_asserted_phases -pin execute_recovery -rat
- > get_asserted_phases -pin execute_xcptn -rat
- > get_asserted_phases -pin xc_frc_ia_to_if -rat
- > get_asserted_phases -pin iu_slow_mode_t1 -rat

Pin: NO PHASES for iu_slow_mode_t1:

- > set_required -time 999 -phase C3+R -ports iu_slow_mode_t...
- > set_required -time -999 -phase C3+R -ports iu_slow_mode_...
- > get_asserted_phases -pin gp_tr_scan_out -rat

Pin: NO PHASES for gp_tr_scan_out:

- > set_required -time 999 -phase C3+R -ports gp_tr_scan_out ...
- > set_required -time -999 -phase C3+R -ports gp_tr_scan_out...
- > get_asserted_phases -pin iu_reset_fst -rat
- > get_asserted_phases -pin scan_out -rat

Pin: NO PHASES for scan_out:

- > set_required -time 999 -phase C3+R -ports scan_out -late
- > set_required -time -999 -phase C3+R -ports scan_out -early
- > get_asserted_phases -pin iu_eu_dcd_succ_tr -rat
- > get_asserted_phases -pin idcdsuc_err -rat

Pin: NO PHASES for idcdsuc_err:

```
> set_required -time 999 -phase C3+R -ports idcdsuc_err -late
> set_required -time -999 -phase C3+R -ports idcdsuc_err -...
> get_asserted_phases -pin frc_milli -rat
> get_asserted_phases -pin iu_intrupt_info(0) -rat
> get_asserted_phases -pin iu_intrupt_info(1) -rat
> get_asserted_phases -pin iu_intrupt_info(2) -rat
> get_asserted_phases -pin iu_intrupt_info(3) -rat
> get_asserted_phases -pin blk_dcd_info_tr(0) -rat
> get_asserted_phases -pin blk_dcd_info_tr(1) -rat
> get_asserted_phases -pin blk_dcd_info_tr(2) -rat
> get_asserted_phases -pin blk_dcd_info_tr(3) -rat
> get_asserted_phases -pin iu_srlz_op_encode(0) -rat
> get_asserted_phases -pin iu_srlz_op_encode(1) -rat
> get_asserted_phases -pin iu_srlz_op_encode(2) -rat
> get_asserted_phases -pin iu_srlz_op_encode(3) -rat
> get_asserted_phases -pin iu_srlz_op_encode(4) -rat
> get_asserted_phases -pin iu_srlz_op_encode(5) -rat
> get_asserted_phases -pin iu_srlz_op_encode(6) -rat
> get_asserted_phases -pin iu_srlz_op_encode(7) -rat
> get_asserted_phases -pin iu_srlz_op_encode(8) -rat
> get_asserted_phases -pin iu_srlz_op_encode(9) -rat
> get_asserted_phases -pin iu_srlz_op_encode(10) -rat
> get_asserted_phases -pin iu_srlz_op_encode(11) -rat
> get_asserted_phases -pin decode_ilc(0) -rat
> get_asserted_phases -pin decode_ilc(1) -rat
> get_asserted_phases -pin srlz_actn_tr(0) -rat
> get_asserted_phases -pin srlz_actn_tr(1) -rat
> get_asserted_phases -pin intrpt_info_tr(0) -rat
> get_asserted_phases -pin intrpt_info_tr(1) -rat
> get_asserted_phases -pin intrpt_info_tr(2) -rat
> get_asserted_phases -pin intrpt_info_tr(3) -rat
> get_asserted_phases -pin op_44_info_tr(0) -rat
> get_asserted_phases -pin op_44_info_tr(1) -rat
> get_asserted_phases -pin dcd_c_cnt(0) -rat
> get_asserted_phases -pin dcd_c_cnt(1) -rat
> read_dcadj_file -file /afs/apd/func/vlsi/alliance00/bssc...
```

[ET-0018]: >Begin...ETE DCADJ reader

for file /afs/apd/func/vlsi/alliance00/bssc8/v5/ndr/a00.dcadj.

[ET-0019]: <End.....ETE DCADJ reader.

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_set_rc.tcl

```
> write_end_point_report -points 2
```

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

*****POU92000-0107US1***** code invocation date

Sun Apr 18 21:58:17 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO	Cell	Delay/ Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	----	------	----------------------------------	-------

```

--
1 dcd_succ_last_t1          R C3+R  3242 -2243  3621 1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT            R C3+R  3242 -2243  3621 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            R C3+R  3242 -2243  3621 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y               R C3+R  3242 -2243  3621 1011 1 cs_invrn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a               F C3+R  1337 -2243   65  302 4 cs_invrn  01c NOT
1906 N675
---->{a} C2738/y           F C3+R  1337 -2243   65  302 4 cs_nnd2n  14c NAND
0 N675
----> C2738/b              R C3+R  1289 -2243   93 1261 4 cs_nnd2n  14c NAND
48 dcd_success&0
----> C2734rwr/y           R C3+R  1289 -2243   93 1261 4 cs_invrn  19c NOT
0 dcd_success&0
----> C2734rwr/a           F C3+R  1236 -2243   40  310 1 cs_invrn  19c NOT
53 N1097
----> C2728rwr/y           F C3+R  1236 -2243   40  310 1 cs_invrn  16c NOT
0 N1097
----> C2728rwr/a           R C3+R  1205 -2243   84  181 2 cs_invrn  16c NOT
31 N1692
---->{b} C2725rwr/y        R C3+R  1205 -2243   84  181 2 cs_nnd2n  13c NAND
0 N1692

```

----> C2725rwr/a 57 N1479	F C3+R	1148	-2243	98	161	2	cs_nnd2n	13c	NAND	
---->{c} C2721rwr/y 0 N1479	F C3+R	1148	-2243	98	161	2	cs_nnd3n	12c	NAND	
----> C2721rwr/a 63 N1497	R C3+R	1085	-2243	184	115	2	cs_nnd3n	12c	NAND	
---->{d} C2709rwr/y 0 N1497	R C3+R	1085	-2243	184	115	2	cs_nor3n	10c	NOR	
----> C2709rwr/c 112 N1976	F C3+R	973	-2243	97	52	1	cs_nor3n	10c	NOR	
---->{e} C2579rwr_0_0/y 0 N1976	F C3+R	973	-2243	97	52	1	cs_nnd3n	07c	NAND	
----> C2579rwr_0_0/b 64 N127	R C3+R	909	-2243	223	61	2	cs_nnd3n	07c	NAND	
----> C2538/y N127	R C3+R	909	-2243	223	61	2	cs_inwn	01c	NOT	0
----> C2538/a blk_dcd_in(0)	F C3+R	785	-2243	85	16	1	cs_inwn	01c	NOT	124
---->{f} C2480rwr/y 0 blk_dcd_in(0)	F C3+R	785	-2243	85	16	1	cs_nnd3n	02c	NAND	
----> C2480rwr/a 55 N393	R C3+R	730	-2243	121	17	1	cs_nnd3n	02c	NAND	
---->{g} C2324/y 0 N393	R C3+R	730	-2243	121	17	1	cs_nnd2n	02c	NAND	
----> C2324/b 89 N1728	F C3+R	641	-2243	203	215	8	cs_nnd2n	02c	NAND	
----> C2224/y N1728	F C3+R	641	-2243	203	215	8	cs_inwn	06c	NOT	0
----> C2224/a 144 N1371	R C3+R	497	-2243	300	87	3	cs_inwn	06c	NOT	
---->{h} C2061/y 0 N1371	R C3+R	497	-2243	300	87	3	cs_nnd2n	02c	NAND	
----> C2061/a 169 dcd_cyl_cnt_q(0)	F C3+R	328	-2243	96	124	4	cs_nnd2n	02c	NAND	
----> dcd_cyl_cnt.reg_n.lat_0/2_out_n SRL 0 dcd_cyl_cnt_q(0)	F C3+R	328	-2243	96	124	4	cl_nnd2n	07c		
----> dcd_cyl_cnt.reg_n.lat_0/c2 168 slow_mode.c2_1	R C3+	160	N/C	60	222	13	cl_nnd2n	07c	SRL	
----> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB		

2 dcd_succ_last_t1 dcd_succ_last_t1 RAT	F C3+R	2696	-1697	2124	1011	1	PO		0	
----> BOX714/OUT 0 dcd_succ_last_t1	999					0				
----> BOX714/IN 0 dcd_succ_last_t1&0	F C3+R	2696	-1697	2124	1011	1	IOPAD		IOPAD	
----> C167/y 0 dcd_succ_last_t1&0	F C3+R	2696	-1697	2124	1011	1	IOPAD		IOPAD	
----> C167/a 1457 N675	F C3+R	2696	-1697	2124	1011	1	cs_inwn	01c	NOT	
---->{a} C2738/y 0 N675	R C3+R	1240	-1697	97	302	4	cs_inwn	01c	NOT	
	R C3+R	1240	-1697	97	302	4	cs_nnd2n	14c	NAND	

----> C2738/b	F C3+R	1179	-1697	56	1261	4	cs_nnd2n	14c	NAND	
61 dcd_success&0										
----> C2734rwr/y	F C3+R	1179	-1697	56	1261	4	cs_invvn	19c	NOT	
0 dcd_success&0										
----> C2734rwr/a	R C3+R	1138	-1697	58	310	1	cs_invvn	19c	NOT	
41 N1097										
----> C2728rwr/y	R C3+R	1138	-1697	58	310	1	cs_invvn	16c	NOT	
0 N1097										
----> C2728rwr/a	F C3+R	1099	-1697	61	181	2	cs_invvn	16c	NOT	
39 N1692										
---->{b} C2725rwr/y	F C3+R	1099	-1697	61	181	2	cs_nnd2n	13c	NAND	
0 N1692										
----> C2725rwr/a	R C3+R	1056	-1697	98	161	2	cs_nnd2n	13c	NAND	
43 N1479										
---->{c} C2721rwr/y	R C3+R	1056	-1697	98	161	2	cs_nnd3n	12c	NAND	
0 N1479										
----> C2721rwr/a	F C3+R	992	-1697	86	115	2	cs_nnd3n	12c	NAND	
64 N1497										
---->{d} C2709rwr/y	F C3+R	992	-1697	86	115	2	cs_nor3n	10c	NOR	
0 N1497										
----> C2709rwr/c	R C3+R	927	-1697	117	52	1	cs_nor3n	10c	NOR	
65 N1976										
---->{e} C2579rwr_0_0/y	R C3+R	927	-1697	117	52	1	cs_nnd3n	07c	NAND	
0 N1976										
----> C2579rwr_0_0/b	F C3+R	842	-1697	131	61	2	cs_nnd3n	07c	NAND	
85 N127										
----> C2538/y	F C3+R	842	-1697	131	61	2	cs_invvn	01c	NOT	0
N127										
----> C2538/a	R C3+R	752	-1697	96	16	1	cs_invvn	01c	NOT	90
blk_dcd_in(0)										
---->{f} C2480rwr/y	R C3+R	752	-1697	96	16	1	cs_nnd3n	02c	NAND	
0 blk_dcd_in(0)										
----> C2480rwr/a	F C3+R	688	-1697	90	17	1	cs_nnd3n	02c	NAND	
64 N393										
---->{g} C2324/y	F C3+R	688	-1697	90	17	1	cs_nnd2n	02c	NAND	
0 N393										
----> C2324/b	R C3+R	632	-1697	286	215	8	cs_nnd2n	02c	NAND	
56 N1728										
----> C2224/y	R C3+R	632	-1697	286	215	8	cs_invvn	06c	NOT	0
N1728										
----> C2224/a	F C3+R	452	-1697	212	87	3	cs_invvn	06c	NOT	
180 N1371										
---->{h} C2061/y	F C3+R	452	-1697	212	87	3	cs_nnd2n	02c	NAND	
0 N1371										
----> C2061/a	R C3+R	315	-1697	111	124	4	cs_nnd2n	02c	NAND	
137 dcd_cyl_cnt_q(0)										
----> dcd_cyl_cnt.reg_n.lat_0/l2_out_n	R C3+R	315	-1697	111	124	4	cl_nnd2n	07c		
SRL 0 dcd_cyl_cnt_q(0)										
----> dcd_cyl_cnt.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_nnd2n	07c	SRL	
155 slow_mode.c2_1										
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB		
0 slow_mode.c2_1										

--

> timing_reset

[timing_reset]: Timing has been reset.
 > write_end_point_report -points 2
 [ET-0018]: >Begin...New EndPoint Report
 for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 21:58:18 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 2

Cause of Slack Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time   RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup      ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold       ClkGHld      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width  ClkTPW      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                   Setup        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                     Hold          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle              EndOfC       ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth         ClkPW        ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
ClockSeparation         ClkSep       ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
Loop                     ALTest      ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
Arrival Time Limiting   ATLimit     Slack discontinuity due to failed test

```

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO	Cell	Delay/ Failed Test/ P Func	T.Adj
1 dcd_succ_last_t1	R C3+R	3242	-2243	3621	1011	1	PO		0
dcd_succ_last_t1									
RAT		999					0		
----> BOX714/OUT	R C3+R	3242	-2243	3621	1011	1	IOPAD		IOPAD
0 dcd_succ_last_t1									
----> BOX714/IN	R C3+R	3242	-2243	3621	1011	1	IOPAD		IOPAD
0 dcd_succ_last_t1&0									
----> C167/y	R C3+R	3242	-2243	3621	1011	1	cs_invvn	01c	NOT
0 dcd_succ_last_t1&0									
----> C167/a	F C3+R	1337	-2243	65	302	4	cs_invvn	01c	NOT
1906 N675									
---->{a} C2738/y	F C3+R	1337	-2243	65	302	4	cs_nnd2n	14c	NAND

0 N675																			
----> C2738/b	R C3+R	1289	-2243	93	1261	4	cs_nnd2n	14c	NAND										
48 dcd_success&0																			
----> C2734rwr/y	R C3+R	1289	-2243	93	1261	4	cs_invvn	19c	NOT										
0 dcd_success&0																			
----> C2734rwr/a	F C3+R	1236	-2243	40	310	1	cs_invvn	19c	NOT										
53 N1097																			
----> C2728rwr/y	F C3+R	1236	-2243	40	310	1	cs_invvn	16c	NOT										
0 N1097																			
----> C2728rwr/a	R C3+R	1205	-2243	84	181	2	cs_invvn	16c	NOT										
31 N1692																			
---->{b} C2725rwr/y	R C3+R	1205	-2243	84	181	2	cs_nnd2n	13c	NAND										
0 N1692																			
----> C2725rwr/a	F C3+R	1148	-2243	98	161	2	cs_nnd2n	13c	NAND										
57 N1479																			
---->{c} C2721rwr/y	F C3+R	1148	-2243	98	161	2	cs_nnd3n	12c	NAND										
0 N1479																			
----> C2721rwr/a	R C3+R	1085	-2243	184	115	2	cs_nnd3n	12c	NAND										
63 N1497																			
---->{d} C2709rwr/y	R C3+R	1085	-2243	184	115	2	cs_nor3n	10c	NOR										
0 N1497																			
----> C2709rwr/c	F C3+R	973	-2243	97	52	1	cs_nor3n	10c	NOR										
112 N1976																			
---->{e} C2579rwr_0_0/y	F C3+R	973	-2243	97	52	1	cs_nnd3n	07c	NAND										
0 N1976																			
----> C2579rwr_0_0/b	R C3+R	909	-2243	223	61	2	cs_nnd3n	07c	NAND										
64 N127																			
----> C2538/y	R C3+R	909	-2243	223	61	2	cs_invvn	01c	NOT	0									
N127																			
----> C2538/a	F C3+R	785	-2243	85	16	1	cs_invvn	01c	NOT	124									
blk_dcd_in(0)																			
---->{f} C2480rwr/y	F C3+R	785	-2243	85	16	1	cs_nnd3n	02c	NAND										
0 blk_dcd_in(0)																			
----> C2480rwr/a	R C3+R	730	-2243	121	17	1	cs_nnd3n	02c	NAND										
55 N393																			
---->{g} C2324/y	R C3+R	730	-2243	121	17	1	cs_nnd2n	02c	NAND										
0 N393																			
----> C2324/b	F C3+R	641	-2243	203	215	8	cs_nnd2n	02c	NAND										
89 N1728																			
----> C2224/y	F C3+R	641	-2243	203	215	8	cs_invvn	06c	NOT	0									
N1728																			
----> C2224/a	R C3+R	497	-2243	300	87	3	cs_invvn	06c	NOT										
144 N1371																			
---->{h} C2061/y	R C3+R	497	-2243	300	87	3	cs_nnd2n	02c	NAND										
0 N1371																			
----> C2061/a	F C3+R	328	-2243	96	124	4	cs_nnd2n	02c	NAND										
169 dcd_cyl_cnt_q(0)																			
----> dcd_cyl_cnt.reg_n.lat_0/l2_out_n	F C3+R	328	-2243	96	124	4	cl_nnd2n	07c											
SRL 0 dcd_cyl_cnt_q(0)																			
----> dcd_cyl_cnt.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_nnd2n	07c	SRL										
168 slow_mode.c2_1																			
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB											
0 slow_mode.c2_1																			

--


```

---->{h} C2061/y          F C3+R   452 -1697  212  87 3 cs_nnd2n  02c NAND
0 N1371
----> C2061/a             R C3+R   315 -1697  111  124 4 cs_nnd2n  02c NAND
137 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/2_out_n      R C3+R   315 -1697  111  124 4 cl_nnd2n  07c
SRL    0 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/c2           R C3+    160   N/C   60  222 13 cl_nnd2n  07c SRL
155 slow_mode.c2_1
----> slow_mode.clockblock/c2             R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
> accTime_enable
[BD-13116]: Initializing accounting
> write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report
           for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 21:58:18 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 2

Cause of Slack Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont  Slack due to a point downstream on path
Required Arrival Time   RAT      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup      ClkGSet  ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold       ClkGHld  ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width  ClkTPW   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                   Setup    ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                     Hold     ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle              EndOfC  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth         ClkPW    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
ClockSeparation         ClkSep   ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
Loop                    ALTest   ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
Arrival Time Limiting   ATLimit  Slack discontinuity due to failed test

```

```

Num/                    LimitedAT/                    Delay/ Failed Test/
Test PinName            E Phase   AT Slack Slew CL FO Cell   P Func T.Adj
NetName

```

```

--
1 dcd_succ_last_t1          R C3+R  3242 -2243  3621 1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT            R C3+R  3242 -2243  3621 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            R C3+R  3242 -2243  3621 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1&0
----> C167/y              R C3+R  3242 -2243  3621 1011 1 cs_invpn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a              F C3+R  1337 -2243   65  302 4 cs_invpn  01c NOT
1906 N675
---->{a} C2738/y          F C3+R  1337 -2243   65  302 4 cs_nnd2n  14c NAND
0 N675
----> C2738/b            R C3+R  1289 -2243   93 1261 4 cs_nnd2n  14c NAND
48 dcd_success&0
----> C2734rwr/y          R C3+R  1289 -2243   93 1261 4 cs_invpn  19c NOT
0 dcd_success&0
----> C2734rwr/a          F C3+R  1236 -2243   40  310 1 cs_invpn  19c NOT
53 N1097
----> C2728rwr/y          F C3+R  1236 -2243   40  310 1 cs_invpn  16c NOT
0 N1097
----> C2728rwr/a          R C3+R  1205 -2243   84  181 2 cs_invpn  16c NOT
31 N1692
---->{b} C2725rwr/y        R C3+R  1205 -2243   84  181 2 cs_nnd2n  13c NAND
0 N1692
----> C2725rwr/a          F C3+R  1148 -2243   98  161 2 cs_nnd2n  13c NAND
57 N1479
---->{c} C2721rwr/y        F C3+R  1148 -2243   98  161 2 cs_nnd3n  12c NAND
0 N1479
----> C2721rwr/a          R C3+R  1085 -2243  184  115 2 cs_nnd3n  12c NAND
63 N1497
---->{d} C2709rwr/y        R C3+R  1085 -2243  184  115 2 cs_nor3n  10c NOR
0 N1497
----> C2709rwr/c          F C3+R   973 -2243   97  52 1 cs_nor3n  10c NOR
112 N1976
---->{e} C2579rwr_0_0/y    F C3+R   973 -2243   97  52 1 cs_nnd3n  07c NAND
0 N1976
----> C2579rwr_0_0/b      R C3+R   909 -2243  223  61 2 cs_nnd3n  07c NAND
64 N127
----> C2538/y            R C3+R   909 -2243  223  61 2 cs_invpn  01c NOT    0
N127
----> C2538/a            F C3+R   785 -2243   85  16 1 cs_invpn  01c NOT    124
blk_dcd_in(0)
---->{f} C2480rwr/y        F C3+R   785 -2243   85  16 1 cs_nnd3n  02c NAND
0 blk_dcd_in(0)
----> C2480rwr/a          R C3+R   730 -2243  121  17 1 cs_nnd3n  02c NAND
55 N393
---->{g} C2324/y          R C3+R   730 -2243  121  17 1 cs_nnd2n  02c NAND
0 N393
----> C2324/b            F C3+R   641 -2243  203  215 8 cs_nnd2n  02c NAND
89 N1728
----> C2224/y            F C3+R   641 -2243  203  215 8 cs_invpn  06c NOT    0
N1728
----> C2224/a            R C3+R   497 -2243  300  87 3 cs_invpn  06c NOT

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144 N1371
---->{h} C2061/y          R C3+R   497 -2243   300   87 3 cs_nnd2n  02c NAND
0 N1371
----> C2061/a            F C3+R   328 -2243   96  124 4 cs_nnd2n  02c NAND
169 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/l2_out_n      F C3+R   328 -2243   96  124 4 cl_nnd2n  07c
SRL    0 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/c2            R C3+    160   N/C   60  222 13 cl_nnd2n  07c SRL
168 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
    2 dcd_succ_last_t1      F C3+R   2696 -1697  2124 1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT            F C3+R   2696 -1697  2124 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            F C3+R   2696 -1697  2124 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y              F C3+R   2696 -1697  2124 1011 1 cs_invn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a              R C3+R   1240 -1697   97  302 4 cs_invn  01c NOT
1457 N675
---->{a} C2738/y          R C3+R   1240 -1697   97  302 4 cs_nnd2n  14c NAND
0 N675
----> C2738/b            F C3+R   1179 -1697   56 1261 4 cs_nnd2n  14c NAND
61 dcd_success&0
----> C2734rwr/y          F C3+R   1179 -1697   56 1261 4 cs_invn  19c NOT
0 dcd_success&0
----> C2734rwr/a          R C3+R   1138 -1697   58  310 1 cs_invn  19c NOT
41 N1097
----> C2728rwr/y          R C3+R   1138 -1697   58  310 1 cs_invn  16c NOT
0 N1097
----> C2728rwr/a          F C3+R   1099 -1697   61  181 2 cs_invn  16c NOT
39 N1692
---->{b} C2725rwr/y      F C3+R   1099 -1697   61  181 2 cs_nnd2n  13c NAND
0 N1692
----> C2725rwr/a          R C3+R   1056 -1697   98  161 2 cs_nnd2n  13c NAND
43 N1479
---->{c} C2721rwr/y      R C3+R   1056 -1697   98  161 2 cs_nnd3n  12c NAND
0 N1479
----> C2721rwr/a          F C3+R   992 -1697   86  115 2 cs_nnd3n  12c NAND
64 N1497
---->{d} C2709rwr/y      F C3+R   992 -1697   86  115 2 cs_nor3n  10c NOR
0 N1497
----> C2709rwr/c          R C3+R   927 -1697  117   52 1 cs_nor3n  10c NOR
65 N1976
---->{e} C2579rwr_0_0/y  R C3+R   927 -1697  117   52 1 cs_nnd3n  07c NAND
0 N1976
----> C2579rwr_0_0/b      F C3+R   842 -1697  131   61 2 cs_nnd3n  07c NAND
85 N127
----> C2538/y            F C3+R   842 -1697  131   61 2 cs_invn  01c NOT    0
N127
----> C2538/a            R C3+R   752 -1697   96   16 1 cs_invn  01c NOT    90

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blk_dcd_in(0)
---->{f} C2480rwr/y          R C3+R    752 -1697   96   16 1 cs_nnd3n  02c NAND
0 blk_dcd_in(0)
----> C2480rwr/a            F C3+R    688 -1697   90   17 1 cs_nnd3n  02c NAND
64 N393
---->{g} C2324/y           F C3+R    688 -1697   90   17 1 cs_nnd2n  02c NAND
0 N393
----> C2324/b              R C3+R    632 -1697  286  215 8 cs_nnd2n  02c NAND
56 N1728
----> C2224/y              R C3+R    632 -1697  286  215 8 cs_invn  06c NOT    0
N1728
----> C2224/a              F C3+R    452 -1697  212   87 3 cs_invn  06c NOT
180 N1371
---->{h} C2061/y           F C3+R    452 -1697  212   87 3 cs_nnd2n  02c NAND
0 N1371
----> C2061/a              R C3+R    315 -1697  111  124 4 cs_nnd2n  02c NAND
137 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/l2_out_n    R C3+R    315 -1697  111  124 4 cl_nnd2n  07c
SRL    0 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/c2          R C3+    160   N/C   60  222 13 cl_nnd2n  07c SRL
155 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

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> checkfan

Electrical Violations in Network 'IDCDSUC'

Pin/Port	-> Net	Capacitance Limit / AdjLim / Actual	Slew Limit / AdjLim / Actual	Fanout
eu_iu_enter_slow_md / 290.00 / 352.00 * 1	-> eu_iu_enter_slow_md	141.00 / 141.00 / 16.89	290.00 /	
eu_iu_mmode 290.00 / 326.00 * 1	-> eu_iu_mmode	141.00 / 141.00 / 32.56	290.00 /	
du_iu_hold_aa_req 290.00 / 424.00 * 1	-> du_iu_hold_aa_req	141.00 / 141.00 / 73.63	290.00 /	
eu_iu_fpu_end_op 290.00 / 339.00 * 1	-> eu_iu_fpu_end_op	141.00 / 141.00 / 15.67	290.00 /	
eu_iu_misc_hold 290.00 / 332.00 * 1	-> eu_iu_misc_hold	141.00 / 141.00 / 18.88	290.00 /	
clkg 60.00 1	-> clkg	141.00 / 141.00 / 145.52	* 100.00 / 100.00 /	
du_iu_quiesced 290.00 / 338.00 * 1	-> du_iu_quiesced	141.00 / 141.00 / 16.89	290.00 /	
iq_empty / 116.00 1	-> iq_empty	141.00 / 141.00 / 174.31	* 290.00 / 290.00	
gptr_scan_in 0.00 1	-> gptr_scan_in	141.00 / 141.00 / 1011.00	* 0.00 / 0.00 /	
gptr_a_clk 0.00 1	-> gptr_a_clk	141.00 / 141.00 / 1011.00	* 0.00 / 0.00 /	
gptr_b_clk 0.00 1	-> gptr_b_clk	141.00 / 141.00 / 1011.00	* 0.00 / 0.00 /	
clkg2 60.00 1	-> clkg2	141.00 / 141.00 / 145.52	* 100.00 / 100.00 /	

eu_iu_fxu_exc_cond	-> eu_iu_fxu_exc_cond	141.00 / 141.00 / 15.67	290.00
/ 290.00 / 390.00 * 1			
du_iu_store_status(2)	-> du_iu_store_status(2)	141.00 / 141.00 / 16.89	290.00 /
290.00 / 500.00 * 1			
eu_iu_srlz_op_actn(0)	-> eu_iu_srlz_op_actn(0)	141.00 / 141.00 / 47.57	290.00 /
290.00 / 374.00 * 1			
eu_iu_srlz_op_actn(1)	-> eu_iu_srlz_op_actn(1)	141.00 / 141.00 / 47.57	290.00 /
290.00 / 341.00 * 1			
eu_iu_srlz_op_encode(0)	-> eu_iu_srlz_op_encode(0)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 401.00 * 1			
eu_iu_srlz_op_encode(1)	-> eu_iu_srlz_op_encode(1)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 400.00 * 1			
eu_iu_srlz_op_encode(2)	-> eu_iu_srlz_op_encode(2)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 420.00 * 1			
eu_iu_srlz_op_encode(3)	-> eu_iu_srlz_op_encode(3)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 302.00 * 1			
eu_iu_srlz_op_encode(4)	-> eu_iu_srlz_op_encode(4)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 406.00 * 1			
eu_iu_srlz_op_encode(5)	-> eu_iu_srlz_op_encode(5)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 373.00 * 1			
eu_iu_srlz_op_encode(6)	-> eu_iu_srlz_op_encode(6)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 354.00 * 1			
eu_iu_srlz_op_encode(7)	-> eu_iu_srlz_op_encode(7)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 398.00 * 1			
eu_iu_srlz_op_encode(8)	-> eu_iu_srlz_op_encode(8)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 367.00 * 1			
eu_iu_srlz_op_encode(9)	-> eu_iu_srlz_op_encode(9)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 323.00 * 1			
eu_iu_srlz_op_encode(11)	-> eu_iu_srlz_op_encode(11)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 500.00 * 1			
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1		78.50 / 78.50 / 220.92 *	
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1		78.50 / 78.50 / 222.27 *	
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1		78.50 / 78.50 / 212.39 *	
200.00 / 200.00 / 184.59 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2		78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2		78.50 / 78.50 / 239.36 *	
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_1:cb_clk_3_ -> slow_mode.clka_2		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3		78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_2:cb_clk_3_ -> slow_mode.clka_3		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4		78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4		78.50 / 78.50 / 239.36 *	
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_3:cb_clk_3_ -> slow_mode.clka_4		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5		78.50 / 78.50 / 237.91 *	

200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL

Pin/Port	-> Net	Capacitance Limit / AdjLim / Actual	Slew Limit / AdjLim / Actual	Fanout
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5			78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3_ -> slow_mode.clka_5			78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1			78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2			78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_5:cb_clk_3_ -> slow_mode.clka			78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
y@C167:cs_invvn01c	-> dcd_succ_last_t1&0		68.00 / 68.00 / 1011.00 *	301.00
/ 301.00 / 3676.28 *	1 KEEP_BTR			
y@C2013:cs_invvn01c	-> N18&0		68.00 / 68.00 / 1011.00 *	301.00 /
301.00 / 3608.92 *	1			
y@C2061:cs_nnd2n02c	-> N1371		70.00 / 70.00 / 86.53 *	290.00 /
290.00 / 309.86 *	3			
y@C2082:cs_invvn01c	-> N146&0		68.00 / 68.00 / 1011.00 *	301.00 /
301.00 / 3604.78 *	1			
y@C2224:cs_invvn06c	-> N1728		208.00 / 208.00 / 214.85 *	290.00 /
290.00 / 285.51	8			
y@C2393:cs_nnd2n02c	-> iu_reset_op_c_t1&0		70.00 / 70.00 / 1044.40 *	
290.00 / 290.00 / 3683.69 *	3			
y@C2496:cs_nnd4n03c	-> N1435		85.00 / 85.00 / 97.83 *	290.00 /
290.00 / 353.82 *	5			
y@C2646:cs_invvn04c	-> N1645		133.00 / 133.00 / 150.69 *	290.00 /
290.00 / 273.28	6			
y@C2724:cs_nnd2n02c	-> N23		70.00 / 70.00 / 92.41 *	290.00 /
290.00 / 326.23 *	3			
y@C2750:cs_invvn05c	-> N1333		167.00 / 167.00 / 180.24 *	290.00 /
290.00 / 266.70	8			
y@C2794:cs_ao12n03c	-> N73		86.00 / 86.00 / 92.41 *	290.00 /
290.00 / 466.30 *	3			
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q			247.00 / 247.00 / 256.34 *	
290.00 / 290.00 / 205.99	8			

[BD-500900]: (W) There were 57 electrical violations.

> checkfan

Electrical Violations in Network 'IDCDSUC'

Pin/Port	-> Net	Capacitance Limit / AdjLim / Actual	Slew Limit / AdjLim / Actual	Fanout
eu_iu_enter_slow_md	-> eu_iu_enter_slow_md		141.00 / 141.00 / 16.89	290.00
/ 290.00 / 352.00 *	1			
eu_iu_mmode	-> eu_iu_mmode		141.00 / 141.00 / 32.56	290.00 /
290.00 / 326.00 *	1			
du_iu_hold_aa_req	-> du_iu_hold_aa_req		141.00 / 141.00 / 73.63	290.00 /
290.00 / 424.00 *	1			
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op		141.00 / 141.00 / 15.67	290.00 /
290.00 / 339.00 *	1			
eu_iu_misc_hold	-> eu_iu_misc_hold		141.00 / 141.00 / 18.88	290.00 /

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290.00 / 332.00 * 1
clkg                -> clkg                141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 1
du_iu_quiesced      -> du_iu_quiesced      141.00 / 141.00 / 16.89 290.00 /
290.00 / 338.00 * 1
iq_empty            -> iq_empty            141.00 / 141.00 / 174.31 * 290.00 / 290.00
/ 116.00 1
gp_tr_scan_in       -> gp_tr_scan_in       141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1
gp_tr_a_clk         -> gp_tr_a_clk         141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1
gp_tr_b_clk         -> gp_tr_b_clk         141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1
clk_g2              -> clk_g2              141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 1
eu_iu_fxu_exc_cond  -> eu_iu_fxu_exc_cond  141.00 / 141.00 / 15.67 290.00
/ 290.00 / 390.00 * 1
du_iu_store_status(2) -> du_iu_store_status(2)  141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 * 1
eu_iu_srlz_op_actn(0) -> eu_iu_srlz_op_actn(0)  141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 * 1
eu_iu_srlz_op_actn(1) -> eu_iu_srlz_op_actn(1)  141.00 / 141.00 / 47.57 290.00 /
290.00 / 341.00 * 1
eu_iu_srlz_op_encode(0) -> eu_iu_srlz_op_encode(0)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.00 * 1
eu_iu_srlz_op_encode(1) -> eu_iu_srlz_op_encode(1)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.00 * 1
eu_iu_srlz_op_encode(2) -> eu_iu_srlz_op_encode(2)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.00 * 1
eu_iu_srlz_op_encode(3) -> eu_iu_srlz_op_encode(3)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 * 1
eu_iu_srlz_op_encode(4) -> eu_iu_srlz_op_encode(4)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 406.00 * 1
eu_iu_srlz_op_encode(5) -> eu_iu_srlz_op_encode(5)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 * 1
eu_iu_srlz_op_encode(6) -> eu_iu_srlz_op_encode(6)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 * 1
eu_iu_srlz_op_encode(7) -> eu_iu_srlz_op_encode(7)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 * 1
eu_iu_srlz_op_encode(8) -> eu_iu_srlz_op_encode(8)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 * 1
eu_iu_srlz_op_encode(9) -> eu_iu_srlz_op_encode(9)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 1
eu_iu_srlz_op_encode(11) -> eu_iu_srlz_op_encode(11)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 * 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1 78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1 78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1 78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2 78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2 78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL

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clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2          78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_2:cb_clk_32 -> slow_mode.c1_3             78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_2:cb_clk_32 -> slow_mode.c2_3             78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3          78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32 -> slow_mode.c1_4             78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_3:cb_clk_32 -> slow_mode.c2_4             78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4          78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_4:cb_clk_32 -> slow_mode.c1_5             78.50 / 78.50 / 237.91 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL

```

Pin/Port	-> Net	Capacitance Limit / AdjLim / Actual	Slew Limit / AdjLim / Actual	Fanout
c2@slow_mode.clockblock_4:cb_clk_32	-> slow_mode.c2_5		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3	-> slow_mode.clka_5		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32	-> slow_mode.c1		78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32	-> slow_mode.c2		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_5:cb_clk_3	-> slow_mode.clka		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
y@C167:cs_invvn01c	-> dcd_succ_last_t1&0		68.00 / 68.00 / 1011.00 *	301.00
/ 301.00 / 3676.28	* 1 KEEP_BTR			
y@C2013:cs_invvn01c	-> N18&0		68.00 / 68.00 / 1011.00 *	301.00 /
301.00 / 3608.92	* 1			
y@C2061:cs_nnd2n02c	-> N1371		70.00 / 70.00 / 86.53 *	290.00 /
290.00 / 309.86	* 3			
y@C2082:cs_invvn01c	-> N146&0		68.00 / 68.00 / 1011.00 *	301.00 /
301.00 / 3604.78	* 1			
y@C2224:cs_invvn06c	-> N1728		208.00 / 208.00 / 214.85 *	290.00 /
290.00 / 285.51	8			
y@C2393:cs_nnd2n02c	-> iu_reset_op_c_t1&0		70.00 / 70.00 / 1044.40 *	
290.00 / 290.00 / 3683.69	* 3			
y@C2496:cs_nnd4n03c	-> N1435		85.00 / 85.00 / 97.83 *	290.00 /
290.00 / 353.82	* 5			
y@C2646:cs_invvn04c	-> N1645		133.00 / 133.00 / 150.69 *	290.00 /
290.00 / 273.28	6			
y@C2724:cs_nnd2n02c	-> N23		70.00 / 70.00 / 92.41 *	290.00 /
290.00 / 326.23	* 3			
y@C2750:cs_invvn05c	-> N1333		167.00 / 167.00 / 180.24 *	290.00 /
290.00 / 266.70	8			
y@C2794:cs_ao12n03c	-> N73		86.00 / 86.00 / 92.41 *	290.00 /
290.00 / 466.30	* 3			
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl	-> frc_blk_1cyc_q		247.00 / 247.00 / 256.34 *	
290.00 / 290.00 / 205.99	8			

[BD-500900]: (W) There were 57 electrical violations.

```

> optimize_delay -medium
[BD-80000]: check_tech CMVC version 1.6 compiled on Apr 8 1999 at 05:20:06
bdz> late_time 0 1
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/late_time.tcl
> get_default_delay_synlimit
> get_default_synlimit
> echo {In David's Exp. Timing Opt Scenario}
In David's Exp. Timing Opt Scenario
> checkfan

```

Electrical Violations in Network 'IDCDSUC'

Pin/Port	-> Net	Capacitance		Slew		Fanout	
		Limit / AdjLim	Actual	Limit / AdjLim	Actual	Limit / AdjLim	Actual
eu_iu_enter_slow_md / 290.00 / 352.00 * 1	-> eu_iu_enter_slow_md			141.00 / 141.00	16.89	290.00 /	
eu_iu_mmode 290.00 / 326.00 * 1	-> eu_iu_mmode			141.00 / 141.00	32.56	290.00 /	
du_iu_hold_aa_req 290.00 / 424.00 * 1	-> du_iu_hold_aa_req			141.00 / 141.00	73.63	290.00 /	
eu_iu_fpu_end_op 290.00 / 339.00 * 1	-> eu_iu_fpu_end_op			141.00 / 141.00	15.67	290.00 /	
eu_iu_misc_hold 290.00 / 332.00 * 1	-> eu_iu_misc_hold			141.00 / 141.00	18.88	290.00 /	
clkg 60.00 1	-> clkg			141.00 / 141.00	145.52 * 100.00 / 100.00		
du_iu_quiesced 290.00 / 338.00 * 1	-> du_iu_quiesced			141.00 / 141.00	16.89	290.00 /	
iq_empty / 116.00 1	-> iq_empty			141.00 / 141.00	174.31 * 290.00 / 290.00		
gptr_scan_in 0.00 1	-> gptr_scan_in			141.00 / 141.00	1011.00 * 0.00 / 0.00		
gptr_a_clk 0.00 1	-> gptr_a_clk			141.00 / 141.00	1011.00 * 0.00 / 0.00		
gptr_b_clk 0.00 1	-> gptr_b_clk			141.00 / 141.00	1011.00 * 0.00 / 0.00		
clkg2 60.00 1	-> clkg2			141.00 / 141.00	145.52 * 100.00 / 100.00		
eu_iu_fxu_exc_cond / 290.00 / 390.00 * 1	-> eu_iu_fxu_exc_cond			141.00 / 141.00	15.67	290.00	
du_iu_store_status(2) 290.00 / 500.00 * 1	-> du_iu_store_status(2)			141.00 / 141.00	16.89	290.00 /	
eu_iu_srlz_op_actn(0) 290.00 / 374.00 * 1	-> eu_iu_srlz_op_actn(0)			141.00 / 141.00	47.57	290.00 /	
eu_iu_srlz_op_actn(1) 290.00 / 341.00 * 1	-> eu_iu_srlz_op_actn(1)			141.00 / 141.00	47.57	290.00 /	
eu_iu_srlz_op_encode(0) 290.00 / 290.00 / 401.00 * 1	-> eu_iu_srlz_op_encode(0)			141.00 / 141.00	16.89		
eu_iu_srlz_op_encode(1) 290.00 / 290.00 / 400.00 * 1	-> eu_iu_srlz_op_encode(1)			141.00 / 141.00	16.89		
eu_iu_srlz_op_encode(2) 290.00 / 290.00 / 420.00 * 1	-> eu_iu_srlz_op_encode(2)			141.00 / 141.00	16.89		
eu_iu_srlz_op_encode(3) 290.00 / 290.00 / 302.00 * 1	-> eu_iu_srlz_op_encode(3)			141.00 / 141.00	16.89		
eu_iu_srlz_op_encode(4)	-> eu_iu_srlz_op_encode(4)			141.00 / 141.00	16.89		

```

290.00 / 290.00 / 406.00 * 1
eu_iu_srlz_op_encode(5)      -> eu_iu_srlz_op_encode(5)      141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 * 1
eu_iu_srlz_op_encode(6)      -> eu_iu_srlz_op_encode(6)      141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 * 1
eu_iu_srlz_op_encode(7)      -> eu_iu_srlz_op_encode(7)      141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 * 1
eu_iu_srlz_op_encode(8)      -> eu_iu_srlz_op_encode(8)      141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 * 1
eu_iu_srlz_op_encode(9)      -> eu_iu_srlz_op_encode(9)      141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 1
eu_iu_srlz_op_encode(11)     -> eu_iu_srlz_op_encode(11)     141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 * 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1      78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1      78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.clka_1    78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_1 -> slow_mode.c1_2      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_1 -> slow_mode.c2_2      78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_1:cb_clk_32_1 -> slow_mode.clka_2    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_2:cb_clk_32_1 -> slow_mode.c1_3      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_2:cb_clk_32_1 -> slow_mode.c2_3      78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_2:cb_clk_32_1 -> slow_mode.clka_3    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_1 -> slow_mode.c1_4      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_3:cb_clk_32_1 -> slow_mode.c2_4      78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_3:cb_clk_32_1 -> slow_mode.clka_4    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_4:cb_clk_32_1 -> slow_mode.c1_5      78.50 / 78.50 / 237.91 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL

```

Pin/Port	-> Net	Capacitance Limit / AdjLim / Actual	Slew Limit / AdjLim / Actual	Fanout
c2@slow_mode.clockblock_4:cb_clk_32_1	-> slow_mode.c2_5		78.50 / 78.50 / 239.37	*
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_32_1	-> slow_mode.clka_5		78.50 / 78.50 / 228.73	*
200.00 / 200.00 / 198.79	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32_1	-> slow_mode.c1		78.50 / 78.50 / 237.92	*
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32_1	-> slow_mode.c2		78.50 / 78.50 / 239.37	*
200.00 / 200.00 / 60.00	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
clka@slow_mode.clockblock_5:cb_clk_32_1	-> slow_mode.clka		78.50 / 78.50 / 228.73	*
200.00 / 200.00 / 198.79	14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL			
y@C167:cs_invv01c	-> dcd_succ_last_t1&0		68.00 / 68.00 / 1011.00	* 301.00
/ 301.00 / 3676.28	* 1 KEEP_BTR			
y@C2013:cs_invv01c	-> N18&0		68.00 / 68.00 / 1011.00	* 301.00 /

301.00 / 3608.92 * 1		
y@C2061:cs_nnd2n02c	-> N1371	70.00 / 70.00 / 86.53 * 290.00 /
290.00 / 309.86 * 3		
y@C2082:cs_invvn01c	-> N146&0	68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 * 1		
y@C2224:cs_invvn06c	-> N1728	208.00 / 208.00 / 214.85 * 290.00 /
290.00 / 285.51 8		
y@C2393:cs_nnd2n02c	-> iu_reset_op_c_t1&0	70.00 / 70.00 / 1044.40 *
290.00 / 290.00 / 3683.69 * 3		
y@C2496:cs_nnd4n03c	-> N1435	85.00 / 85.00 / 97.83 * 290.00 /
290.00 / 353.82 * 5		
y@C2646:cs_invvn04c	-> N1645	133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 273.28 6		
y@C2724:cs_nnd2n02c	-> N23	70.00 / 70.00 / 92.41 * 290.00 /
290.00 / 326.23 * 3		
y@C2750:cs_invvn05c	-> N1333	167.00 / 167.00 / 180.24 * 290.00 /
290.00 / 266.70 8		
y@C2794:cs_ao12n03c	-> N73	86.00 / 86.00 / 92.41 * 290.00 /
290.00 / 466.30 * 3		
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q		247.00 / 247.00 / 256.34 *
290.00 / 290.00 / 205.99 8		

[BD-500900]: (W) There were 57 electrical violations.

> echo {Standard Late Time}

Standard Late Time

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/lx.tcl

> echo {Delay Effort = 5}

Delay Effort = 5

> echo {Area Effort = 4}

Area Effort = 4

> echo {initialize window repower}

initialize window repower

> hide -clear -cells { cs_ao12f }

> find cell cs_ao12f*

> hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...

> hide -clear -cells { cs_nnd2f cs_nnd2w }

> find cell cs_nnd2f*

> hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...

> find cell cs_nnd2w*

> hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...

> hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }

> find cell cs_nnd3f*

> hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...

> find cell cs_nnd3h*

> hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...

> find cell cs_nnd3w*

> hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...

> find cell cs_nnd3y*

> hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...

> hide -clear -cells { cs_nor2f cs_nor2w }

> find cell cs_nor2f*

> hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...

> find cell cs_nor2w*

> hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...

```

> hide -clear -cells { cs_nor3f cs_nor3h }
> find cell cs_nor3f*
> hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
> find cell cs_nor3h*
> hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
> hide -clear -cells { cs_oa12f }
> find cell cs_oa12f*
> hide -clear -cells {cs_oa12f03b cs_oa12f03c cs_oa12f03d ...
> hide -clear -cells { "cs_invvv" }
> find cell cs_invvv*
> hide -clear -cells {cs_invvv01b cs_invvv01c cs_invvv01d ...
> hide -clear -cells { cs_ao12v cs_ao12g }
> find cell cs_ao12v*
> hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
> find cell cs_ao12g*
> hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
> hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
> find cell cs_nnd2v*
> hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
> find cell cs_nnd2g*
> hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
> find cell cs_nnd2x*
> hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
> hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
> find cell cs_nnd3v*
> hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
> find cell cs_nnd3g*
> hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
> find cell cs_nnd3i*
> hide -clear -cells {cs_nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
> find cell cs_nnd3x*
> hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
> find cell cs_nnd3z*
> hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
> hide -clear -cells { cs_nnd4v }
> find cell cs_nnd4v*
> hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
> hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
> find cell cs_nor2v*
> hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
> find cell cs_nor2g*
> hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
> find cell cs_nor2x*
> hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
> hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
> find cell cs_nor3v*
> hide -clear -cells {cs_nor3v03b cs_nor3v03c cs_nor3v03d ...
> find cell cs_nor3g*
> hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...
> find cell cs_nor3i*
> hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
> hide -clear -cells { cs_ao12v cs_ao12g }
> find cell cs_ao12v*
> hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
> find cell cs_ao12g*

```

```

> hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
> init_gain_based_repower REPOWER_INTERVAL(8)
Delays are given in units of 1.000000e-12 seconds
Fuzziness is 5.000000e-02[ET-0203]: Timing top level created for design: def_proto, analysis mode:
default.

```

```

> str_parm unhide_rules
> hide_def_with_view XPANDVIEW,SRULE
> syn_hide_boxes_clear
> copy_hide
> trulegen
[BD-502300]: Created 80 timing expansions.
> traceset {syntrace HOWMANY}
[traceset]: trace string = syntrace HOWMANY
[tracing]: set trace variable syntrace to 20
> setmaxfanout
> set_maxarea
> nextbox syn_hide_set(!HIDE_DOMINANT)
[
>>]: nextbox( syn_hide_set(!HIDE_DOMINANT) );
[syn_hide_set]: Rel 0.2 Compiled on Mar 10 1999 at 05:19:36.
[syn_hide_set]: Setting synthesis hide = 0, clear = 4
[syn_hide_set]: Number of boxes affected was 946.
> write_end_point_report -points 10
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 21:58:28 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 10

Cause of Slack Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2

Loop
CLOCK + ADJUST) ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO	Delay/ Cell	Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	----	----------------	------------------------	-------

1 dcd_succ_last_t1	R C3+R	3242	-2243	3621	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	R C3+R	3242	-2243	3621	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	3242	-2243	3621	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	3242	-2243	3621	1011	1 cs_invvn	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1337	-2243	65	302	4 cs_invvn	01c NOT
1906 N675							
---->{a} C2738/y	F C3+R	1337	-2243	65	302	4 cs_nnd2n	14c NAND
0 N675							
----> C2738/b	R C3+R	1289	-2243	93	1261	4 cs_nnd2n	14c NAND
48 dcd_success&0							
----> C2734rwr/y	R C3+R	1289	-2243	93	1261	4 cs_invvn	19c NOT
0 dcd_success&0							
----> C2734rwr/a	F C3+R	1236	-2243	40	310	1 cs_invvn	19c NOT
53 N1097							
----> C2728rwr/y	F C3+R	1236	-2243	40	310	1 cs_invvn	16c NOT
0 N1097							
----> C2728rwr/a	R C3+R	1205	-2243	84	181	2 cs_invvn	16c NOT
31 N1692							
---->{b} C2725rwr/y	R C3+R	1205	-2243	84	181	2 cs_nnd2n	13c NAND
0 N1692							
----> C2725rwr/a	F C3+R	1148	-2243	98	161	2 cs_nnd2n	13c NAND
57 N1479							
---->{c} C2721rwr/y	F C3+R	1148	-2243	98	161	2 cs_nnd3n	12c NAND
0 N1479							
----> C2721rwr/a	R C3+R	1085	-2243	184	115	2 cs_nnd3n	12c NAND
63 N1497							
---->{d} C2709rwr/y	R C3+R	1085	-2243	184	115	2 cs_nor3n	10c NOR
0 N1497							
----> C2709rwr/c	F C3+R	973	-2243	97	52	1 cs_nor3n	10c NOR
112 N1976							
---->{e} C2579rwr_0_0/y	F C3+R	973	-2243	97	52	1 cs_nnd3n	07c NAND
0 N1976							
----> C2579rwr_0_0/b	R C3+R	909	-2243	223	61	2 cs_nnd3n	07c NAND
64 N127							
----> C2538/y	R C3+R	909	-2243	223	61	2 cs_invvn	01c NOT 0
N127							
----> C2538/a	F C3+R	785	-2243	85	16	1 cs_invvn	01c NOT 124
blk_dcd_in(0)							
---->{f} C2480rwr/y	F C3+R	785	-2243	85	16	1 cs_nnd3n	02c NAND
0 blk_dcd_in(0)							

```

----> C2480rwr/a          R C3+R   730 -2243  121  17 1 cs_nnd3n  02c NAND
55 N393
---->{g} C2324/y          R C3+R   730 -2243  121  17 1 cs_nnd2n  02c NAND
0 N393
----> C2324/b             F C3+R   641 -2243  203  215 8 cs_nnd2n  02c NAND
89 N1728
----> C2224/y             F C3+R   641 -2243  203  215 8 cs_invvn  06c NOT    0
N1728
----> C2224/a             R C3+R   497 -2243  300   87 3 cs_invvn  06c NOT
144 N1371
---->{h} C2061/y          R C3+R   497 -2243  300   87 3 cs_nnd2n  02c NAND
0 N1371
----> C2061/a             F C3+R   328 -2243   96  124 4 cs_nnd2n  02c NAND
169 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/2_out_n F C3+R   328 -2243   96  124 4 cl_nnd2n  07c
SRL    0 dcd_cyl_cnt_q(0)
----> dcd_cyl_cnt.reg_n.lat_0/c2    R C3+    160  N/C   60  222 13 cl_nnd2n  07c SRL
168 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+    160  N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
-----
--
2 dcd_succ_last_t1      F C3+R  2696 -1697  2124 1011 1 PO          0
dcd_succ_last_t1
RAT                      999                      0
----> BOX714/OUT          F C3+R  2696 -1697  2124 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          F C3+R  2696 -1697  2124 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1&0
----> C167/y             F C3+R  2696 -1697  2124 1011 1 cs_invvn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a             R C3+R   1240 -1697   97  302 4 cs_invvn  01c NOT
1457 N675
---->{a} C2738/y          R C3+R   1240 -1697   97  302 4 cs_nnd2n  14c NAND
0 N675
----> C2738/b             F C3+R   1179 -1697   56 1261 4 cs_nnd2n  14c NAND
61 dcd_success&0
----> C2734rwr/y          F C3+R   1179 -1697   56 1261 4 cs_invvn  19c NOT
0 dcd_success&0
----> C2734rwr/a          R C3+R   1138 -1697   58  310 1 cs_invvn  19c NOT
41 N1097
----> C2728rwr/y          R C3+R   1138 -1697   58  310 1 cs_invvn  16c NOT
0 N1097
----> C2728rwr/a          F C3+R   1099 -1697   61  181 2 cs_invvn  16c NOT
39 N1692
---->{b} C2725rwr/y        F C3+R   1099 -1697   61  181 2 cs_nnd2n  13c NAND
0 N1692
----> C2725rwr/a          R C3+R   1056 -1697   98  161 2 cs_nnd2n  13c NAND
43 N1479
---->{c} C2721rwr/y        R C3+R   1056 -1697   98  161 2 cs_nnd3n  12c NAND
0 N1479
----> C2721rwr/a          F C3+R   992 -1697   86  115 2 cs_nnd3n  12c NAND
64 N1497
---->{d} C2709rwr/y        F C3+R   992 -1697   86  115 2 cs_nor3n  10c NOR
0 N1497

```

----> C2709rwr/c 65 N1976	R C3+R 927 -1697 117 52 1 cs_nor3n 10c NOR
---->{e} C2579rwr_0_0/y 0 N1976	R C3+R 927 -1697 117 52 1 cs_nnd3n 07c NAND
----> C2579rwr_0_0/b 85 N127	F C3+R 842 -1697 131 61 2 cs_nnd3n 07c NAND
----> C2538/y N127	F C3+R 842 -1697 131 61 2 cs_invvn 01c NOT 0
----> C2538/a blk_dcd_in(0)	R C3+R 752 -1697 96 16 1 cs_invvn 01c NOT 90
---->{f} C2480rwr/y 0 blk_dcd_in(0)	R C3+R 752 -1697 96 16 1 cs_nnd3n 02c NAND
----> C2480rwr/a 64 N393	F C3+R 688 -1697 90 17 1 cs_nnd3n 02c NAND
---->{g} C2324/y 0 N393	F C3+R 688 -1697 90 17 1 cs_nnd2n 02c NAND
----> C2324/b 56 N1728	R C3+R 632 -1697 286 215 8 cs_nnd2n 02c NAND
----> C2224/y N1728	R C3+R 632 -1697 286 215 8 cs_invvn 06c NOT 0
----> C2224/a 180 N1371	F C3+R 452 -1697 212 87 3 cs_invvn 06c NOT
---->{h} C2061/y 0 N1371	F C3+R 452 -1697 212 87 3 cs_nnd2n 02c NAND
----> C2061/a 137 dcd_cyl_cnt_q(0)	R C3+R 315 -1697 111 124 4 cs_nnd2n 02c NAND
----> dcd_cyl_cnt.reg_n.lat_0/2_out_n SRL 0 dcd_cyl_cnt_q(0)	R C3+R 315 -1697 111 124 4 cl_nnd2n 07c
----> dcd_cyl_cnt.reg_n.lat_0/c2 155 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_nnd2n 07c SRL
----> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB

3 local_milli_t2.reg_n.lat_0/a 46 N2054	F C3+R 2888 -1574 72 31 1 cl_invvn 07c SRL
Setup local_milli_t2.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
----> C3011/y N2054	F C3+R 2888 -1574 72 31 1 cs_invvn 07c NOT 0
----> C3011/a 37 N73	R C3+R 2851 -1574 466 92 3 cs_invvn 07c NOT
---->{a} C2794/y 0 N73	R C3+R 2851 -1574 466 92 3 cs_ao12n 03c AOI
----> C2794/a2 253 N1866	F C3+R 2598 -1574 157 18 1 cs_ao12n 03c AOI
---->{b} C2555/y 0 N1866	F C3+R 2598 -1574 157 18 1 cs_ao12n 03c AOI
----> C2555/b 109 iu_reset_op_c_t1&0	R C3+R 2489 -1574 3605 1044 3 cs_ao12n 03c AOI
---->{c} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2489 -1574 3605 1044 3 cs_nnd2n 02c NAND
----> C2393/a 2011 gbfont_6	F C3+R 479 -1574 89 137 3 cs_nnd2n 02c NAND
----> gbfont_6/y	F C3+R 479 -1574 89 137 3 cs_invvn 09c NOT 0

```

gbfonet_6
----> gbfozell_6/a          R C3+R    416 -1574  201  43 1 cs_invn  09c NOT
62 N2031
---->{d} C2162/y          R C3+R    416 -1574  201  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/c             F C3+R    303 -1574   57  49 3 cs_nnd3n  02c NAND
113 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n    F C3+R    303 -1574   57  49 3 cl_invn  07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2          R C3+    160  N/C   60 239 14 cl_invn  07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2        R C3+    160  N/C   60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

--
4 local_milli_t1.reg_n.lat_0/a      F C3+R   2888 -1574   72  31 1 cl_invn  07c SRL
46 N2052
Setup local_milli_t1.reg_n.lat_0/c1    F C3-    160          60 238 14 cl_invn  07c
1200 slow_mode.c1_4
----> C3008/y             F C3+R   2888 -1574   72  31 1 cs_invn  07c NOT    0
N2052
----> C3008/a            R C3+R   2851 -1574  466  92 3 cs_invn  07c NOT
37 N73
---->{a} C2794/y          R C3+R   2851 -1574  466  92 3 cs_ao12n  03c AOI
0 N73
----> C2794/a2            F C3+R   2598 -1574  157  18 1 cs_ao12n  03c AOI
253 N1866
---->{b} C2555/y          F C3+R   2598 -1574  157  18 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b            R C3+R   2489 -1574 3605 1044 3 cs_ao12n  03c AOI
109 iu_reset_op_c_t1&0
---->{c} C2393/y          R C3+R   2489 -1574 3605 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a            F C3+R    479 -1574   89 137 3 cs_nnd2n  02c NAND
2011 gbfonet_6
----> gbfozell_6/y        F C3+R    479 -1574   89 137 3 cs_invn  09c NOT    0
gbfonet_6
----> gbfozell_6/a        R C3+R    416 -1574  201  43 1 cs_invn  09c NOT
62 N2031
---->{d} C2162/y          R C3+R    416 -1574  201  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/c            F C3+R    303 -1574   57  49 3 cs_nnd3n  02c NAND
113 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n    F C3+R    303 -1574   57  49 3 cl_invn  07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2          R C3+    160  N/C   60 239 14 cl_invn  07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2        R C3+    160  N/C   60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

--
5 local_milli.reg_n.lat_0/a      F C3+R   2888 -1574   72  31 1 cl_invn  07c SRL
46 N2040
Setup local_milli.reg_n.lat_0/c1    F C3-    160          60 238 14 cl_invn  07c    1200
slow_mode.c1_2

```

----> C2962/y N2040	F C3+R	2888	-1574	72	31	1	cs_invvn	07c NOT	0
----> C2962/a 37 N73	R C3+R	2851	-1574	466	92	3	cs_invvn	07c NOT	
---->{a} C2794/y 0 N73	R C3+R	2851	-1574	466	92	3	cs_ao12n	03c AOI	
----> C2794/a2 253 N1866	F C3+R	2598	-1574	157	18	1	cs_ao12n	03c AOI	
---->{b} C2555/y 0 N1866	F C3+R	2598	-1574	157	18	1	cs_ao12n	03c AOI	
----> C2555/b 109 iu_reset_op_c_t1&0	R C3+R	2489	-1574	3605	1044	3	cs_ao12n	03c AOI	
---->{c} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2489	-1574	3605	1044	3	cs_nnd2n	02c NAND	
----> C2393/a 2011 gbfonet_6	F C3+R	479	-1574	89	137	3	cs_nnd2n	02c NAND	
----> gbfozell_6/y gbfonet_6	F C3+R	479	-1574	89	137	3	cs_invvn	09c NOT	0
----> gbfozell_6/a 62 N2031	R C3+R	416	-1574	201	43	1	cs_invvn	09c NOT	
---->{d} C2162/y 0 N2031	R C3+R	416	-1574	201	43	1	cs_nnd3n	02c NAND	
----> C2162/c 113 exc_cond_q	F C3+R	303	-1574	57	49	3	cs_nnd3n	02c NAND	
----> exc_cond.reg_n.lat_0/l2_out_n 0 exc_cond_q	F C3+R	303	-1574	57	49	3	cl_invvn	07d SRL	
----> exc_cond.reg_n.lat_0/c2 143 slow_mode.c2_4	R C3+	160	N/C	60	239	14	cl_invvn	07d SRL	
----> slow_mode.clockblock_3/c2 0 slow_mode.c2_4	R C3+	160	N/C	60	239	14	cb_clk_32_1	LCB	

6 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT	R C3+R	2489	-1490	3605	1011	1	PO		0
----> BOX716/OUT 0 iu_reset_op_c_t1	R C3+R	2489	-1490	3605	1011	1	IOPAD	IOPAD	
----> BOX716/IN 0 iu_reset_op_c_t1&0	R C3+R	2489	-1490	3605	1044	3	IOPAD	IOPAD	
---->{a} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2489	-1574	3605	1044	3	cs_nnd2n	02c NAND	
----> C2393/a 2011 gbfonet_6	F C3+R	479	-1574	89	137	3	cs_nnd2n	02c NAND	
----> gbfozell_6/y gbfonet_6	F C3+R	479	-1574	89	137	3	cs_invvn	09c NOT	0
----> gbfozell_6/a 62 N2031	R C3+R	416	-1574	201	43	1	cs_invvn	09c NOT	
---->{b} C2162/y 0 N2031	R C3+R	416	-1574	201	43	1	cs_nnd3n	02c NAND	
----> C2162/c 113 exc_cond_q	F C3+R	303	-1574	57	49	3	cs_nnd3n	02c NAND	
----> exc_cond.reg_n.lat_0/l2_out_n 0 exc_cond_q	F C3+R	303	-1574	57	49	3	cl_invvn	07d SRL	
----> exc_cond.reg_n.lat_0/c2 143 slow_mode.c2_4	R C3+	160	N/C	60	239	14	cl_invvn	07d SRL	


```

----> slow_mode.clockblock_3/c2          R C3+   160   N/C   60  239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

--
    7 local_milli_t2.reg_n.lat_0/a          R C3+R   2832 -1469   88   31 1 cl_invvn 07c SRL
-3 N2054
Setup local_milli_t2.reg_n.lat_0/c1        F C3-    160         60  238 14 cl_invvn 07c
1200 slow_mode.c1_4
----> C3011/y          R C3+R   2832 -1469   88   31 1 cs_invvn 07c NOT    0
N2054
----> C3011/a          F C3+R   2771 -1469   263   92 3 cs_invvn 07c NOT
62 N73
---->{a} C2794/y        F C3+R   2771 -1469   263   92 3 cs_ao12n 03c AOI
0 N73
----> C2794/b          R C3+R   2604 -1469    87   17 1 cs_ao12n 03c AOI
166 N1988
---->{b} C2748/y        R C3+R   2604 -1469    87   17 1 cs_nnd2n 02c NAND
0 N1988
----> C2748/a          F C3+R   2546 -1469    92   17 1 cs_nnd2n 02c NAND
58 N639
---->{c} C2466/y        F C3+R   2546 -1469    92   17 1 cs_nnd2n 02c NAND
0 N639
----> C2466/b          R C3+R   2489 -1469  3605  1044 3 cs_nnd2n 02c NAND
57 iu_reset_op_c_t1&0
---->{d} C2393/y        R C3+R   2489 -1574  3605  1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   479  -1574    89   137 3 cs_nnd2n 02c NAND
2011 gbfonet_6
----> gbfcocell_6/y      F C3+R   479  -1574    89   137 3 cs_invvn 09c NOT    0
gbfonet_6
----> gbfcocell_6/a      R C3+R   416  -1574   201   43 1 cs_invvn 09c NOT
62 N2031
---->{e} C2162/y        R C3+R   416  -1574   201   43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/c          F C3+R   303  -1574    57   49 3 cs_nnd3n 02c NAND
113 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n        F C3+R   303  -1574    57   49 3 cl_invvn 07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2          R C3+    160   N/C   60  239 14 cl_invvn 07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2          R C3+    160   N/C   60  239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

--
    8 local_milli_t1.reg_n.lat_0/a          R C3+R   2832 -1469   88   31 1 cl_invvn 07c SRL
-3 N2052
Setup local_milli_t1.reg_n.lat_0/c1        F C3-    160         60  238 14 cl_invvn 07c
1200 slow_mode.c1_4
----> C3008/y          R C3+R   2832 -1469   88   31 1 cs_invvn 07c NOT    0
N2052
----> C3008/a          F C3+R   2771 -1469   263   92 3 cs_invvn 07c NOT
62 N73
---->{a} C2794/y        F C3+R   2771 -1469   263   92 3 cs_ao12n 03c AOI
0 N73
----> C2794/b          R C3+R   2604 -1469    87   17 1 cs_ao12n 03c AOI

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166 N1988	R C3+R	2604	-1469	87	17	1 cs_nnd2n	02c NAND
---->{b} C2748/y 0 N1988	F C3+R	2546	-1469	92	17	1 cs_nnd2n	02c NAND
----> C2748/a 58 N639	F C3+R	2546	-1469	92	17	1 cs_nnd2n	02c NAND
---->{c} C2466/y 0 N639	R C3+R	2489	-1469	3605	1044	3 cs_nnd2n	02c NAND
----> C2466/b 57 iu_reset_op_c_t1&0	R C3+R	2489	-1574	3605	1044	3 cs_nnd2n	02c NAND
---->{d} C2393/y 0 iu_reset_op_c_t1&0	F C3+R	479	-1574	89	137	3 cs_nnd2n	02c NAND
----> C2393/a 2011 gbfonet_6	F C3+R	479	-1574	89	137	3 cs_invvn	09c NOT
----> gbfozell_6/y gbfonet_6	R C3+R	416	-1574	201	43	1 cs_invvn	09c NOT
----> gbfozell_6/a 62 N2031	R C3+R	416	-1574	201	43	1 cs_nnd3n	02c NAND
---->{e} C2162/y 0 N2031	F C3+R	303	-1574	57	49	3 cs_nnd3n	02c NAND
----> C2162/c 113 exc_cond_q	F C3+R	303	-1574	57	49	3 cl_invvn	07d SRL
----> exc_cond.reg_n.lat_0/l2_out_n 0 exc_cond_q	R C3+	160	N/C	60	239	14 cl_invvn	07d SRL
----> exc_cond.reg_n.lat_0/c2 143 slow_mode.c2_4	R C3+	160	N/C	60	239	14 cb_clk_32_1	LCB
----> slow_mode.clockblock_3/c2 0 slow_mode.c2_4	<hr/>						
-- 9 local_milli.reg_n.lat_0/a	R C3+R	2832	-1469	88	31	1 cl_invvn	07c SRL
-3 N2040	F C3-	160		60	238	14 cl_invvn	07c
Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2	R C3+R	2832	-1469	88	31	1 cs_invvn	07c NOT
----> C2962/y N2040	F C3+R	2771	-1469	263	92	3 cs_invvn	07c NOT
----> C2962/a 62 N73	F C3+R	2771	-1469	263	92	3 cs_ao12n	03c AOI
---->{a} C2794/y 0 N73	R C3+R	2604	-1469	87	17	1 cs_ao12n	03c AOI
----> C2794/b 166 N1988	R C3+R	2604	-1469	87	17	1 cs_nnd2n	02c NAND
---->{b} C2748/y 0 N1988	F C3+R	2546	-1469	92	17	1 cs_nnd2n	02c NAND
----> C2748/a 58 N639	F C3+R	2546	-1469	92	17	1 cs_nnd2n	02c NAND
---->{c} C2466/y 0 N639	R C3+R	2489	-1469	3605	1044	3 cs_nnd2n	02c NAND
----> C2466/b 57 iu_reset_op_c_t1&0	R C3+R	2489	-1574	3605	1044	3 cs_nnd2n	02c NAND
---->{d} C2393/y 0 iu_reset_op_c_t1&0	F C3+R	479	-1574	89	137	3 cs_nnd2n	02c NAND
----> C2393/a 2011 gbfonet_6	F C3+R	479	-1574	89	137	3 cs_invvn	09c NOT
----> gbfozell_6/y gbfonet_6							

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----> gbfcocell_6/a          R C3+R   416 -1574  201  43 1 cs_invrn  09c NOT
62 N2031
---->{e} C2162/y            R C3+R   416 -1574  201  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/c                F C3+R   303 -1574   57  49 3 cs_nnd3n  02c NAND
113 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n  F C3+R   303 -1574   57  49 3 cl_invrn  07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2      R C3+    160  N/C   60 239 14 cl_invrn  07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2    R C3+    160  N/C   60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

--
10 idcdsuc_err          R C3+R  2126 -1127  3605 1011 1 PO          0
N146
RAT                      999                      0
----> BOX750/OUT          R C3+R  2126 -1127  3605 1011 1 IOPAD    IOPAD
0 N146
----> BOX750/IN          R C3+R  2126 -1127  3605 1011 1 IOPAD    IOPAD
0 N146&0
----> C2082/y            R C3+R  2126 -1127  3605 1011 1 cs_invrn  01c NOT
0 N146&0
----> C2082/a            F C3+R   295 -1127   48  32 2 cs_invrn  01c NOT
1831 dcdsuc_err_q
----> dcdsuc_err.reg_n.lat_0/l2_out_n  F C3+R   295 -1127   48  32 2 cl_nnd2n  07c
SRL  0 dcdsuc_err_q
----> dcdsuc_err.reg_n.lat_0/c2      R C3+    160  N/C   60 222 13 cl_nnd2n  07c-SRL
135 slow_mode.c2_1
----> slow_mode.clockblock/c2    R C3+    160  N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
> measure
[levelize][get_ltor]: number of levels = 19

```

The model <IDCDSUC> has:

```

Primary Inputs   =      122
Primary Outputs  =      73
Primary BIDs     =       0
Signals          =     1167
Gate Count       =      946
Connections      =     1783
Master REG Bits  =      83
Slave REG Bits   =      83
Internal Area    =     4487
External Area    =       0
Gates/Connects  =     0.530566
Fanout Count     =     1783
Average Fanout   =     1.527849
Avg Tech Box Size =     4.743129
Tech Box Size Stddev =     0.010329
Power            =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 792
 Real boxes = 571
 Real connections = 1408
 Real LSTs = 2200
 Real ICells/box = 7.858144
 Real LSTs/box = 3.852890
 Real nets/box = 1.387040

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
5		cs_ao12n03c	03c	>	AOI	4	0	0.000	20	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
180		BRKPT		>	BRKPT	0	0	0.000	0	0	0.000
195		IOPAD		>	IOPAD	0	0	0.000	0	0	0.000
166		cs_nnd2n02c	02c	>	NAND	3	0	0.000	498	0	0.000
24		cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
3		cs_nnd2n05c	05c	>	NAND	4	0	0.000	12	0	0.000
6		cs_nnd4n03c	03c	>	NAND	5	0	0.000	30	0	0.000
4		cs_nnd2n13c	13c	>	NAND	15	0	0.000	60	0	0.000
3		cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
2		cs_nnd3n07c	07c	>	NAND	6	0	0.000	12	0	0.000
3		cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
1		cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
2		cs_nnd2n14c	14c	>	NAND	19	0	0.000	38	0	0.000
1		cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1		cs_nnd4n09c	09c	>	NAND	16	0	0.000	16	0	0.000
4		cs_nnd2n07c	07c	>	NAND	4	0	0.000	16	0	0.000
1		cs_nnd2n11c	11c	>	NAND	11	0	0.000	11	0	0.000
1		cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3n09c	09c	>	NAND	12	0	0.000	12	0	0.000
10		cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1		cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1		cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
2		cs_nor2n04c	04c	>	NOR	3	0	0.000	6	0	0.000
1		cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
102		cs_invvn01c	01c	>	NOT	2	0	0.000	204	0	0.000
5		cs_invvn11c	11c	>	NOT	6	0	0.000	30	0	0.000
6		cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
21		cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
7		cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
33		cs_invvn07c	07c	>	NOT	2	0	0.000	66	0	0.000
4		cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
9		cs_invvn06c	06c	>	NOT	2	0	0.000	18	0	0.000
13		cs_invvn05c	05c	>	NOT	2	0	0.000	26	0	0.000
4		cs_invvn13c	13c	>	NOT	8	0	0.000	32	0	0.000
3		cs_invvn08c	08c	>	NOT	4	0	0.000	12	0	0.000
7		cs_invvn02c	02c	>	NOT	2	0	0.000	14	0	0.000
1		cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
5		cs_invvn04c	04c	>	NOT	2	0	0.000	10	0	0.000
1		cs_invvn18c	18c	>	NOT	20	0	0.000	20	0	0.000
3		cs_invvn16c	16c	>	NOT	14	0	0.000	42	0	0.000
1		cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
1		cs_oa21n04c	04c	>	OAI	5	0	0.000	5	0	0.000

1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
1	cs_oa21n05c	05c	>	OAI	8	0	0.000	8	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	1	*
14	2	**

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	2	**
6	6	*****
7	4	****
8	4	****
9	1	*
10	6	*****
12	1	*
14	1	*
15	5	*****
16	4	****
17	7	*****
18	2	**
19	14	*****

The Histogram Of Fanin vs. Box

	# of Fanin	Ops	
1	405	400* plus *****	
2	203	200* plus ***	
3	37	*****	
4	16	*****	

The Histogram Of Fanout vs. Net

	# of Fanout	Nets	
1	964	950* plus *****	
2	102	100* plus **	
3	39	*****	
4	17	*****	
5	8	*****	
6	11	*****	
7	2	**	
8	4	****	
13	3	***	
14	16	*****	
15	1	*	

[End of measure]

[measure]: Execution time was 0.5 seconds.

> randsim q

[

>>]: randsim(q);

> checksrc

[BD-40000]: checksrc CMVC version 1.27 compiled on Apr 13 1999 at 18:00:56

[BD-40132]: Network IDCDSUC has no potential problems.

> is_parm new_assert

> set_slew_prop OFF

[set_slew_prop]: Setting slew propagation to 0 (OFF)

> tc_parm CHK_SINKSLEW(N)

[tc_parm]: CMVC version 1.26.2.1 compiled on Apr 1 1999 at 05:20:31.

> tc_parm {PINTYPE(OUTPUT_PIN),OFFSET(0) MARGIN(0),ATTEMPT...

> tc_parm USE_AREA,BENEFIT_UNITS(0)

[tc_parm]: benefit units factor is 0.0002

> measure

[levelize][get_ltor]: number of levels = 19

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Primary Outputs	=	73
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Signals	=	1167
Gate Count	=	946
Connections	=	1783
Master REG Bits	=	83
Slave REG Bits	=	83
Internal Area	=	4487

External Area = 0
 Gates/Connects = 0.530566
 Fanout Count = 1783
 Average Fanout = 1.527849
 Avg Tech Box Size = 4.743129
 Tech Box Size Stddev = 0.010329
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 792
 Real boxes = 571
 Real connections = 1408
 Real LSTs = 2200
 Real ICells/box = 7.858144
 Real LSTs/box = 3.852890
 Real nets/box = 1.387040
 Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7	cs_ao22n03c	03c >	AOI	6	0	0.000	42	0	0.000		
5	cs_ao12n03c	03c >	AOI	4	0	0.000	20	0	0.000		
1	cs_ao22n10c	10c >	AOI	18	0	0.000	18	0	0.000		
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
166	cs_nnd2n02c	02c >	NAND	3	0	0.000	498	0	0.000		
24	cs_nnd3n02c	02c >	NAND	4	0	0.000	96	0	0.000		
3	cs_nnd2n05c	05c >	NAND	4	0	0.000	12	0	0.000		
6	cs_nnd4n03c	03c >	NAND	5	0	0.000	30	0	0.000		
4	cs_nnd2n13c	13c >	NAND	15	0	0.000	60	0	0.000		
3	cs_nnd2n04c	04c >	NAND	3	0	0.000	9	0	0.000		
2	cs_nnd3n07c	07c >	NAND	6	0	0.000	12	0	0.000		
3	cs_nnd2n03c	03c >	NAND	3	0	0.000	9	0	0.000		
1	cs_nnd2n12c	12c >	NAND	12	0	0.000	12	0	0.000		
2	cs_nnd2n14c	14c >	NAND	19	0	0.000	38	0	0.000		
1	cs_nnd3n12c	12c >	NAND	22	0	0.000	22	0	0.000		
1	cs_nnd4n09c	09c >	NAND	16	0	0.000	16	0	0.000		
4	cs_nnd2n07c	07c >	NAND	4	0	0.000	16	0	0.000		
1	cs_nnd2n11c	11c >	NAND	11	0	0.000	11	0	0.000		
1	cs_nnd2n06c	06c >	NAND	4	0	0.000	4	0	0.000		
1	cs_nnd3n09c	09c >	NAND	12	0	0.000	12	0	0.000		
10	cs_nor2n02c	02c >	NOR	3	0	0.000	30	0	0.000		
1	cs_nor3n03c	03c >	NOR	4	0	0.000	4	0	0.000		
1	cs_nor2n12c	12c >	NOR	12	0	0.000	12	0	0.000		
2	cs_nor2n04c	04c >	NOR	3	0	0.000	6	0	0.000		
1	cs_nor3n10c	10c >	NOR	12	0	0.000	12	0	0.000		
102	cs_invvn01c	01c >	NOT	2	0	0.000	204	0	0.000		
5	cs_invvn11c	11c >	NOT	6	0	0.000	30	0	0.000		
6	cs_invvn10c	10c >	NOT	4	0	0.000	24	0	0.000		
21	cs_invvn12c	12c >	NOT	6	0	0.000	126	0	0.000		
7	cs_invvn09c	09c >	NOT	4	0	0.000	28	0	0.000		
33	cs_invvn07c	07c >	NOT	2	0	0.000	66	0	0.000		
4	cs_invvn15c	15c >	NOT	10	0	0.000	40	0	0.000		
9	cs_invvn06c	06c >	NOT	2	0	0.000	18	0	0.000		
13	cs_invvn05c	05c >	NOT	2	0	0.000	26	0	0.000		

4	cs_invvn13c	13c	>	NOT	8	0	0.000	32	0	0.000
3	cs_invvn08c	08c	>	NOT	4	0	0.000	12	0	0.000
7	cs_invvn02c	02c	>	NOT	2	0	0.000	14	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
5	cs_invvn04c	04c	>	NOT	2	0	0.000	10	0	0.000
1	cs_invvn18c	18c	>	NOT	20	0	0.000	20	0	0.000
3	cs_invvn16c	16c	>	NOT	14	0	0.000	42	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
1	cs_oa21n04c	04c	>	OAI	5	0	0.000	5	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
1	cs_oa21n05c	05c	>	OAI	8	0	0.000	8	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of		
Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	1	*
14	2	**

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of		
Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	2	**
6	6	*****
7	4	****
8	4	****
9	1	*
10	6	*****
12	1	*

14	1	*
15	5	*****
16	4	****
17	7	*****
18	2	**
19	14	*****

The Histogram Of Fanin vs. Box

# of	
Fanin	Ops
----	---
1	405 400* plus *****
2	203 200* plus ***
3	37 *****
4	16 *****

The Histogram Of Fanout vs. Net

# of	
Fanout	Nets
-----	----
1	964 950* plus *****
2	102 100* plus **
3	39 *****
4	17 *****
5	8 *****
6	11 *****
7	2 **
8	4 ****
13	3 ***
14	16 *****
15	1 *

[End of measure]

[measure]: Execution time was 0.6 seconds.

> tc_parm SLEW_LIM(100)

> tc_parm CAP_LIM(100)

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/techredund.tcl

> str_parm tgfs_effort

> is_parm no_tech_redund

> is_parm remove_redundant_regs

> make_constants_in nonreg_only

> ignore_trivial_expansions EQNVIEW

> expansions_from_tib EQNVIEW

> expansions_from_eqn EQNVIEW

> copy_def_to_proto EQNVIEW

> apply decide_boolean(EQNVIEW)

generated 1 paths in 70 milliseconds

> apply Hstructure(EQNVIEW)

generated 1 paths in 30 milliseconds

> gen_nonreg_tib_expns TIB_EXPANSIONS

> apply Hunstructure()

> expandable_name

```

> set_nochange
> constmod
> is_parm keep_bad_pgroups
> bad_pgroups_expandable
> nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
[
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(EQNVIEW)) );
[BD-350000]: [test_key]: CMVC version 1.9 compiled on Apr 8 1999 at 05:15:23.
[simple_expand]: Compiled on Mar 10 1999 at 05:19:51.
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 946 objects as matching keyword criteria.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: Compiled on Mar 10 1999 at 05:08:18.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 1169 signals, 946 usage boxes and 1783 connections.
[simple_expand]: Modified 0 gates.
> nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
[
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(TIB_EXPANSIONS)) );
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 946 objects as matching keyword criteria.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 1169 signals, 946 usage boxes and 1783 connections.
[simple_expand]: Modified 0 gates.
> headless
[headless]: Compiled on Mar 10 1999 at 05:13:38.
[headless]: Removed 0 boxes
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 1169 signals, 946 usage boxes and 1783 connections.
> cleanse1
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 1169 signals, 946 usage boxes and 1783 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40000]: invrem CMVC version 1.11 compiled on Apr 8 1999 at 05:03:32
[BD-40000]: onein CMVC version 1.12 compiled on Apr 8 1999 at 05:03:55

```

```

[BD-40000]: twoin CMVC version 1.6 compiled on Apr 8 1999 at 05:04:02
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cleanup]: Compiled on Apr 13 1999 at 18:01:26.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
          The model has 1169 signals, 946 usage boxes and 1783 connections.

[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
        > nochange
        > set_nochange
        > apply {Hstructure( EQNVIEW TIB_EXPANSIONS)}
generated 1 paths in 60 milliseconds
        > rtolbox {Htgsfiredund( 100 )}

[
>>]: rtolbox( Htgsfiredund( 100 ) );
[BD-330000]: Htgsfiredund CMVC version 1.15 compiled on Apr 8 1999 at 05:29:58.
[BD-330500]: Out of 2898 faults found 0 redundancies, eliminated 0, could not decide 0 in 2 seconds.
        > apply Hunstructure()
        > nochange
        > DeleteAllProtosUnderView TIB_EXPANSIONS
[SRULE-17175]: Deleted 5 Proto Boxes
        > randsim q

[
>>]: randsim( q );
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/simple_map.tcl
        > randsim q

[
>>]: randsim( q );
        > is_parm keep_bad_pgroups
        > copyinfo
        > fix_bad_pgroups
[BD-80000]: fix_bad_pgroups CMVC version 1.3 compiled on Apr 8 1999 at 05:22:04
[BD-82400]: Added 0 terminators, deleted 0 pins and tied 0 pins.
        > basetype

[
>>]: nextbox_with_test( test_syn_hide(!HIDE_MAP),genmark );
[test_syn_hide]: Number of objects selected was 946 of 946 checked.
[
>>]: nextnet( geninv );
        > copyinfo
        > nextbox {mapprim, mapterm}

[
>>]: nextbox( mapprim, mapterm );
[BD-80000]: mapprim CMVC version 1.14 compiled on Apr 13 1999 at 18:10:28
[BD-80000]: mapterm CMVC version 1.8 compiled on Apr 8 1999 at 05:24:14
[mapprim]: Execution time was 0.0 seconds.
[BD-83600]: 0 terminators processed 0 dummy nets removed.

```

```

> cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1169 signals, 946 usage boxes and 1783 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: CMVC version 1.12 compiled on Apr 13 1999 at 18:01:28.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1169 signals, 946 usage boxes and 1783 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1169 signals, 946 usage boxes and 1783 connections.
[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
    > nextbox tchname(NOERR)
[
>>]: nextbox( tchname(NOERR) );
[BD-80000]: tchname CMVC version 1.13 compiled on Apr 8 1999 at 05:28:02
NOERR option set
[BD-85300]: Looked at 946 gates, bound 0, 0 had hints.
[tchname]: Execution time was 0.0 seconds.
    > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1169 signals, 946 usage boxes and 1783 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1169 signals, 946 usage boxes and 1783 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1169 signals, 946 usage boxes and 1783 connections.
[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
    > copyinfo

```

```

    > has_children CONSTANT
    > tiegen FOLIM(8)
[BD-80000]: tiegen CMVC version 1.11 compiled on Apr 8 1999 at 05:28:21
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > compare_key_slack_limit TIME_REDUND
-2329.30 Avg: -296.08
comparing keyed new slack -2329.3015 to keyed saved slack
-1122931754048350200000000000000000000000.0000
    > reset_key_slack_limit TIME_REDUND
-2329.30 Avg: -296.08
resetting keyed current slack to -2329.3015
    > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
[BD-500000]: critical CMVC version 1.22 compiled on Apr 13 1999 at 18:21:44
-2329.30 Avg: -296.08
maximum area for proto box IDCDSUC is 4487
[BD-500000]: tswap CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-2329.30 Avg: -296.08
ArrayNum: 15 ArrayMax: 946
-2314.78 Avg: -294.64
ArrayNum: 15 ArrayMax: 946
-2306.24 Avg: -294.08
ArrayNum: 15 ArrayMax: 946
-2299.91 Avg: -293.12
ArrayNum: 15 ArrayMax: 946
-2294.80 Avg: -293.12
ArrayNum: 15 ArrayMax: 946
-2294.50 Avg: -293.42
ArrayNum: 15 ArrayMax: 946
[BD-500304]: 12 pins swapped on 5 gates and 0 gates cloned.
[tswap]: Execution time was 0.5 seconds.
[BD-502000]: Called transforms 30 times and applied 5 of them.
    > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS)}
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS) );
-2294.50 Avg: -293.42
maximum area for proto box IDCDSUC is 4487
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-2294.50 Avg: -293.42
ArrayNum: 15 ArrayMax: 946
-2273.00 Avg: -289.24
ArrayNum: 13 ArrayMax: 946
-2252.61 Avg: -287.39
ArrayNum: 11 ArrayMax: 946

```

```

-2252.05 Avg: -287.35
ArrayNum: 11 ArrayMax: 946
-2250.42 Avg: -287.20
ArrayNum: 11 ArrayMax: 946
[BD-500026]: repower was applied 4 times.
[repower]: Execution time was 0.8 seconds.
[BD-502000]: Called transforms 27 times and applied 4 of them.
    > compare_key_slack_limit TIME_REDUND
-2250.42 Avg: -287.20
comparing keyed new slack -2250.4236 to keyed saved slack -2306.0085
    > reset_key_slack_limit TIME_REDUND
-2250.42 Avg: -287.20
resetting keyed current slack to -2250.4236
    > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
-2250.42 Avg: -287.20
maximum area for proto box IDCDSUC is 4497
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-2250.42 Avg: -287.20
ArrayNum: 11 ArrayMax: 946
-2249.91 Avg: -287.22
ArrayNum: 11 ArrayMax: 946
-2248.67 Avg: -287.28
ArrayNum: 11 ArrayMax: 946
[BD-500304]: 4 pins swapped on 2 gates and 0 gates cloned.
[tswap]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 15 times and applied 2 of them.
    > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}
critical( repower(SCORE(ALL),INC ,NO_VIOLATIONS) );
-2248.67 Avg: -287.28
maximum area for proto box IDCDSUC is 4497
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-2248.67 Avg: -287.28
ArrayNum: 11 ArrayMax: 946
-2242.84 Avg: -286.73
ArrayNum: 11 ArrayMax: 946
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 0.2 seconds.
[BD-502000]: Called transforms 14 times and applied 1 of them.
    > compare_key_slack_limit TIME_REDUND
-2242.84 Avg: -286.73
comparing keyed new slack -2242.8408 to keyed saved slack -2227.9194
    > delete_key_slack_limit TIME_REDUND
    > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
[quick]: CMVC version 1.31 compiled on Apr 1 1999 at 05:18:11.
-2242.84 Avg: -286.73
[onebuff]: Compiled on Mar 31 1999 at 11:33:14.
[onebuff]: setting SCORE option to ALL.

```

```

[onebuff]: setting RE_POWER option.
[onebuff]: setting INC mode.
[onebuff]: setting NO_VIOLATIONS option.
-2242.84 Avg: -286.73
maximum area for proto box IDCDSUC is 4503
[quick]: Number of boxes to process is 946.
[quick]: Number of boxes processed is 0.
-2242.84 Avg: -286.73
[onebuff]: was applied 0 times
      > quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-2242.84 Avg: -286.73
[BD-500000]: dinv CMVC version 1.13 compiled on Apr 13 1999 at 18:30:14
setting SCORE option to ALL.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
-2242.84 Avg: -286.73
maximum area for proto box IDCDSUC is 4503
[quick]: Number of boxes to process is 946.
[quick]: Number of boxes processed is 0.
-2227.45 Avg: -238.89
[BD-500500]: Moved 12 sinks and removed 19 inverters.
      > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS) , repowe...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS) ,
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-2227.45 Avg: -238.89
maximum area for proto box IDCDSUC is 4460
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-2227.45 Avg: -238.89
ArrayNum: 6 ArrayMax: 927
-2189.99 Avg: -233.31
ArrayNum: 6 ArrayMax: 927
-2168.35 Avg: -233.23
ArrayNum: 6 ArrayMax: 927
-2160.94 Avg: -233.27
ArrayNum: 6 ArrayMax: 927
[BD-500026]: repower was applied 3 times.
[repower]: Execution time was 0.3 seconds.
[BD-500026]: repower was applied 3 times.
[repower]: Execution time was 0.3 seconds.
[BD-502000]: Called transforms 24 times and applied 3 of them.
      > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 21:58:43 1999
Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

 Slack Continuation SlkCont Slack due to a point downstream on path
 Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
 Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
 Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
 Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
 Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
 Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ LimitedAT/ Delay/ Failed Test/
 Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj
 NetName

 1 dcd_succ_last_t1 R C3+R 3160 -2161 3847 1011 1 PO 0
 dcd_succ_last_t1
 RAT 999 0
 ----> BOX714/OUT R C3+R 3160 -2161 3847 1011 1 IOPAD IOPAD
 0 dcd_succ_last_t1
 ----> BOX714/IN R C3+R 3160 -2161 3847 1011 1 IOPAD IOPAD
 0 dcd_succ_last_t1&0
 ----> C167/y R C3+R 3160 -2161 3847 1011 1 cs_invvn 01c NOT
 0 dcd_succ_last_t1&0
 ----> C167/a F C3+R 1202 -2161 76 302 4 cs_invvn 01c NOT
 1958 N675
 ---->{a} C2738/y F C3+R 1202 -2161 76 302 4 cs_nnd2n 14b NAND
 0 N675
 ----> C2738/a R C3+R 1148 -2161 183 108 1 cs_nnd2n 14b NAND
 54 last_cycle
 ---->{b} C2487/y R C3+R 1148 -2161 183 108 1 cs_nnd2n 05e NAND
 0 last_cycle
 ----> C2487/b F C3+R 1058 -2161 60 42 2 cs_nnd2n 05e NAND
 90 N1587
 ----> C1952/y F C3+R 1058 -2161 60 42 2 cs_invvn 05b NOT 0


```

N1587
----> C1952/a          R C3+R   1024 -2161   80   53 2 cs_invmn  05b NOT
34 num_dcd_cyl&0(1)
----> BOX679/OUT       R C3+R   1024 -2161   80   53 2 IOPAD    IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN       R C3+R   1024 -2161   80   53 2 IOPAD    IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)   R C3+R   1024 -2161   80   53 2 PI          0
num_dcd_cyl(1)
-----
--
2-dcd_succ_last_t1    F C3+R   2880 -1881  2362 -1011 1 PO          0
dcd_succ_last_t1
RAT                    999                                0
----> BOX714/OUT       F C3+R   2880 -1881  2362 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1
----> BOX714/IN       F C3+R   2880 -1881  2362 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1&0
----> C167/y          F C3+R   2880 -1881  2362 1011 1 cs_invmn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          R C3+R   1284 -1881   130  302 4 cs_invmn  01c NOT
1596 N675
----> {a} C2738/y      R C3+R   1284 -1881   130  302 4 cs_nnd2n  14b NAND
0 N675
----> C2738/a          F C3+R   1192 -1881   195  108 1 cs_nnd2n  14b NAND
93 last_cycle
----> {b} C2487/y      F C3+R   1192 -1881   195  108 1 cs_nnd2n  05e NAND
0 last_cycle
----> C2487/b          R C3+R   1077 -1881   110   42 2 cs_nnd2n  05e NAND
115 N1587
----> C1952/y          R C3+R   1077 -1881   110   42 2 cs_invmn  05b NOT
0 N1587
----> C1952/a          F C3+R   1016 -1881   80   53 2 cs_invmn  05b NOT    61
num_dcd_cyl&0(1)
----> BOX679/OUT       F C3+R   1016 -1881   80   53 2 IOPAD    IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN       F C3+R   1016 -1881   80   53 2 IOPAD    IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)   F C3+R   1016 -1881   80   53 2 PI          0
num_dcd_cyl(1)
-----
--
3 local_milli_t2.reg_n.lat_0/a    F C3+R   2825 -1505   48   31 1 cl_invmn  07c SRL
41 N2054
Setup local_milli_t2.reg_n.lat_0/c1    F C3-    160           60  238 14 cl_invmn  07c
1200 slow_mode.c1_4
----> C3011/y          F C3+R   2825 -1505   48   31 1 cs_invmn  07c NOT    0
N2054
----> C3011/a          R C3+R   2788 -1505  466   92 3 cs_invmn  07c NOT
37 N73
----> {a} C2794/y      R C3+R   2788 -1505  466   92 3 cs_ao12n  03c AOI
0 N73
----> C2794/a2         F C3+R   2547 -1505  115   18 1 cs_ao12n  03c AOI
241 N1866
----> {b} C2555/y      F C3+R   2547 -1505  115   18 1 cs_ao12n  03c AOI

```

```

0 N1866
----> C2555/b          R C3+R   2438  -1505   3912  1044  3 cs_ao12n   03c AOI
109 iu_reset_op_c_t1&0
---->{c} C2393/y       R C3+R   2438  -1505   3912  1044  3 cs_nnd2n   02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   480   -1505    78   137  3 cs_nnd2n   02c NAND
1958 gbfonet_6
----> gbfozell_6/y     F C3+R   480   -1505    78   137  3 cs_invvn   09c NOT    0
gbfonet_6
----> gbfozell_6/a     R C3+R   417   -1505   217   43  1 cs_invvn   09c NOT
64 N2031
---->{d} C2162/y       R C3+R   417   -1505   217   43  1 cs_nnd3n   02c NAND
0 N2031
----> C2162/c          F C3+R   303   -1505    57   49  3 cs_nnd3n   02c NAND
113 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n F C3+R   303   -1505    57   49  3 cl_invvn   07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2 R C3+    160   N/C    60  239 14 cl_invvn   07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2 R C3+    160   N/C    60  239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

> measure

The model <IDCDSUC> has:

```

Primary Inputs   =      122
Primary Outputs  =       73
Primary BIDs     =        0
Signals          =     1148
Gate Count       =      927
Connections      =     1764
Master REG Bits  =       83
Slave REG Bits   =       83
Internal Area    =     4461
External Area    =        0
Gates/Connects  =     0.525510
Fanout Count     =     1764
Average Fanout   =     1.536585
Avg Tech Box Size =     4.812298
Tech Box Size Stddev =    0.010650
Power            =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals     =      773
Real boxes       =      552
Real connections =     1389
Real LSTs        =     2162
Real ICells/box  =     8.081522
Real LSTs/box    =     3.916667
Real nets/box    =     1.400362

```

```

Cell            Total
Each            Cell

```

```

Type Cnt  Boxname      Power Level  Function  Int  Ext  Power  Int  Ext  Power
-----

```

7	cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
5	cs_ao12n03c	03c	>	AOI	4	0	0.000	20	0	0.000
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
180	BRKPT	>	BRKPT		0	0	0.000	0	0	0.000
195	IOPAD	>	IOPAD		0	0	0.000	0	0	0.000
164	cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
24	cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
2	cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000
6	cs_nnd4n03c	03c	>	NAND	5	0	0.000	30	0	0.000
2	cs_nnd2n13c	13c	>	NAND	15	0	0.000	30	0	0.000
3	cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
2	cs_nnd3n07c	07c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05e	05e	>	NAND	4	0	0.000	4	0	0.000
3	cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5	cs_nnd2n07c	07c	>	NAND	4	0	0.000	20	0	0.000
2	cs_nnd2n12c	12c	>	NAND	12	0	0.000	24	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
2	cs_nnd2n14c	14c	>	NAND	19	0	0.000	38	0	0.000
1	cs_nnd4n09c	09c	>	NAND	16	0	0.000	16	0	0.000
1	cs_nnd2n11c	11c	>	NAND	11	0	0.000	11	0	0.000
1	cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n09c	09c	>	NAND	12	0	0.000	12	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n08c	08c	>	NOR	7	0	0.000	7	0	0.000
90	cs_invvn01c	01c	>	NOT	2	0	0.000	180	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
5	cs_invvn10c	10c	>	NOT	4	0	0.000	20	0	0.000
21	cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
29	cs_invvn07c	07c	>	NOT	2	0	0.000	58	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
9	cs_invvn06c	06c	>	NOT	2	0	0.000	18	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
4	cs_invvn13c	13c	>	NOT	8	0	0.000	32	0	0.000
1	cs_invvn05b	05b	>	NOT	2	0	0.000	2	0	0.000
3	cs_invvn08c	08c	>	NOT	4	0	0.000	12	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
5	cs_invvn04c	04c	>	NOT	2	0	0.000	10	0	0.000
1	cs_invvn18c	18c	>	NOT	20	0	0.000	20	0	0.000
3	cs_invvn16c	16c	>	NOT	14	0	0.000	42	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
1	cs_oa21n04c	04c	>	OAI	5	0	0.000	5	0	0.000
1	cs_ao22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
1	cs_ao21n10c	10c	>	OAI	14	0	0.000	14	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000

2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of Fanin	Ops	
1	386	350* plus *****
2	203	200* plus ***
3	37	*****
4	16	*****

The Histogram Of Fanout vs. Net

of
Fanout Nets

	# of Fanout	Nets
1	945	900* plus *****
2	101	100* plus *
3	41	*****
4	16	*****
5	8	*****
6	11	*****
7	2	**
8	4	****
13	3	***
14	16	*****
15	1	*

[End of measure]

[measure]: Execution time was 0.7 seconds.

> traceset {repower_paths HOWMANY}

[traceset]: trace string = repower_paths HOWMANY

[tracing]: set trace variable repower_paths to 20

> tc_parm MARGIN(10000000)

> repower_paths FUZZY(0.02)

initial slack is -2161

after repower paths slack is -1993

> write_end_point_report -points 3 -paths 1

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 21:59:01 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

ARRIVAL TIME + ADJUST)	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST)		
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO	Delay/ Cell	Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	----	----------------	------------------------	-------

```

1 dcd_succ_last_t1          R C3+R    2992 -1993  3847 1011 1 PO          0
dcd_succ_last_t1
RAT          999          0
----> BOX714/OUT          R C3+R    2992 -1993  3847 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          R C3+R    2992 -1993  3847 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y          R C3+R    2992 -1993  3847 1011 1 cs_invvn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          F C3+R    1130 -1993    55 139 4 cs_invvn  01c NOT
1862 N675
---->{a} C2738/y          F C3+R    1130 -1993    55 139 4 cs_nnd2n  14b NAND
0 N675
----> C2738/b          R C3+R    1099 -1993    90 159 3 cs_nnd2n  14b NAND
31 N1692
---->{b} C2725rwr/y          R C3+R    1099 -1993    90 159 3 cs_nnd2n  14c NAND
0 N1692
----> C2725rwr/a          F C3+R    1050 -1993    93 168 2 cs_nnd2n  14c NAND
49 N1479
---->{c} C2721rwr/y          F C3+R    1050 -1993    93 168 2 cs_nnd3n  12c NAND
0 N1479
----> C2721rwr/c          R C3+R    990 -1993    179 95 2 cs_nnd3n  12c NAND
59 N1497
---->{d} C2709rwr/y          R C3+R    990 -1993    179 95 2 cs_nor3n  10c NOR
0 N1497
----> C2709rwr/b          F C3+R    899 -1993    49 52 1 cs_nor3n  10c NOR
92 N1986
---->{e} C2677rwr_0/y          F C3+R    899 -1993    49 52 1 cs_nnd2n  12c NAND
0 N1986
----> C2677rwr_0/b          R C3+R    872 -1993    74 88 2 cs_nnd2n  12c NAND
27 N1094
---->{f} C2909/y          R C3+R    872 -1993    74 88 2 cs_nnd2n  14c NAND
0 N1094
----> C2909/a          F C3+R    835 -1993    80 108 1 cs_nnd2n  14c NAND
37 dcd_mcr41_blk&0
----> BOX615/OUT          F C3+R    835 -1993    80 108 1 IOPAD      IOPAD
0 dcd_mcr41_blk&0
----> BOX615/IN          F C3+R    835 -1993    80 108 1 IOPAD      IOPAD
dcd_mcr41_blk
----> dcd_mcr41_blk          F C3+R    835 -1993    80 108 1 PI          0
dcd mcr41 blk

```

2 dcd_succ_last_t1	F C3+R	2575	-1576	2362	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	F C3+R	2575	-1576	2362	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	F C3+R	2575	-1576	2362	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	F C3+R	2575	-1576	2362	1011	1 cs_invn	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	R C3+R	1139	-1576	93	139	4 cs_invn	01c NOT
1436 N675							
---->{a} C2738/y	R C3+R	1139	-1576	93	139	4 cs_nnd2n	14b NAND
0 N675							
----> C2738/b	F C3+R	1087	-1576	63	159	3 cs_nnd2n	14b NAND
52 N1692							
---->{b} C2725rwr/y	F C3+R	1087	-1576	63	159	3 cs_nnd2n	14c NAND
0 N1692							
----> C2725rwr/a	R C3+R	1045	-1576	135	168	2 cs_nnd2n	14c NAND
42 N1479							
---->{c} C2721rwr/y	R C3+R	1045	-1576	135	168	2 cs_nnd3n	12c NAND
0 N1479							
----> C2721rwr/c	F C3+R	963	-1576	89	95	2 cs_nnd3n	12c NAND
82 N1497							
---->{d} C2709rwr/y	F C3+R	963	-1576	89	95	2 cs_nor3n	10c NOR
0 N1497							
----> C2709rwr/b	R C3+R	915	-1576	73	52	1 cs_nor3n	10c NOR
49 N1986							
---->{e} C2677rwr_0/y	R C3+R	915	-1576	73	52	1 cs_nnd2n	12c NAND
0 N1986							
----> C2677rwr_0/b	F C3+R	877	-1576	50	88	2 cs_nnd2n	12c NAND
37 N1094							
---->{f} C2909/y	F C3+R	877	-1576	50	88	2 cs_nnd2n	14c NAND
0 N1094							
----> C2909/a	R C3+R	850	-1576	80	108	1 cs_nnd2n	14c NAND
27 dcd_mcr41_blk&0							
----> BOX615/OUT	R C3+R	850	-1576	80	108	1 IOPAD	IOPAD
0 dcd_mcr41_blk&0							
----> BOX615/IN	R C3+R	850	-1576	80	108	1 IOPAD	IOPAD
dcd_mcr41_blk							
----> dcd_mcr41_blk	R C3+R	850	-1576	80	108	1 PI	0
dcd_mcr41_blk							

3 local_milli_t2.reg_n.lat_0/a	F C3+R	2825	-1505	48	31	1 cl_invn	07c SRL
41 N2054							
Setup local_milli_t2.reg_n.lat_0/c1	F C3-	160		60	238	14 cl_invn	07c
1200 slow_mode.c1_4							
----> C3011/y	F C3+R	2825	-1505	48	31	1 cs_invn	07c NOT
N2054							
----> C3011/a	R C3+R	2788	-1505	466	92	3 cs_invn	07c NOT
37 N73							
---->{a} C2794/y	R C3+R	2788	-1505	466	92	3 cs_ao12n	03c AOI
0 N73							
----> C2794/a2	F C3+R	2547	-1505	115	18	1 cs_ao12n	03c AOI
241 N1866							

```

---->{b} C2555/y          F C3+R   2547  -1505   115   18 1 cs_ao12n   03c AOI
0 N1866
----> C2555/b             R C3+R   2438  -1505  3912  1044 3 cs_ao12n   03c AOI
109 iu_reset_op_c_t1&0
---->{c} C2393/y          R C3+R   2438  -1505  3912  1044 3 cs_nnd2n   02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a             F C3+R   480   -1505   78   137 3 cs_nnd2n   02c NAND
1958 gbfonet_6
----> gbfonet_6/y         F C3+R   480   -1505   78   137 3 cs_invvn   09c NOT    0
gbfonet_6
----> gbfonet_6/a         R C3+R   417   -1505   217   43 1 cs_invvn   09c NOT
64 N2031
---->{d} C2162/y          R C3+R   417   -1505   217   43 1 cs_nnd3n   02c NAND
0 N2031
----> C2162/c             F C3+R   303   -1505   57   49 3 cs_nnd3n   02c NAND
113 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n F C3+R   303   -1505   57   49 3 cl_invvn   07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2 R C3+    160   N/C    60  239 14 cl_invvn   07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2 R C3+    160   N/C    60  239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

-----
--
-- > measure

```

The model <IDCDSUC> has:

```

Primary Inputs   =      122
Primary Outputs  =      73
Primary BIDs     =       0
Signals          =     1148
Gate Count       =      927
Connections      =     1764
Master REG Bits  =      83
Slave REG Bits   =      83
Internal Area    =     4533
External Area    =       0
Gates/Connects  =     0.525510
Fanout Count     =     1764
Average Fanout   =     1.536585
Avg Tech Box Size =     4.889968
Tech Box Size Stddev =    0.010696
Power            =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals     =      773
Real boxes       =      552
Real connections =     1389
Real LSTs        =     2162
Real ICells/box  =     8.211957
Real LSTs/box    =     3.916667
Real nets/box    =     1.400362

```

```

Cell            Total
Each            Cell

```

```

Type Cnt  Boxname          Power Level  Function  Int  Ext  Power  Int  Ext  Power

```


7	cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
4	cs_ao12n03c	03c	>	AOI	4	0	0.000	16	0	0.000
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180	BRKPT	>		BRKPT	0	0	0.000	0	0	0.000
195	IOPAD	>		IOPAD	0	0	0.000	0	0	0.000
164	cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
24	cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
2	cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
3	cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
2	cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000
3	cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000
2	cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1	cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89	cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
28	cs_invvn07c	07c	>	NOT	2	0	0.000	56	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000

18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of		
Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of		
Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	386	350* plus *****
2	203	200* plus ***
3	37	*****
4	16	*****

The Histogram Of Fanout vs. Net

of
Fanout Nets

```

-----
 1  945  900* plus *****
 2  101  100* plus *
 3   41  *****
 4   16  *****
 5    8  *****
 6   11  *****
 7    2  **
 8    4  ****
13    3  ***
14   16  *****
15    1  *

```

[End of measure]

[measure]: Execution time was 0.6 seconds.

> measure

The model <IDCDSUC> has:

```

Primary Inputs    =      122
Primary Outputs  =       73
Primary BIDs     =        0
Signals          =     1148
Gate Count       =      927
Connections      =     1764
Master REG Bits  =       83
Slave REG Bits   =       83
Internal Area    =     4533
External Area    =        0
Gates/Connects  =     0.525510
Fanout Count     =     1764
Average Fanout   =     1.536585
Avg Tech Box Size =     4.889968
Tech Box Size Stddev =     0.010696
Power            =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals      =      773
Real boxes        =      552
Real connections  =     1389
Real LSTs         =     2162
Real ICells/box   =     8.211957
Real LSTs/box     =     3.916667
Real nets/box     =     1.400362

```

Cell Total
Each Cell

Type	Cnt	Boxname	Power Level	Function	Int	Ext	Power	Int	Ext	Power
7	cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
4	cs_ao12n03c	03c	>	AOI	4	0	0.000	16	0	0.000
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000

1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180	BRKPT		>	BRKPT	0	0	0.000	0	0	0.000
195	IOPAD		>	IOPAD	0	0	0.000	0	0	0.000
164	cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
24	cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
2	cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
3	cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
2	cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000
3	cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000
2	cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1	cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89	cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
28	cs_invvn07c	07c	>	NOT	2	0	0.000	56	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000

1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of		
Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of		
Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	386	350* plus *****
2	203	200* plus ***
3	37	*****
4	16	*****

The Histogram Of Fanout vs. Net

of

Fanout Nets

```

-----
1    945    900* plus *****
2    101    100* plus *
3     41    *****
4     16    *****
5      8    *****
6     11    *****
7      2    **
8      4    ****
13     3    ***
14    16    *****
15     1    *

```

[End of measure]

[measure]: Execution time was 0.6 seconds.

> quick tcte(SCORE(ALL),NO_VIOLATIONS)

[

>>]: [quick]:(tcte(SCORE(ALL),NO_VIOLATIONS));

-1993.41 Avg: -212.60

[BD-500000]: tcte CMVC version 1.6 compiled on Apr 13 1999 at 18:26:19

-1993.41 Avg: -212.60

maximum area for proto box IDCDSUC is 4533

[quick]: Number of boxes to process is 927.

[quick]: Number of boxes processed is 0.

-1993.41 Avg: -208.85

[BD-502200]: Combined 4 gates.

[tcte]: Execution time was 0.2 seconds.

> measure

The model <IDCDSUC> has:

```

Primary Inputs    =    122
Primary Outputs   =     73
Primary BIDs      =      0
Signals           =   1144
Gate Count        =     923
Connections       =   1760
Master REG Bits   =     83
Slave REG Bits    =     83
Internal Area     =   4525
External Area     =      0
Gates/Connects   =   0.524432
Fanout Count      =   1760
Average Fanout    =   1.538462
Avg Tech Box Size =   4.902492
Tech Box Size Stddev = 0.010763
Power             =   0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals      =     769
Real boxes        =     548
Real connections   =   1385
Real LSTs         =   2154
Real ICells/box   =   8.257299

```

Real LSTs/box = 3.930657
Real nets/box = 1.403285
Cell Total
Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7	cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000	
4	cs_ao12n03c	03c	>	AOI	4	0	0.000	16	0	0.000	
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000	
1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000	
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
164	cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000	
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000	
24	cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000	
2	cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000	
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000	
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000	
3	cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000	
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000	
1	cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000	
2	cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000	
3	cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000	
2	cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000	
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000	
1	cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000	
1	cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000	
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000	
1	cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000	
1	cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000	
1	cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000	
1	cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000	
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000	
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000	
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000	
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000	
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000	
1	cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000	
1	cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000	
89	cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000	
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000	
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000	
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000	
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000	
24	cs_invvn07c	07c	>	NOT	2	0	0.000	48	0	0.000	
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000	
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000	
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000	
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000	
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000	
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000	
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000	
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000	
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000	
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000	

2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	55 50* plus *****
2	1 *
3	8 *****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	20 *****
3	1 *
4	5 *****
5	3 ***
6	10 *****
7	3 ***
9	1 *
10	6 *****
12	1 *
13	2 **
14	4 *****
15	10 *****
16	3 ***
17	14 *****

The Histogram Of Fanin vs. Box

# of Fanin	Ops
---------------	-----


```

-----
1  382  350* plus *****
2  203  200* plus ***
3   37  *****
4   16  *****

```

The Histogram Of Fanout vs. Net

of
Fanout Nets

```

-----
1  943  900* plus *****
2  100  100* plus
3   41  *****
4   16  *****
5    7  *****
6   11  *****
7    2  **
8    4  ****
13   3  ***
14  16  *****
20   1  *

```

[End of measure]

[measure]: Execution time was 0.6 seconds.

> tc_parm CAP_LIM(200)

> tc_parm CAP_LIM(100)

> fanmatch ESTIMATED, SORT, ONE_LEVEL

[>>]: ltorbox(dfanmatch(ESTIMATED, SORT, ONE_LEVEL));

[BD-500000]: fanmatch CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32

setting ESTIMATED option.

setting SORT option.

setting ONE_LEVEL option.

-1993.41 Avg: -208.85

[BD-500300]: 137 pins on 66 gates swapped.

-1978.06 Avg: -206.71

[fanmatch]: Execution time was 1.4 seconds.

> measure

The model <IDCDSUC> has:

```

Primary Inputs   =      122
Primary Outputs  =       73
Primary BIDs     =        0
Signals          =     1144
Gate Count       =      923
Connections      =     1760
Master REG Bits  =       83
Slave REG Bits   =       83
Internal Area    =     4525
External Area    =        0
Gates/Connects  =     0.524432
Fanout Count     =     1760
Average Fanout   =     1.538462

```

Avg Tech Box Size = 4.902492
 Tech Box Size Stddev = 0.010763
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 769
 Real boxes = 548
 Real connections = 1385
 Real LSTs = 2154
 Real ICells/box = 8.257299
 Real LSTs/box = 3.930657
 Real nets/box = 1.403285

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
4		cs_ao12n03c	03c	>	AOI	4	0	0.000	16	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1		cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180		BRKPT	>		BRKPT	0	0	0.000	0	0	0.000
195		IOPAD	>		IOPAD	0	0	0.000	0	0	0.000
164		cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000
1		cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
24		cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
2		cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000
5		cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
1		cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
3		cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
1		cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1		cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
2		cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000
3		cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000
2		cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
1		cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1		cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000
6		cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1		cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000
1		cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
1		cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
10		cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1		cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1		cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1		cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1		cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1		cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89		cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4		cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6		cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22		cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7		cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
24		cs_invvn07c	07c	>	NOT	2	0	0.000	48	0	0.000

4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*

13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	382	350* plus *****
2	203	200* plus ***
3	37	*****
4	16	*****

The Histogram Of Fanout vs. Net

# of		
Fanout	Nets	
1	943	900* plus *****
2	100	100* plus *****
3	41	*****
4	16	*****
5	7	*****
6	11	*****
7	2	**
8	4	****
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.7 seconds.

> treematch ESTIMATED,TWO_LEVEL,NO_VIOLATIONS

[

>>]: ltorbox(dtreematch(ESTIMATED,TWO_LEVEL,NO_VIOLATIONS));

[BD-500000]: treematch CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32

setting ESTIMATED option.

setting TWO_LEVEL option.

setting NO_VIOLATIONS option.

-1978.06 Avg: -206.71

[BD-500301]: 5 pins on 2 gates swapped.

-1978.02 Avg: -210.98

[treematch]: Execution time was 0.2 seconds.

> measure

The model <IDCDSUC> has:

Primary Inputs	=	122
Primary Outputs	=	73
Primary BIDs	=	0
Signals	=	1144
Gate Count	=	923

Connections = 1760
 Master REG Bits = 83
 Slave REG Bits = 83
 Internal Area = 4525
 External Area = 0
 Gates/Connects = 0.524432
 Fanout Count = 1760
 Average Fanout = 1.538462
 Avg Tech Box Size = 4.902492
 Tech Box Size Stddev = 0.010763
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 769
 Real boxes = 548
 Real connections = 1385
 Real LSTs = 2154
 Real ICells/box = 8.257299
 Real LSTs/box = 3.930657
 Real nets/box = 1.403285

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7	cs_ao22n03c	03c >	AOI	6	0	0.000	42	0	0.000		
4	cs_ao12n03c	03c >	AOI	4	0	0.000	16	0	0.000		
1	cs_ao22n10c	10c >	AOI	18	0	0.000	18	0	0.000		
1	cs_ao12n04c	04c >	AOI	4	0	0.000	4	0	0.000		
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
164	cs_nnd2n02c	02c >	NAND	3	0	0.000	492	0	0.000		
1	cs_nnd2n10c	10c >	NAND	8	0	0.000	8	0	0.000		
24	cs_nnd3n02c	02c >	NAND	4	0	0.000	96	0	0.000		
2	cs_nnd2n05c	05c >	NAND	4	0	0.000	8	0	0.000		
5	cs_nnd4n03c	03c >	NAND	5	0	0.000	25	0	0.000		
1	cs_nnd2n13c	13c >	NAND	15	0	0.000	15	0	0.000		
3	cs_nnd2n04c	04c >	NAND	3	0	0.000	9	0	0.000		
1	cs_nnd3n07c	07c >	NAND	6	0	0.000	6	0	0.000		
1	cs_nnd2n14e	14e >	NAND	19	0	0.000	19	0	0.000		
2	cs_nnd2n03c	03c >	NAND	3	0	0.000	6	0	0.000		
3	cs_nnd2n07c	07c >	NAND	4	0	0.000	12	0	0.000		
2	cs_nnd2n11c	11c >	NAND	11	0	0.000	22	0	0.000		
1	cs_nnd2n14b	14b >	NAND	20	0	0.000	20	0	0.000		
1	cs_nnd3n12c	12c >	NAND	22	0	0.000	22	0	0.000		
1	cs_nnd4n06c	06c >	NAND	8	0	0.000	8	0	0.000		
6	cs_nnd2n14c	14c >	NAND	19	0	0.000	114	0	0.000		
1	cs_nnd4n10c	10c >	NAND	20	0	0.000	20	0	0.000		
1	cs_nnd2n06c	06c >	NAND	4	0	0.000	4	0	0.000		
1	cs_nnd3n05c	05c >	NAND	6	0	0.000	6	0	0.000		
1	cs_nnd2n12c	12c >	NAND	12	0	0.000	12	0	0.000		
1	cs_nnd3n10c	10c >	NAND	12	0	0.000	12	0	0.000		
10	cs_nor2n02c	02c >	NOR	3	0	0.000	30	0	0.000		
1	cs_nor3n03c	03c >	NOR	4	0	0.000	4	0	0.000		
1	cs_nor2n12c	12c >	NOR	12	0	0.000	12	0	0.000		
1	cs_nor2n04c	04c >	NOR	3	0	0.000	3	0	0.000		
1	cs_nor3n10c	10c >	NOR	12	0	0.000	12	0	0.000		

1	cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89	cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
24	cs_invvn07c	07c	>	NOT	2	0	0.000	48	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_ao21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_ao22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	-A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1	>	SEQUENTIAL	80	0	0.000	480	0	0.000	
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register	
0	7	*****
2	20	*****
3	1	*

4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

	# of Fanin	Ops
1	382	350* plus *****
2	203	200* plus ***
3	37	*****
4	16	*****

The Histogram Of Fanout vs. Net

	# of Fanout	Nets
1	943	900* plus *****
2	100	100* plus
3	41	*****
4	16	*****
5	7	*****
6	11	*****
7	2	**
8	4	****
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.7 seconds.

> pad_pos

pad_pos: Found 152 valid buffers or inverters.

[BD-500718]: pad_pos too many buffers and/or inverters 152, may slow down optimizations.

[BD-500705]: (W) No noninverting buffers in technology, primary output buffer insertion will not be done.

> nextbox synexpand(XPANDVIEW)

[

>>]: nextbox(synexpand(XPANDVIEW));

[synexpand]: Compiled on Mar 10 1999 at 05:19:51

[

>>]: nextbox(SASname(RESTORE));

[syndasname]: Restored 0 BRKPT net names

[syndasname]: Restored 189 REG and SEQUENTIAL output net names

[synsasname]: Execution time was 0.0 seconds.

[restore_pin_keywords]: deleted 0 nets and pins

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1146 signals, 923 usage boxes and 1760 connections.

[

>>]: nextbox(SASName(PROTECT));

[synsasname]: Protected 180 BRKPT net names

[synsasname]: Protected 189 REG and SEQUENTIAL output net names

[synsasname]: Execution time was 0.0 seconds.

[synexpand]: expanded 0 boxes

> measure

The model <IDCDSUC> has:

Primary Inputs = 122
Primary Outputs = 73
Primary BIDs = 0
Signals = 1146
Gate Count = 923
Connections = 1760
Master REG Bits = 83
Slave REG Bits = 83
Internal Area = 4525
External Area = 0
Gates/Connects = 0.524432
Fanout Count = 1760
Average Fanout = 1.535777
Avg Tech Box Size = 4.902492
Tech Box Size Stddev = 0.010763
Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 771
Real boxes = 548
Real connections = 1385
Real LSTs = 2156
Real ICells/box = 8.257299
Real LSTs/box = 3.934307
Real nets/box = 1.406934

Cell Total
Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7	cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000	
4	cs_ao12n03c	03c	>	AOI	4	0	0.000	16	0	0.000	
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000	
1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000	
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
164	cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000	
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000	
24	cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000	
2	cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000	
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000	
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000	
3	cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000	

1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
2	cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000
3	cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000
2	cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1	cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89	cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
24	cs_invvn07c	07c	>	NOT	2	0	0.000	48	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

of

Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of Fanin	Ops	
1	382	350* plus *****
2	203	200* plus ***
3	37	*****
4	16	*****

The Histogram Of Fanout vs. Net

# of Fanout	Nets	
0	2	**
1	943	900* plus *****
2	100	100* plus *****
3	41	*****
4	16	*****
5	7	*****
6	11	*****
7	2	**

----> BOX714/IN	R C3+R	2977	-1978	3847	1011	1	IOPAD	IOPAD
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2977	-1978	3847	1011	1	cs_invvn	01c NOT
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1115	-1978	55	139	4	cs_invvn	01c NOT
1862 N675								
---->{a} C2738/y	F C3+R	1115	-1978	55	139	4	cs_nnd2n	14b NAND
0 N675								
----> C2738/b	R C3+R	1084	-1978	90	159	3	cs_nnd2n	14b NAND
31 N1692								
---->{b} C2725rwr/y	R C3+R	1084	-1978	90	159	3	cs_nnd2n	14c NAND
0 N1692								
----> C2725rwr/a	F C3+R	1035	-1978	93	168	2	cs_nnd2n	14c NAND
49 N1479								
---->{c} C2721rwr/y	F C3+R	1035	-1978	93	168	2	cs_nnd3n	12c NAND
0 N1479								
----> C2721rwr/c	R C3+R	975	-1978	179	95	2	cs_nnd3n	12c NAND
59 N1497								
---->{d} C2709rwr/y	R C3+R	975	-1978	179	95	2	cs_nor3n	10c NOR
0 N1497								
----> C2709rwr/a	F C3+R	899	-1978	50	53	1	cs_nor3n	10c NOR
76 N1986								
---->{e} C2677rwr_0/y	F C3+R	899	-1978	50	53	1	cs_nnd2n	12c NAND
0 N1986								
----> C2677rwr_0/b	R C3+R	872	-1978	74	88	2	cs_nnd2n	12c NAND
27 N1094								
---->{f} C2909/y	R C3+R	872	-1978	74	88	2	cs_nnd2n	14c NAND
0 N1094								
----> C2909/a	F C3+R	835	-1978	80	108	1	cs_nnd2n	14c NAND
37 dcd_mcr41_blk&0								
----> BOX615/OUT	F C3+R	835	-1978	80	108	1	IOPAD	IOPAD
0 dcd_mcr41_blk&0								
----> BOX615/IN	F C3+R	835	-1978	80	108	1	IOPAD	IOPAD
dcd_mcr41_blk								
----> dcd_mcr41_blk	F C3+R	835	-1978	80	108	1	PI	0
dcd_mcr41_blk								

2 dcd_succ_last_t1	F C3+R	2574	-1575	2362	1011	1	PO	0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	F C3+R	2574	-1575	2362	1011	1	IOPAD	IOPAD
0 dcd_succ_last_t1								
----> BOX714/IN	F C3+R	2574	-1575	2362	1011	1	IOPAD	IOPAD
0 dcd_succ_last_t1&0								
----> C167/y	F C3+R	2574	-1575	2362	1011	1	cs_invvn	01c NOT
0 dcd_succ_last_t1&0								
----> C167/a	R C3+R	1138	-1575	92	139	4	cs_invvn	01c NOT
1436 N675								
---->{a} C2738/y	R C3+R	1138	-1575	92	139	4	cs_nnd2n	14b NAND
0 N675								
----> C2738/a	F C3+R	1094	-1575	65	108	1	cs_nnd2n	14b NAND
44 last_cycle								
---->{b} C2487/y	F C3+R	1094	-1575	65	108	1	cs_nnd2n	14e NAND
0 last_cycle								

```

----> C2487/b          R C3+R   1057  -1575   69  124  2 cs_nnd2n  14e NAND
37 N1587
----> C1952/y          R C3+R   1057  -1575   69  124  2 cs_invvn  14b NOT
0 N1587
----> C1952/a          F C3+R   1016  -1575   80  139  2 cs_invvn  14b NOT
41 num_dcd_cyl&0(1)
----> BOX679/OUT        F C3+R   1016  -1575   80  139  2 IOPAD      IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN        F C3+R   1016  -1575   80  139  2 IOPAD      IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)    F C3+R   1016  -1575   80  139  2 PI          0
num_dcd_cyl(1)

```

```

--
    3 local_milli_t2.reg_n.lat_0/a      F C3+R   2818  -1499   48   31  1 cl_invvn  07c SRL
41 N2054
Setup local_milli_t2.reg_n.lat_0/c1      F C3-     160          60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
----> C3011/y          F C3+R   2818  -1499   48   31  1 cs_invvn  07c NOT    0
N2054
----> C3011/a          R C3+R   2781  -1499  466   92  3 cs_invvn  07c NOT
37 N73
----> {a} C2794/y       R C3+R   2781  -1499  466   92  3 cs_ao12n  03c AOI
0 N73
----> C2794/a2         F C3+R   2540  -1499  115   18  1 cs_ao12n  03c AOI
241 N1866
----> {b} C2555/y       F C3+R   2540  -1499  115   18  1 cs_ao12n  03c AOI
0 N1866
----> C2555/b          R C3+R   2431  -1499 3912 1044  3 cs_ao12n  03c AOI
109 iu_reset_op_c_t1&0
----> {c} C2393/y       R C3+R   2431  -1499 3912 1044  3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   474   -1499   78  137  3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfozell_6/y      F C3+R   474   -1499   78  137  3 cs_invvn  09c NOT    0
gbfonet_6
----> gbfozell_6/a      R C3+R   410   -1499  217   43  1 cs_invvn  09c NOT
64 N2031
----> {d} C2162/y       R C3+R   410   -1499  217   43  1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b          F C3+R   303   -1499   57   49  3 cs_nnd3n  02c NAND
107 exc_cond_q
----> exc_cond.reg_n.lat_0/2_out_n      F C3+R   303   -1499   57   49  3 cl_invvn  07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2            R C3+     160    N/C   60  239 14 cl_invvn  07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2          R C3+     160    N/C   60  239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

```

--
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

```

```

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > quick texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WO...
[
>>]: [quick]:(
texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST,SIMILAR,VIEW(TRUE_BASE_AU
TOGEN),NO_VIOLATIONS) );
-1978.02 Avg: -210.98
[BD-500000]: texpand CMVC version 1.13.1.9 compiled on Apr 13 1999 at 18:26:58
[expand]: setting SCORE option to ALL.
[expand]: setting PUSH option.
[expand]: setting SORT_PINS option.
[expand]: setting NO_PRIMITIVES option.
[expand]: setting WORST option.
[expand]: setting SIMILAR option.
[expand]: explicit VIEWS used.
[expand]: setting NO_VIOLATIONS option.
-1978.02 Avg: -210.98
[expand]: TRUE view TRUE_BASE_AUTOGEN was found.
maximum area for proto box IDCDSUC is 4525
Rel 0.5 Compiled on Apr 13 1999 at 18:30:09.
-1978.02 Avg: -210.98
Selected 401 critical boxes of 923 total.
[quick]: Number of boxes to process is 401.
[quick]: Number of boxes processed is 0.
[pattern_util]: CMVC version 1.19 compiled on Apr 1 1999 at 05:05:05.
[BD-80000]: pattern CMVC version 1.21.1.1 compiled on Apr 8 1999 at 05:25:52
-1978.02 Avg: -206.57
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[expand]: Execution time was 0.6 seconds.
[BD-502600]: 11 gates checked and 1 expanded.
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > quick {texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,W...
[
>>]: [quick]:( texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST
,VIEW(TRUE_BASE_AUTOGEN) NO_VIOLATIONS) );
-1978.02 Avg: -206.57
[expand]: setting SCORE option to ALL.
[expand]: setting PUSH option.
[expand]: setting SORT_PINS option.
[expand]: setting NO_PRIMITIVES option.
[expand]: setting WORST option.
[expand]: explicit VIEWS used.
[expand]: setting NO_VIOLATIONS option.

```

```

-1978.02 Avg: -206.57
[txpand]: TRULE view TRULE_BASE_AUTOGEN was found.
maximum area for proto box IDCDSUC is 4525
-1978.02 Avg: -206.57
Selected 400 critical boxes of 922 total.
[quick]: Number of boxes to process is 400.
[quick]: Number of boxes processed is 0.
-1978.02 Avg: -206.57
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[txpand]: Execution time was 0.4 seconds.
[BD-502600]: 10 gates checked and 0 expanded.
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > quick {txpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,W...
[
>>]: [quick]:(
txpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST,SIMILAR,VIEW(TRULE_AND_OR
_AUTOGEN) ,NO_VIOLATIONS) );
-1978.02 Avg: -206.57
[txpand]: setting SCORE option to ALL.
[txpand]: setting PUSH option.
[txpand]: setting SORT_PINS option.
[txpand]: setting NO_PRIMITIVES option.
[txpand]: setting WORST option.
[txpand]: setting SIMILAR option.
[txpand]: explicit VIEWS used.
[txpand]: setting NO_VIOLATIONS option.
-1978.02 Avg: -206.57
[txpand]: TRULE view TRULE_AND_OR_AUTOGEN was found.
maximum area for proto box IDCDSUC is 4525
-1978.02 Avg: -206.57
Selected 400 critical boxes of 922 total.
[quick]: Number of boxes to process is 400.
[quick]: Number of boxes processed is 0.
-1978.02 Avg: -206.57
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[txpand]: Execution time was 0.0 seconds.
[BD-502600]: 0 gates checked and 0 expanded.
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====

```

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
> quick {texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,W...

[

>>]: [quick]:(texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST
,VIEW(TRUE_AND_OR_AUTOGEN) ,NO_VIOLATIONS));

-1978.02 Avg: -206.57

[texpand]: setting SCORE option to ALL.

[texpand]: setting PUSH option.

[texpand]: setting SORT_PINS option.

[texpand]: setting NO_PRIMITIVES option.

[texpand]: setting WORST option.

[texpand]: explicit VIEWs used.

[texpand]: setting NO_VIOLATIONS option.

-1978.02 Avg: -206.57

[texpand]: TRUE view TRUE_AND_OR_AUTOGEN was found.

maximum area for proto box IDCDSUC is 4525

-1978.02 Avg: -206.57

Selected 400 critical boxes of 922 total.

[quick]: Number of boxes to process is 400.

[quick]: Number of boxes processed is 0.

-1978.02 Avg: -206.57

Pattern hint flag is inactive

[cleanup]: 0 boxes disconnected

[texpand]: Execution time was 0.0 seconds.

[BD-502600]: 0 gates checked and 0 expanded.

> get_default_delay_synlimit

> tc_parm OFFSET(0)

> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000

[tc_parm]: =====

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000

> quick tmerge(SCORE(ALL),ORD2,SORT_PINS,NO_VIOLATIONS)

[

>>]: [quick]:(tmerge(SCORE(ALL),ORD2,SORT_PINS,NO_VIOLATIONS));

-1978.02 Avg: -206.57

[tmerge]: Compiled on Mar 31 1999 at 11:35:37.

[tmerge]: setting SCORE option to ALL.

[tmerge]: setting ORD2 option.

[tmerge]: setting SORT_PINS option.

[tmerge]: setting NO_VIOLATIONS option.

-1978.02 Avg: -206.57

maximum area for proto box IDCDSUC is 4525

-1978.02 Avg: -206.57

Selected 400 critical boxes of 922 total.

[quick]: Number of boxes to process is 400.

[quick]: Number of boxes processed is 0.

-1978.02 Avg: -206.57

[tmerge]: applied 0 times

> write_end_point_report -points 3 -paths 1

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.


```

--
3 iu_reset_op_c_t1          R C3+R  2431 -1432  3912 1011 1 PO          0
iu_reset_op_c_t1
RAT                          999          0
----> BOX716/OUT            R C3+R  2431 -1432  3912 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN            R C3+R  2431 -1432  3912 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R  2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a             F C3+R  474 -1432   78 137 3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfozell_6/y        F C3+R  474 -1432   78 137 3 cs_invrn  09c NOT      0
gbfonet_6
----> gbfozell_6/a        R C3+R  410 -1432  217  43 1 cs_invrn  09c NOT
64 N2031
---->{b} C2162/y          R C3+R  410 -1432  217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b             F C3+R  303 -1432   57  49 3 cs_nnd3n  02c NAND
107 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n F C3+R  303 -1432   57  49 3 cl_invrn  07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2 R C3+   160   N/C   60 239 14 cl_invrn  07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2 R C3+   160   N/C   60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4

```

> measure

The model <IDCDSUC> has:

```

Primary Inputs   =      122
Primary Outputs  =       73
Primary BIDs     =        0
Signals          =     1145
Gate Count       =      922
Connections      =     1759
Master REG Bits  =       83
Slave REG Bits   =       83
Internal Area    =     4525
External Area    =        0
Gates/Connects  =     0.524161
Fanout Count     =     1759
Average Fanout   =     1.536245
Avg Tech Box Size =     4.907809
Tech Box Size Stddev =     0.010780
Power            =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals     =      770
Real boxes       =      547
Real connections  =     1384
Real LSTs        =     2154
Real ICells/box  =     8.272395

```

Real LSTs/box = 3.937843
Real nets/box = 1.407678
Cell Total
Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
3		cs_ao12n03c	03c	>	AOI	4	0	0.000	12	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1		cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180		BRKPT	>	BRKPT	0	0	0.000	0	0	0.000	
195		IOPAD	>	IOPAD	0	0	0.000	0	0	0.000	
164		cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000
1		cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
24		cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
2		cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000
5		cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
1		cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
3		cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
1		cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1		cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
2		cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000
3		cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000
2		cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
1		cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1		cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000
6		cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1		cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000
1		cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
1		cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
2		cs_nnd2f03c	03c	>	NAND	4	0	0.000	8	0	0.000
10		cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1		cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1		cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1		cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1		cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1		cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89		cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4		cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6		cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22		cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7		cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
21		cs_invvn07c	07c	>	NOT	2	0	0.000	42	0	0.000
4		cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11		cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12		cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5		cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1		cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4		cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6		cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1		cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3		cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000

1	cs_inwn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_inwn16c	16c	>	NOT	14	0	0.000	28	0	0.000
1	cs_inwn03c	03c	>	NOT	2	0	0.000	2	0	0.000
2	cs_0a21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_0a22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_inwn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_inwn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_0a21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	55 50* plus *****
2	1 *
3	8 *****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	20 *****
3	1 *
4	5 *****
5	3 ***
6	10 *****
7	3 ***
9	1 *
10	6 *****
12	1 *
13	2 **
14	4 ****
15	10 *****
16	3 ***
17	14 *****

The Histogram Of Fanin vs. Box

	# of Fanin	Ops
1	380	350* plus *****
2	205	200* plus *****
3	36	*****
4	16	*****

The Histogram Of Fanout vs. Net

	# of Fanout	Nets
0	2	**
1	942	900* plus *****
2	100	100* plus
3	41	*****
4	16	*****
5	7	*****
6	11	*****
7	2	**
8	4	****
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds.

> critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...

critical(

repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED),faninv(LIMITED));

-1978.02 Avg: -206.57

maximum area for proto box IDCDSUC is 4525

repower: setting SCORE option to ALL.

repower: setting INC mode.

repower: setting NO_VIOLATIONS option.

[BD-500000]: clone CMVC version 1.20 compiled on Apr 13 1999 at 18:21:21

setting SCORE option to ALL.

setting ACTUAL option.

setting RE_POWER option.

setting INC mode.

setting NO_VIOLATIONS option.

[BD-500000]: fantom CMVC version 1.54 compiled on Apr 13 1999 at 18:23:22

[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.

-1978.02 Avg: -206.57

ArrayNum: 9 ArrayMax: 922

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.1 seconds.

[BD-500100]: 0 parallel copies of gates were made.

[clone]: Execution time was 0.3 seconds.

[BD-500700]: Added 0 buffers.

[fantom]: Execution time was 0.0 seconds.

[BD-500701]: Added 0 inverters.

```

[faninv]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 36 times and applied 0 of them.
    > nextbox synexpand(XPANDVIEW)
[
>>]: nextbox( synexpand(XPANDVIEW) );
[restore_pin_keywords]: restored 0 keywords
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[restore_pin_keywords]: deleted 0 nets and pins
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1145 signals, 922 usage boxes and 1759 connections.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
    > measure

```

The model <IDCDSUC> has:

```

Primary Inputs    =      122
Primary Outputs   =       73
Primary BIDs      =        0
Signals           =     1145
Gate Count        =      922
Connections       =     1759
Master REG Bits   =       83
Slave REG Bits    =       83
Internal Area     =     4525
External Area     =        0
Gates/Connects   =     0.524161
Fanout Count      =     1759
Average Fanout    =     1.536245
Avg Tech Box Size =     4.907809
Tech Box Size Stddev = 0.010780
Power             =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals      =      770
Real boxes        =      547
Real connections  =     1384
Real LSTs         =     2154
Real ICells/box   =     8.272395
Real LSTs/box     =     3.937843
Real nets/box     =     1.407678

```

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
3		cs_ao12n03c	03c	>	AOI	4	0	0.000	12	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000

1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180	BRKPT		>	BRKPT	0	0	0.000	0	0	0.000
195	IOPAD		>	IOPAD	0	0	0.000	0	0	0.000
164	cs_nnd2n02c	02c	>	NAND	3	0	0.000	492	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
24	cs_nnd3n02c	02c	>	NAND	4	0	0.000	96	0	0.000
2	cs_nnd2n05c	05c	>	NAND	4	0	0.000	8	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
3	cs_nnd2n04c	04c	>	NAND	3	0	0.000	9	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
2	cs_nnd2n03c	03c	>	NAND	3	0	0.000	6	0	0.000
3	cs_nnd2n07c	07c	>	NAND	4	0	0.000	12	0	0.000
2	cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
1	cs_nnd4n06c	06c	>	NAND	8	0	0.000	8	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd4n10c	10c	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd2n06c	06c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n05c	05c	>	NAND	6	0	0.000	6	0	0.000
1	cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
2	cs_nnd2f03c	03c	>	NAND	4	0	0.000	8	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10c	10c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n09c	09c	>	NOR	7	0	0.000	7	0	0.000
89	cs_invvn01c	01c	>	NOT	2	0	0.000	178	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
7	cs_invvn09c	09c	>	NOT	4	0	0.000	28	0	0.000
21	cs_invvn07c	07c	>	NOT	2	0	0.000	42	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
11	cs_invvn06c	06c	>	NOT	2	0	0.000	22	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
5	cs_invvn13c	13c	>	NOT	8	0	0.000	40	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
1	cs_invvn03c	03c	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000

2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of		
Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of		
Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
13	2	**
14	4	****
15	10	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	380	350* plus *****
2	205	200* plus *****
3	36	*****
4	16	*****

The Histogram Of Fanout vs. Net

# of		
Fanout	Nets	
0	2	**
1	942	900* plus *****
2	100	100* plus
3	41	*****
4	16	*****
5	7	*****
6	11	*****
7	2	**
8	4	****
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds.
 > write_end_point_report -points 3 -paths 1
 [ET-0018]: >Begin...New EndPoint Report
 for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 21:59:18 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj
--								
1 dcd_succ_last_t1	R C3+R	2977	-1978	3847	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	R C3+R	2977	-1978	3847	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2977	-1978	3847	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2977	-1978	3847	1011	1 cs_invn	01c NOT	
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1115	-1978	55	139	4 cs_invn	01c NOT	
1862 N675								
---->{a} C2738/y	F C3+R	1115	-1978	55	139	4 cs_nnd2n	14b NAND	
0 N675								
----> C2738/b	R C3+R	1084	-1978	90	159	3 cs_nnd2n	14b NAND	
31 N1692								
---->{b} C2725rwr/y	R C3+R	1084	-1978	90	159	3 cs_nnd2n	14c NAND	
0 N1692								
----> C2725rwr/a	F C3+R	1035	-1978	93	168	2 cs_nnd2n	14c NAND	
49 N1479								
---->{c} C2721rwr/y	F C3+R	1035	-1978	93	168	2 cs_nnd3n	12c NAND	
0 N1479								
----> C2721rwr/c	R C3+R	975	-1978	179	95	2 cs_nnd3n	12c NAND	
59 N1497								
---->{d} C2709rwr/y	R C3+R	975	-1978	179	95	2 cs_nor3n	10c NOR	
0 N1497								
----> C2709rwr/a	F C3+R	899	-1978	50	53	1 cs_nor3n	10c NOR	
76 N1986								
---->{e} C2677rwr_0/y	F C3+R	899	-1978	50	53	1 cs_nnd2n	12c NAND	
0 N1986								
----> C2677rwr_0/b	R C3+R	872	-1978	74	88	2 cs_nnd2n	12c NAND	
27 N1094								
---->{f} C2909/y	R C3+R	872	-1978	74	88	2 cs_nnd2n	14c NAND	
0 N1094								
----> C2909/a	F C3+R	835	-1978	80	108	1 cs_nnd2n	14c NAND	
37 dcd_mcr41_blk&0								
----> BOX615/OUT	F C3+R	835	-1978	80	108	1 IOPAD	IOPAD	
0 dcd_mcr41_blk&0								
----> BOX615/IN	F C3+R	835	-1978	80	108	1 IOPAD	IOPAD	0
dcd_mcr41_blk								
----> dcd_mcr41_blk	F C3+R	835	-1978	80	108	1 PI		0
dcd_mcr41_blk								
--								
2 dcd_succ_last_t1	F C3+R	2574	-1575	2362	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	F C3+R	2574	-1575	2362	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1								
----> BOX714/IN	F C3+R	2574	-1575	2362	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1&0								

```

----> C167/y          F C3+R  2574 -1575  2362 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0
----> C167/a          R C3+R  1138 -1575   92 139 4 cs_invvn 01c NOT
1436 N675
----> {a} C2738/y     R C3+R  1138 -1575   92 139 4 cs_nnd2n 14b NAND
0 N675
----> C2738/a        F C3+R  1094 -1575   65 108 1 cs_nnd2n 14b NAND
44 last_cycle
----> {b} C2487/y     F C3+R  1094 -1575   65 108 1 cs_nnd2n 14e NAND
0 last_cycle
----> C2487/b        R C3+R  1057 -1575   69 124 2 cs_nnd2n 14e NAND
37 N1587
----> C1952/y        R C3+R  1057 -1575   69 124 2 cs_invvn 14b NOT
0 N1587
----> C1952/a        F C3+R  1016 -1575   80 139 2 cs_invvn 14b NOT
41 num_dcd_cyl&0(1)
----> BOX679/OUT      F C3+R  1016 -1575   80 139 2 IOPAD    IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN      F C3+R  1016 -1575   80 139 2 IOPAD    IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1) F C3+R  1016 -1575   80 139 2 PI          0
num_dcd_cyl(1)
-----
--
3 iu_reset_op_c_t1    R C3+R  2431 -1432  3912 1011 1 PO          0
iu_reset_op_c_t1
RAT 999 0
----> BOX716/OUT      R C3+R  2431 -1432  3912 1011 1 IOPAD    IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN      R C3+R  2431 -1432  3912 1044 3 IOPAD    IOPAD
0 iu_reset_op_c_t1&0
----> {a} C2393/y     R C3+R  2431 -1432  3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a        F C3+R  474 -1432   78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6
----> gbfcoll_6/y     F C3+R  474 -1432   78 137 3 cs_invvn 09c NOT    0
gbfonet_6
----> gbfcoll_6/a     R C3+R  410 -1432  217 43 1 cs_invvn 09c NOT
64 N2031
----> {b} C2162/y     R C3+R  410 -1432  217 43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b        F C3+R  303 -1432   57 49 3 cs_nnd3n 02c NAND
107 exc_cond_q
----> exc_cond.reg_n.lat_0/l2_out_n F C3+R  303 -1432   57 49 3 cl_invvn 07d SRL
0 exc_cond_q
----> exc_cond.reg_n.lat_0/c2 R C3+  160 N/C   60 239 14 cl_invvn 07d SRL
143 slow_mode.c2_4
----> slow_mode.clockblock_3/c2 R C3+  160 N/C   60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4
-----
--
> echo {Finished initial power up}
Finished initial power up
> fanmatch ACTUAL,ONE_LEVEL,NO_VIOLATIONS
[

```

```

>>]: ltorbox( dfanmatch(ACTUAL,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1978.02 Avg: -206.57
[BD-500300]: 70 pins on 32 gates swapped.
-1977.33 Avg: -205.40
[fanmatch]: Execution time was 3.6 seconds.
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1) ...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > reset_critical_slack_limit
-1977.33 Avg: -205.40
resetting the current slack to -1977.3279
    > repower_paths FUZZY(0.02)
initial slack is -1977
after repower paths slack is -1977
    > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS) , repowe...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS) ,
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1977.33 Avg: -200.64
maximum-area for proto box IDCDSUC is 4595
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1977.33 Avg: -200.64
ArrayNum: 9 ArrayMax: 922
-1967.14 Avg: -200.49
ArrayNum: 6 ArrayMax: 922
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 0.4 seconds.
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 0.4 seconds.
[BD-502000]: Called transforms 24 times and applied 1 of them.
    > compare_critical_slack_limit
-1967.14 Avg: -200.49
comparing new slack -1967.1356 to saved slack -1957.5546
    > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
    for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 21:59:41 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO	Cell	Delay/ P Func	Failed Test/ T.Adj
---------------------------------	-----------------------	----	-------	------	----	----	------	------------------	-----------------------

```

--
1 dcd_succ_last_t1          R C3+R  2966 -1967  3847 1011 1 PO          0
dcd_succ_last_t1
RAT          999          0
----> BOX714/OUT          R C3+R  2966 -1967  3847 1011 1 IOPAD  IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          R C3+R  2966 -1967  3847 1011 1 IOPAD  IOPAD
0 dcd_succ_last_t1&0
----> C167/y          R C3+R  2966 -1967  3847 1011 1 cs_invn 01c NOT
0 dcd_succ_last_t1&0
----> C167/a          F C3+R  1104 -1967   55 139 4 cs_invn 01c NOT
1862 N675
---->{a} C2738/y          F C3+R  1104 -1967   55 139 4 cs_nnd2n 14b NAND
0 N675
----> C2738/a          R C3+R  1075 -1967   71 108 1 cs_nnd2n 14b NAND
29 last_cycle
---->{b} C2487/y          R C3+R  1075 -1967   71 108 1 cs_nnd2n 14e NAND
0 last_cycle
----> C2487/b          F C3+R  1044 -1967   41 124 2 cs_nnd2n 14e NAND
31 N1587
----> C1952/y          F C3+R  1044 -1967   41 124 2 cs_invn 14b NOT    0
N1587
----> C1952/a          R C3+R  1024 -1967   80 139 2 cs_invn 14b NOT

```

20 num_dcd_cyl&0(1)									
----> BOX679/OUT	R C3+R	1024	-1967	80	139	2	IOPAD	IOPAD	
0 num_dcd_cyl&0(1)									
----> BOX679/IN	R C3+R	1024	-1967	80	139	2	IOPAD	IOPAD	0
num_dcd_cyl(1)									
----> num_dcd_cyl(1)	R C3+R	1024	-1967	80	139	2	PI		0
num_dcd_cyl(1)									

--									
2 dcd_succ_last_t1	F C3+R	2616	-1617	2362	1011	1	PO		0
dcd_succ_last_t1									
RAT	999					0			
----> BOX714/OUT	F C3+R	2616	-1617	2362	1011	1	IOPAD	IOPAD	
0 dcd_succ_last_t1									
----> BOX714/IN	F C3+R	2616	-1617	2362	1011	1	IOPAD	IOPAD	
0 dcd_succ_last_t1&0									
----> C167/y	F C3+R	2616	-1617	2362	1011	1	cs_inwn	01c NOT	
0 dcd_succ_last_t1&0									
----> C167/a	R C3+R	1180	-1617	92	139	4	cs_inwn	01c NOT	
1436 N675									
----> {a} C2738/y	R C3+R	1180	-1617	92	139	4	cs_nnd2n	14b NAND	
0 N675									
----> C2738/b	F C3+R	1128	-1617	63	159	3	cs_nnd2n	14b NAND	
52 N1692									
----> {b} C2725rwr/y	F C3+R	1128	-1617	63	159	3	cs_nnd2n	14c NAND	
0 N1692									
----> C2725rwr/a	R C3+R	1086	-1617	134	167	2	cs_nnd2n	14c NAND	
42 N1479									
----> {c} C2721rwr/y	R C3+R	1086	-1617	134	167	2	cs_nnd3n	12c NAND	
0 N1479									
----> C2721rwr/c	F C3+R	994	-1617	125	95	2	cs_nnd3n	12c NAND	
92 N1497									
----> {d} C2709rwr/y	F C3+R	994	-1617	125	95	2	cs_nor3n	10e NOR	
0 N1497									
----> C2709rwr/c	R C3+R	898	-1617	137	68	2	cs_nor3n	10e NOR	
96 N1781									
----> {e} C2885/y	R C3+R	898	-1617	137	68	2	cs_nnd4n	10c NAND	
0 N1781									
----> C2885/d	F C3+R	825	-1617	44	50	1	cs_nnd4n	10c NAND	
73 N1997									
----> {f} C2886/y	F C3+R	825	-1617	44	50	1	cs_nnd2n	14c NAND	
0 N1997									
----> C2886/a	R C3+R	802	-1617	80	124	2	cs_nnd2n	14c NAND	
23 op_serialize&0									
----> BOX638/OUT	R C3+R	802	-1617	80	124	2	IOPAD	IOPAD	
0 op_serialize&0									
----> BOX638/IN	R C3+R	802	-1617	80	124	2	IOPAD	IOPAD	0
op_serialize									
----> op_serialize	R C3+R	802	-1617	80	124	2	PI		0
op_serialize									

--									
3 iu_reset_op_c_t1	R C3+R	2431	-1432	3912	1011	1	PO		0
iu_reset_op_c_t1									
RAT	999					0			

```

----> BOX716/OUT          R C3+R   2431 -1432  3912 1011 1 IOPAD    IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN          R C3+R   2431 -1432  3912 1044 3 IOPAD    IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R   2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a            F C3+R    473 -1432   78 137 3 cs_nnd2n  02c NAND
1958 gbfont_6
----> gbfont_6/y          F C3+R    473 -1432   78 137 3 cs_invvn  09c NOT    0
gbfont_6
----> gbfont_6/a          R C3+R    410 -1432  217  43 1 cs_invvn  09c NOT
64 N2031
---->{b} C2162/y          R C3+R    410 -1432  217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b            F C3+R    303 -1432   57  49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R    303 -1432   57  49 3 cl_invvn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2        R C3+    160  N/C   60 222 13 cl_invvn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160  N/C   60 222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...

```

```

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

```

```

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

```

```

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

```

```

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000

```

```

[tc_parm]: =====

```

```

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000

```

```

> has_dual_rail_children NAND

```

```

> has_dual_rail_children NOR

```

```

> nextbox findtt(TWO_LEVEL,BOX(2),LIMITED)

```

```

[
>>]: nextbox( findtt(TWO_LEVEL,BOX(2),LIMITED) );

```

```

[BD-500000]: findtt CMVC version 1.17 compiled on Apr 13 1999 at 18:23:54

```

```

[create_table_from_view]: No table generated for def cl_scan view EQNVIEW.

```

```

limit search to two levels.

```

```

number of boxes covered by each pattern: 2.

```

```

limit search to offset.

```

```

[BD-502100]: Found 35 patterns.

```

```

[findtt]: Execution time was 0.1 seconds.

```

```

> nextbox findtt(TWO_LEVEL,BOX(3),LIMITED)

```

```

[
>>]: nextbox( findtt(TWO_LEVEL,BOX(3),LIMITED) );

```

```

[create_table_from_view]: No table generated for def cl_scan view EQNVIEW.

```

```

limit search to two levels.

```

```

number of boxes covered by each pattern: 3.

```

```

limit search to offset.

```

```

[BD-502100]: Found 0 patterns.

```

```

[findtt]: Execution time was 0.0 seconds.

```

```

> nextbox tkern

```

```

[
>>]: nextbox( tkern );

```


[tkern]: (W) No AND def - tkern will not apply.

[tkern]: generated patterns for 0 nets

> get_default_delay_synlimit

> tc_parm OFFSET(0)

> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000

[tc_parm]: =====

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000

> nextbox powerize

{

>>]: nextbox(powerize);

[BD-80000]: powerize CMVC version 1.9 compiled on Apr 8 1999 at 05:26:08

[BD-85000]: Changed power level of 35 patterns, added 0 patterns.

> quick trecover(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO1FAN,...

{

>>]: [quick]:(trecover(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO1FAN,NO_VIOLATIONS));

-1967.14 Avg: -200.49

[trecover]: Compiled on Apr 13 1999 at 18:27:36.

[trecover]: setting SCORE option to ALL.

[trecover]: setting RE_POWER option.

[trecover]: setting INC mode.

[trecover]: setting SORT_PINS option.

[trecover]: setting NO1FAN option.

[trecover]: setting NO_VIOLATIONS option.

-1967.14 Avg: -200.49

maximum area for proto box IDCDSUC is 4599

-1967.14 Avg: -200.49

Selected 398 critical boxes of 922 total.

[quick]: Number of boxes to process is 398.

[quick]: Number of boxes processed is 0.

-1967.14 Avg: -189.91

Pattern hint flag is inactive

[cleanup]: 0 boxes disconnected

[trecover]: 309 boxes checked 3 recovered

[trecover]: Execution time was 2.2 seconds.

> measure

The model <IDCDSUC> has:

Primary Inputs = 122

Primary Outputs = 73

Primary BIDs = 0

Signals = 1141

Gate Count = 918

Connections = 1756

Master REG Bits = 83

Slave REG Bits = 83

Internal Area = 4603

External Area = 0

Gates/Connects = 0.522779

Fanout Count = 1756

Average Fanout = 1.539001

Avg Tech Box Size = 5.014161
 Tech Box Size Stddev = 0.010883
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 766
 Real boxes = 543
 Real connections = 1381
 Real LSTs = 2147
 Real ICells/box = 8.476980
 Real LSTs/box = 3.953959
 Real nets/box = 1.410681

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
2		cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000
1		cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1		cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180		BRKPT		>	BRKPT	0	0	0.000	0	0	0.000
195		IOPAD		>	IOPAD	0	0	0.000	0	0	0.000
160		cs_nnd2n02c	02c	>	NAND	3	0	0.000	480	0	0.000
1		cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
2		cs_nnd2n12c	12c	>	NAND	12	0	0.000	24	0	0.000
21		cs_nnd3n02c	02c	>	NAND	4	0	0.000	84	0	0.000
2		cs_nnd2n09c	09c	>	NAND	7	0	0.000	14	0	0.000
3		cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5		cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
2		cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
7		cs_nnd2n14c	14c	>	NAND	19	0	0.000	133	0	0.000
3		cs_nnd2n08c	08c	>	NAND	7	0	0.000	21	0	0.000
1		cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1		cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
1		cs_nnd2n04c	04c	>	NAND	3	0	0.000	3	0	0.000
2		cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1		cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
2		cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
2		cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1		cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1		cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2		cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
10		cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1		cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1		cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1		cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1		cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1		cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
88		cs_invvn01c	01c	>	NOT	2	0	0.000	176	0	0.000
4		cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6		cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
21		cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000

6	cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn07c	07c	>	NOT	2	0	0.000	44	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
8	cs_invvn06c	06c	>	NOT	2	0	0.000	16	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvn14b	14b	>	NOT	10	0	0.000	10	0	0.000
5	cs_invvn08c	08c	>	NOT	4	0	0.000	20	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	55 50* plus *****
2	1 *
3	8 *****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	20 *****
3	1 *
4	5 *****
5	3 ***
6	10 *****
7	3 ***
9	1 *

10	6	*****
12	1	*
13	2	**
14	7	*****
15	7	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	378	350* plus *****
2	202	200* plus **
3	35	*****
4	18	*****

The Histogram Of Fanout vs. Net

# of		
Fanout	Nets	
0	2	**
1	938	900* plus *****
2	99	50* plus *****
3	41	*****
4	17	*****
5	7	*****
6	11	*****
7	3	***
8	3	***
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds.

```

> critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...
critical(
  repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),
  fantom(LIMITED),faninv(LIMITED) );
-1967.14 Avg: -189.91
maximum area for proto box IDCDSUC is 4603
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
fantom: Found 152 valid buffers or inverters.
[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.

```

[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.

-1967.14 Avg: -189.91

ArrayNum: 6 ArrayMax: 918

-1963.71 Avg: -189.33

ArrayNum: 9 ArrayMax: 918

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.1 seconds.

[BD-500100]: 0 parallel copies of gates were made.

[clone]: Execution time was 0.2 seconds.

[BD-500700]: Added 0 buffers.

[fantom]: Execution time was 0.0 seconds.

[BD-500701]: Added 1 inverters.

[faninv]: Execution time was 2.0 seconds.

[BD-502000]: Called transforms 48 times and applied 1 of them.

> nextbox synexpand(XPANDVIEW)

[

>>]: nextbox(synexpand(XPANDVIEW));

[restore_pin_keywords]: restored 0 keywords

[

>>]: nextbox(SASname(RESTORE));

[synsasname]: Restored 0 BRKPT net names

[synsasname]: Restored 189 REG and SEQUENTIAL output net names

[synsasname]: Execution time was 0.0 seconds.

[restore_pin_keywords]: deleted 0 nets and pins

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1142 signals, 919 usage boxes and 1757 connections.

[

>>]: nextbox(SASname(PROTECT));

[synsasname]: Protected 180 BRKPT net names

[synsasname]: Protected 189 REG and SEQUENTIAL output net names

[synsasname]: Execution time was 0.0 seconds.

[synexpand]: expanded 0 boxes

> measure

The model <IDCDSUC> has:

Primary Inputs	=	122
Primary Outputs	=	73
Primary BIDs	=	0
Signals	=	1142
Gate Count	=	919
Connections	=	1757
Master REG Bits	=	83
Slave REG Bits	=	83
Internal Area	=	4623
External Area	=	0
Gates/Connects	=	0.523051
Fanout Count	=	1757
Average Fanout	=	1.538529
Avg Tech Box Size	=	5.030468
Tech Box Size Stddev	=	0.010896
Power	=	0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 767

Real boxes = 544
 Real connections = 1382
 Real LSTs = 2149
 Real ICells/box = 8.498162
 Real LSTs/box = 3.950368
 Real nets/box = 1.409926

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
2		cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000
1		cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1		cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180		BRKPT	>	BRKPT	0	0	0.000	0	0	0.000	
195		IOPAD	>	IOPAD	0	0	0.000	0	0	0.000	
160		cs_nnd2n02c	02c	>	NAND	3	0	0.000	480	0	0.000
1		cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
2		cs_nnd2n12c	12c	>	NAND	12	0	0.000	24	0	0.000
21		cs_nnd3n02c	02c	>	NAND	4	0	0.000	84	0	0.000
2		cs_nnd2n09c	09c	>	NAND	7	0	0.000	14	0	0.000
3		cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5		cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
2		cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
7		cs_nnd2n14c	14c	>	NAND	19	0	0.000	133	0	0.000
3		cs_nnd2n08c	08c	>	NAND	7	0	0.000	21	0	0.000
1		cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
1		cs_nnd2n14e	14e	>	NAND	19	0	0.000	19	0	0.000
1		cs_nnd2n04c	04c	>	NAND	3	0	0.000	3	0	0.000
2		cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1		cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd3n12c	12c	>	NAND	22	0	0.000	22	0	0.000
2		cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
2		cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1		cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1		cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2		cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
10		cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1		cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1		cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1		cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1		cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1		cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
88		cs_invvn01c	01c	>	NOT	2	0	0.000	176	0	0.000
4		cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6		cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
21		cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
6		cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
22		cs_invvn07c	07c	>	NOT	2	0	0.000	44	0	0.000
4		cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
8		cs_invvn06c	06c	>	NOT	2	0	0.000	16	0	0.000
12		cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000

6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvn19b	19b	>	NOT	28	0	0.000	28	0	0.000
5	cs_invvn08c	08c	>	NOT	4	0	0.000	20	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n03c	03c	>	OAI	6	0	0.000	6	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	55 50* plus *****
2	1 *
3	8 *****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	20 *****
3	1 *
4	5 *****
5	3 ***
6	10 *****
7	3 ***
9	1 *
10	6 *****
12	1 *
13	2 **
14	7 *****

15	7	*****
16	3	***
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	379	350* plus *****
2	202	200* plus **
3	35	*****
4	18	*****

The Histogram Of Fanout vs. Net

# of		
Fanout	Nets	
0	2	**
1	940	900* plus *****
2	97	50* plus *****
3	42	*****
4	17	*****
5	7	*****
6	11	*****
7	3	***
8	3	***
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds.

> write_end_point_report -points 3 -paths 1

[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 21:59:52 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack	Abbreviation	Comparison/Description
----------------	--------------	------------------------

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK

----> C2909/a	F C3+R	835	-1964	80	108	1	cs_nnd2n	14c	NAND	
37 dcd_mcr41_blk&0										
----> BOX615/OUT	F C3+R	835	-1964	80	108	1	IOPAD		IOPAD	
0 dcd_mcr41_blk&0										
----> BOX615/IN	F C3+R	835	-1964	80	108	1	IOPAD		IOPAD	0
dcd_mcr41_blk										
----> dcd_mcr41_blk	F C3+R	835	-1964	80	108	1	PI			0
dcd_mcr41_blk										

--										
2 dcd_succ_last_t1	F C3+R	2616	-1617	2362	1011	1	PO			0
dcd_succ_last_t1										
RAT	999						0			
----> BOX714/OUT	F C3+R	2616	-1617	2362	1011	1	IOPAD		IOPAD	
0 dcd_succ_last_t1										
----> BOX714/IN	F C3+R	2616	-1617	2362	1011	1	IOPAD		IOPAD	
0 dcd_succ_last_t1&0										
----> C167/y	F C3+R	2616	-1617	2362	1011	1	cs_invvn	01c	NOT	
0 dcd_succ_last_t1&0										
----> C167/a	R C3+R	1180	-1617	92	139	4	cs_invvn	01c	NOT	
1436 N675										
---->{a} C2738/y	R C3+R	1180	-1617	92	139	4	cs_nnd2n	14b	NAND	
0 N675										
----> C2738/b	F C3+R	1128	-1617	63	159	3	cs_nnd2n	14b	NAND	
52 N1692										
---->{b} C2725rwr/y	F C3+R	1128	-1617	63	159	3	cs_nnd2n	14c	NAND	
0 N1692										
----> C2725rwr/a	R C3+R	1086	-1617	134	167	2	cs_nnd2n	14c	NAND	
42 N1479										
---->{c} C2721rwr/y	R C3+R	1086	-1617	134	167	2	cs_nnd3n	12c	NAND	
0 N1479										
----> C2721rwr/c	F C3+R	994	-1617	125	95	2	cs_nnd3n	12c	NAND	
92 N1497										
---->{d} C2709rwr/y	F C3+R	994	-1617	125	95	2	cs_nor3n	10e	NOR	
0 N1497										
----> C2709rwr/c	R C3+R	898	-1617	137	68	2	cs_nor3n	10e	NOR	
96 N1781										
---->{e} C2885/y	R C3+R	898	-1617	137	68	2	cs_nnd4n	10c	NAND	
0 N1781										
----> C2885/d	F C3+R	825	-1617	44	50	1	cs_nnd4n	10c	NAND	
73 N1997										
---->{f} C2886/y	F C3+R	825	-1617	44	50	1	cs_nnd2n	14c	NAND	
0 N1997										
----> C2886/a	R C3+R	802	-1617	80	124	2	cs_nnd2n	14c	NAND	
23 op_serialize&0										
----> BOX638/OUT	R C3+R	802	-1617	80	124	2	IOPAD		IOPAD	
0 op_serialize&0										
----> BOX638/IN	R C3+R	802	-1617	80	124	2	IOPAD		IOPAD	0
op_serialize										
----> op_serialize	R C3+R	802	-1617	80	124	2	PI			0
op_serialize										

--										
3 iu_reset_op_c_t1	R C3+R	2431	-1432	3912</						

RAT	999	0	
----> BOX716/OUT	R C3+R	2431 -1432 3912 1011 1 IOPAD	IOPAD
0 iu_reset_op_c_t1			
----> BOX716/IN	R C3+R	2431 -1432 3912 1044 3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0			
---->{a} C2393/y	R C3+R	2431 -1432 3912 1044 3 cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0			
----> C2393/a	F C3+R	473 -1432 78 137 3 cs_nnd2n	02c NAND
1958 gbfonet_6			
----> gbfozell_6/y	F C3+R	473 -1432 78 137 3 cs_invvn	09c NOT 0
gbfonet_6			
----> gbfozell_6/a	R C3+R	410 -1432 217 43 1 cs_invvn	09c NOT
64 N2031			
---->{b} C2162/y	R C3+R	410 -1432 217 43 1 cs_nnd3n	02c NAND
0 N2031			
----> C2162/b	F C3+R	303 -1432 57 49 3 cs_nnd3n	02c NAND
107 rcvry_reset_q			
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R	303 -1432 57 49 3 cl_invvn	07d SRL
0 rcvry_reset_q			
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160 N/C 60 222 13 cl_invvn	07d SRL
143 slow_mode.c2_1			
----> slow_mode.clockblock/c2	R C3+	160 N/C 60 222 13 cb_clk_32_1	LCB
0 slow_mode.c2_1			

```

--
> treematch {ACTUAL ,TWO_LEVEL,NO_VIOLATIONS}
[
-->]: ltorbox( dtreematch(ACTUAL ,TWO_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1963.71 Avg: -189.33
[BD-500301]: 8 pins on 3 gates swapped.
-1963.69 Avg: -190.04
[treematch]: Execution time was 0.9 seconds.
> fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}

```

```

[
-->]: ltorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1963.69 Avg: -190.04
[BD-500300]: 25 pins on 11 gates swapped.
-1963.71 Avg: -189.83
[fanmatch]: Execution time was 3.7 seconds.
> get_default_delay_synlimit
> tc_parm OFFSET(0)
> tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),W...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
> reset_critical_slack_limit

```

-1963.71 Avg: -189.83
 resetting the current slack to -1963.7057
 > repower_paths FUZZY(0.02)
 initial slack is -1964
 after repower paths slack is -1964
 > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS), repower...
 critical(repower(SCORE(ALL),INC,NO_VIOLATIONS),
 repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
 -1963.71 Avg: -189.46
 maximum area for proto box IDCDSUC is 4648
 repower: setting SCORE option to ALL.
 repower: setting INC mode.
 repower: setting NO_VIOLATIONS option.
 repower: setting SCORE option to ALL.
 repower: setting INC mode.
 repower: setting NO_VIOLATIONS option.
 -1963.71 Avg: -189.46
 ArrayNum: 9 ArrayMax: 919
 -1956.14 Avg: -188.82
 ArrayNum: 9 ArrayMax: 919
 -1955.13 Avg: -188.47
 ArrayNum: 6 ArrayMax: 919
 [BD-500026]: repower was applied 2 times.
 [repower]: Execution time was 0.6 seconds.
 [BD-500026]: repower was applied 2 times.
 [repower]: Execution time was 0.6 seconds.
 [BD-502000]: Called transforms 32 times and applied 2 of them.
 > compare_critical_slack_limit
 -1955.13 Avg: -188.47
 comparing new slack -1955.1339 to saved slack -1944.0686
 > syntrace
 > write_end_point_report -points 10
 [ET-0018]: >Begin...New EndPoint Report
 for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:00:16 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 10

Cause of Slack Abbreviation Comparison/Description

Cause of Slack	Abbreviation	Comparison/Description
Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +

ADJUST)
 Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj
--								
1 dcd_succ_last_t1	R C3+R	2954	-1955	3847	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	R C3+R	2954	-1955	3847	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2954	-1955	3847	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2954	-1955	3847	1011	1 cs_invvn	01c	NOT
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1092	-1955	55	139	4 cs_invvn	01c	NOT
1862 N675								
---->{a} C2738/y	F C3+R	1092	-1955	55	139	4 cs_nnd2n	14b	NAND
0 N675								
----> C2738/a	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14b	NAND
29 last_cycle								
---->{b} C2487/y	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14e	NAND
0 last_cycle								
----> C2487/b	F C3+R	1034	-1955	32	140	3 cs_nnd2n	14e	NAND
29 N1587								
----> C1952/y	F C3+R	1034	-1955	32	140	3 cs_invvv	19b	NOT
N1587								0
----> C1952/a	R C3+R	1024	-1955	80	319	1 cs_invvv	19b	NOT
10 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1955	80	319	1 IOPAD		IOPAD
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1955	80	319	1 IOPAD		IOPAD
num_dcd_cyl(1)								0
----> num_dcd_cyl(1)	R C3+R	1024	-1955	80	319	1 PI		
num_dcd_cyl(1)								
--								
2 dcd_succ_last_t1	F C3+R	2644	-1645	2362	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	F C3+R	2644	-1645	2362	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1								
----> BOX714/IN	F C3+R	2644	-1645	2362	1011	1 IOPAD		IOPAD

0 dcd_succ_last_t1&0	
----> C167/y	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0	
----> C167/a	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
1436 N675	
---->{a} C2738/y	R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
0 N675	
----> C2738/b	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
56 N1692	
---->{b} C2725rwr/y	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND
0 N1692	
----> C2725rwr/a	R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND
56 N1479	
---->{c} C2721rwr/y	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
0 N1479	
----> C2721rwr/c	F C3+R 994 -1645 125 95 2 cs_nnd3n 12b NAND
102 N1497	
---->{d} C2709rwr/y	F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
0 N1497	
----> C2709rwr/c	R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR
96 N1781	
---->{e} C2885/y	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
0 N1781	
----> C2885/d	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
73 N1997	
---->{f} C2886/y	F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
0 N1997	
----> C2886/a	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
23 op_serialize&0	
----> BOX638/OUT	R C3+R 802 -1645 80 124 2 IOPAD IOPAD
0 op_serialize&0	
----> BOX638/IN	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
op_serialize	
----> op_serialize	R C3+R 802 -1645 80 124 2 PI 0
op_serialize	

3 iu_reset_op_c_t1	R C3+R 2431 -1432 3912 1011 1 PO 0
iu_reset_op_c_t1	
RAT	999 0
----> BOX716/OUT	R C3+R 2431 -1432 3912 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	
----> BOX716/IN	R C3+R 2431 -1432 3912 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	
---->{a} C2393/y	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	
----> C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6	
----> gbfonet_6/y	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
gbfonet_6	
----> gbfonet_6/a	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
64 N2031	
---->{b} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
0 N2031	
----> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND

```

107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n      F C3+R    303 -1432   57   49 3 cl_invvn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+      160   N/C    60  222 13 cl_invvn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+      160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
  4 local_milli_t2.reg_n.lat_0/a          F C3+R    2675 -1366   103   92 3 cl_invvn  07c SRL
51 NET1056
Setup local_milli_t2.reg_n.lat_0/c1      F C3-      160     60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                          F C3+R    2675 -1366   103   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/b                             R C3+R    2620 -1366   139   36 1 cs_nnd3z  07c NAND
55 NET1054
---->{b} BOX785/y                          R C3+R    2620 -1366   139   36 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                             F C3+R    2542 -1366   116   19 1 cs_nnd2f  03c NAND
78 N1866
---->{c} C2555/y                          F C3+R    2542 -1366   116   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                             R C3+R    2431 -1366  3912 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                          R C3+R    2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                             F C3+R    473 -1432   78  137 3 cs_nnd2n  02c NAND--
1958 gbfonet_6
----> gbfcocell_6/y                       F C3+R    473 -1432   78  137 3 cs_invvn  09c NOT   0
gbfonet_6
----> gbfcocell_6/a                       R C3+R    410 -1432   217   43 1 cs_invvn  09c NOT
64 N2031
---->{e} C2162/y                          R C3+R    410 -1432   217   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b                             F C3+R    303 -1432   57   49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n      F C3+R    303 -1432   57   49 3 cl_invvn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+      160   N/C    60  222 13 cl_invvn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+      160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
  5 local_milli_t1.reg_n.lat_0/a          F C3+R    2675 -1366   103   92 3 cl_invvn  07c SRL
51 NET1056
Setup local_milli_t1.reg_n.lat_0/c1      F C3-      160     60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                          F C3+R    2675 -1366   103   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/b                             R C3+R    2620 -1366   139   36 1 cs_nnd3z  07c NAND
55 NET1054
---->{b} BOX785/y                          R C3+R    2620 -1366   139   36 1 cs_nnd2f  03c NAND
0 NET1054

```

```

----> BOX785/a          F C3+R  2542 -1366  116  19 1 cs_nnd2f  03c NAND
78 N1866
---->{c} C2555/y        F C3+R  2542 -1366  116  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b          R C3+R  2431 -1366  3912 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y        R C3+R  2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R  473  -1432   78  137 3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfozell_6/y      F C3+R  473  -1432   78  137 3 cs_invn  09c NOT    0
gbfonet_6
----> gbfozell_6/a      R C3+R  410  -1432  217   43 1 cs_invn  09c NOT
64 N2031
---->{e} C2162/y        R C3+R  410  -1432  217   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b          F C3+R  303  -1432   57   49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R  303  -1432   57   49 3 cl_invn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2        R C3+   160   N/C   60  222 13 cl_invn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+   160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
6 local_milli.reg_n.lat_0/a  F C3+R  2675 -1366  103   92 3 cl_invn  07c SRL
51 NET1056
Setup local_milli.reg_n.lat_0/c1  F C3-   160         60  238 14 cl_invn  07c    1200
slow_mode.c1_2
---->{a} BOX789/y        F C3+R  2675 -1366  103   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/b          R C3+R  2620 -1366  139   36 1 cs_nnd3z  07c NAND
55 NET1054
---->{b} BOX785/y        R C3+R  2620 -1366  139   36 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a          F C3+R  2542 -1366  116   19 1 cs_nnd2f  03c NAND
78 N1866
---->{c} C2555/y        F C3+R  2542 -1366  116   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b          R C3+R  2431 -1366  3912 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y        R C3+R  2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R  473  -1432   78  137 3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfozell_6/y      F C3+R  473  -1432   78  137 3 cs_invn  09c NOT    0
gbfonet_6
----> gbfozell_6/a      R C3+R  410  -1432  217   43 1 cs_invn  09c NOT
64 N2031
---->{e} C2162/y        R C3+R  410  -1432  217   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b          F C3+R  303  -1432   57   49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R  303  -1432   57   49 3 cl_invn  07d SRL

```



```

0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+   160   N/C   60  222 13 cl_invrn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+   160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
7 local_milli_t2.reg_n.lat_0/a      R C3+R  2591 -1236  165  92 3 cl_invrn  07c SRL
5 NET1056
Setup local_milli_t2.reg_n.lat_0/c1  F C3-   160         60  238 14 cl_invrn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y      R C3+R  2591 -1236  165  92 3 cs_nnd3z  07c.NAND
0 NET1056
----> BOX789/a      F C3+R  2511 -1236  107  32 1 cs_nnd3z  07c NAND
80 N639
---->{b} C2466/y      F C3+R  2511 -1236  107  32 1 cs_nnd2n  02c NAND
0 N639
----> C2466/b      R C3+R  2431 -1236  3912 1044 3 cs_nnd2n  02c NAND
80 iu_reset_op_c_t1&0
---->{c} C2393/y      R C3+R  2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a      F C3+R  473 -1432   78  137 3 cs_nnd2n  02c NAND
1958 gbfont_6
----> gbfont_6/y      F C3+R  473 -1432   78  137 3 cs_invrn  09c NOT    0
gbfont_6
----> gbfont_6/a      R C3+R  410 -1432  217   43 1 cs_invrn  09c NOT
64 N2031
---->{d} C2162/y      R C3+R  410 -1432  217   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b      F C3+R  303 -1432   57   49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R  303 -1432   57   49 3 cl_invrn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+   160   N/C   60  222 13 cl_invrn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+   160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
8 local_milli_t1.reg_n.lat_0/a      R C3+R  2591 -1236  165  92 3 cl_invrn  07c SRL
5 NET1056
Setup local_milli_t1.reg_n.lat_0/c1  F C3-   160         60  238 14 cl_invrn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y      R C3+R  2591 -1236  165  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a      F C3+R  2511 -1236  107  32 1 cs_nnd3z  07c NAND
80 N639
---->{b} C2466/y      F C3+R  2511 -1236  107  32 1 cs_nnd2n  02c NAND
0 N639
----> C2466/b      R C3+R  2431 -1236  3912 1044 3 cs_nnd2n  02c NAND
80 iu_reset_op_c_t1&0
---->{c} C2393/y      R C3+R  2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a      F C3+R  473 -1432   78  137 3 cs_nnd2n  02c NAND
1958 gbfont_6

```

```

----> gbfcocell_6/y          F C3+R   473 -1432   78  137 3 cs_invvn  09c NOT    0
gbfonet_6
----> gbfcocell_6/a          R C3+R   410 -1432   217  43 1 cs_invvn  09c NOT
64 N2031
----> {d} C2162/y           R C3+R   410 -1432   217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b               F C3+R   303 -1432   57  49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   303 -1432   57  49 3 cl_invvn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+    160  N/C   60 222 13 cl_invvn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+    160  N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
    9 local_milli.reg_n.lat_0/a R C3+R  2591 -1236  165  92 3 cl_invvn  07c SRL
5 NET1056
Setup local_milli.reg_n.lat_0/c1 F C3-    160          60 238 14 cl_invvn  07c    1200
slow_mode.c1_2
----> {a} BOX789/y          R C3+R  2591 -1236  165  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a              F C3+R  2511 -1236  107  32 1 cs_nnd3z  07c NAND
80 N639
----> {b} C2466/y           F C3+R  2511 -1236  107  32 1 cs_nnd2n  02c NAND
0 N639
----> C2466/b               R C3+R  2431 -1236  3912 1044 3 cs_nnd2n  02c NAND
80 iu_reset_op_c_t1&0
----> {c} C2393/y           R C3+R  2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a               F C3+R   473 -1432   78  137 3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfcocell_6/y          F C3+R   473 -1432   78  137 3 cs_invvn  09c NOT    0
gbfonet_6
----> gbfcocell_6/a          R C3+R   410 -1432   217  43 1 cs_invvn  09c NOT
64 N2031
----> {d} C2162/y           R C3+R   410 -1432   217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b               F C3+R   303 -1432   57  49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   303 -1432   57  49 3 cl_invvn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+    160  N/C   60 222 13 cl_invvn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+    160  N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
    10 iu_reset_op_c_t1        F C3+R  2130 -1131  2719 1011 1 PO          0
iu_reset_op_c_t1
RAT                            999                                0
----> BOX716/OUT             F C3+R  2130 -1131  2719 1011 1 IOPAD    IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN              F C3+R  2130 -1131  2719 1044 3 IOPAD    IOPAD
0 iu_reset_op_c_t1&0

```

```

---->{a} C2393/y          F C3+R   2130 -1131  2719 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a             R C3+R   451 -1131   118 137 3 cs_nnd2n  02c NAND
1679 gbfonet_6
----> gbfofcell_6/y       R C3+R   451 -1131   118 137 3 cs_invvn  09c NOT
0 gbfonet_6
----> gbfofcell_6/a       F C3+R   370 -1131   158 43 1 cs_invvn  09c NOT
81 N2031
---->{b} C2162/y          F C3+R   370 -1131   158 43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b             R C3+R   290 -1131   46 49 3 cs_nnd3n  02c NAND
81 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n R C3+R   290 -1131   46 49 3 cl_invvn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2       R C3+    160  N/C   60 222 13 cl_invvn  07d SRL
130 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160  N/C   60 222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

--

> measure

The model <IDCDSUC> has:

```

Primary Inputs   =      122
Primary Outputs  =      73
Primary BIDs     =       0
Signals          =     1142
Gate Count       =      919
Connections      =     1757
Master REG Bits  =      83
Slave REG Bits   =      83
Internal Area    =     4648
External Area    =       0
Gates/Connects  =     0.523051
Fanout Count     =     1757
Average Fanout   =     1.538529
Avg Tech Box Size =     5.057671
Tech Box Size Stddev =     0.010912
Power            =     0.000000

```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```

Real signals     =      767
Real boxes       =      544
Real connections =     1382
Real LSTs        =     2149
Real ICells/box  =     8.544118
Real LSTs/box    =     3.950368
Real nets/box    =     1.409926

```

```

Cell            Total
Each            Cell

```

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
7		cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
2		cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000
1		cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000

1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180	BRKPT		>	BRKPT	0	0	0.000	0	0	0.000
195	IOPAD		>	IOPAD	0	0	0.000	0	0	0.000
160	cs_nnd2n02c	02c	>	NAND	3	0	0.000	480	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
3	cs_nnd2n12c	12c	>	NAND	12	0	0.000	36	0	0.000
21	cs_nnd3n02c	02c	>	NAND	4	0	0.000	84	0	0.000
4	cs_nnd2n11c	11c	>	NAND	11	0	0.000	44	0	0.000
3	cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
2	cs_nnd2n14e	14e	>	NAND	19	0	0.000	38	0	0.000
1	cs_nnd2n04c	04c	>	NAND	3	0	0.000	3	0	0.000
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12b	12b	>	NAND	22	0	0.000	22	0	0.000
2	cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
2	cs_nnd2n08c	08c	>	NAND	7	0	0.000	14	0	0.000
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
88	cs_invvn01c	01c	>	NOT	2	0	0.000	176	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
21	cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
6	cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn07c	07c	>	NOT	2	0	0.000	44	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
8	cs_invvn06c	06c	>	NOT	2	0	0.000	16	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvn19b	19b	>	NOT	28	0	0.000	28	0	0.000
5	cs_invvn08c	08c	>	NOT	4	0	0.000	20	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000

8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	55 50* plus *****
2	1 *
3	8 *****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	20 *****
3	1 *
4	5 *****
5	3 ***
6	10 *****
7	3 ***
9	1 *
10	6 *****
12	1 *
14	6 *****
15	9 *****
16	4 ****
17	14 *****

The Histogram Of Fanin vs. Box

# of Fanin	Ops
1	379 350* plus *****
2	202 200* plus **
3	35 *****
4	18 *****

The Histogram Of Fanout vs. Net

# of		
Fanout	Nets	
0	2	**
1	940	900* plus *****
2	97	50* plus *****
3	42	*****
4	17	*****
5	7	*****
6	11	*****
7	3	***
8	3	***
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds:

> randsim q

[

>>]: randsim(q);

> echo {inside loop}

inside loop

> measure

The model <IDCDSUC> has:

Primary Inputs	=	122
Primary Outputs	=	73
Primary BIDs	=	0
Signals	=	1142
Gate Count	=	919
Connections	=	1757
Master REG Bits	=	83
Slave REG Bits	=	83
Internal Area	=	4648
External Area	=	0
Gates/Connects	=	0.523051
Fanout Count	=	1757
Average Fanout	=	1.538529
Avg Tech Box Size	=	5.057671
Tech Box Size Stddev	=	0.010912
Power	=	0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals	=	767
Real boxes	=	544
Real connections	=	1382
Real LSTs	=	2149
Real ICells/box	=	8.544118
Real LSTs/box	=	3.950368
Real nets/box	=	1.409926

Cell	Total
Each	Cell

Type	Cnt	Boxname	Power Level	Function	Int	Ext	Power	Int	Ext	Power
------	-----	---------	-------------	----------	-----	-----	-------	-----	-----	-------

7	cs_ao22n03c	03c	>	AOI	6	0	0.000	42	0	0.000
2	cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000
1	cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1	cs_ao12n04c	04c	>	AOI	4	0	0.000	4	0	0.000
180	BRKPT	>	BRKPT		0	0	0.000	0	0	0.000
195	IOPAD	>	IOPAD		0	0	0.000	0	0	0.000
160	cs_nnd2n02c	02c	>	NAND	3	0	0.000	480	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
3	cs_nnd2n12c	12c	>	NAND	12	0	0.000	36	0	0.000
21	cs_nnd3n02c	02c	>	NAND	4	0	0.000	84	0	0.000
4	cs_nnd2n11c	11c	>	NAND	11	0	0.000	44	0	0.000
3	cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
2	cs_nnd2n14e	14e	>	NAND	19	0	0.000	38	0	0.000
1	cs_nnd2n04c	04c	>	NAND	3	0	0.000	3	0	0.000
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12b	12b	>	NAND	22	0	0.000	22	0	0.000
2	cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
2	cs_nnd2n08c	08c	>	NAND	7	0	0.000	14	0	0.000
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
10	cs_nor2n02c	02c	>	NOR	3	0	0.000	30	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor2n04c	04c	>	NOR	3	0	0.000	3	0	0.000
1	cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
88	cs_invvn01c	01c	>	NOT	2	0	0.000	176	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
21	cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
6	cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
22	cs_invvn07c	07c	>	NOT	2	0	0.000	44	0	0.000
4	cs_invvn15c	15c	>	NOT	10	0	0.000	40	0	0.000
8	cs_invvn06c	06c	>	NOT	2	0	0.000	16	0	0.000
12	cs_invvn05c	05c	>	NOT	2	0	0.000	24	0	0.000
6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvv19b	19b	>	NOT	28	0	0.000	28	0	0.000
5	cs_invvn08c	08c	>	NOT	4	0	0.000	20	0	0.000
6	cs_invvn02c	02c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
3	cs_invvn04c	04c	>	NOT	2	0	0.000	6	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
2	cs_invvn16c	16c	>	NOT	14	0	0.000	28	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000

1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
22	cl_invvn07c	07c	>	REG	25	0	0.000	550	0	0.000
30	cl_invvn07d	07d	>	REG	25	0	0.000	750	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	55 50* plus *****
2	1 *
3	8 *****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	20 *****
3	1 *
4	5 *****
5	3 ***
6	10 *****
7	3 ***
9	1 *
10	6 *****
12	1 *
14	6 *****
15	9 *****
16	4 *****
17	14 *****

The Histogram Of Fanin vs. Box

# of Fanin	Ops
1	379 350* plus *****
2	202 200* plus **


```

3    35    *****
4    18    *****

```

The Histogram Of Fanout vs. Net

of
Fanout Nets

```

-----
0     2    **
1    940   900* plus *****
2     97   50* plus *****
3     42   *****
4     17   *****
5      7   *****
6     11   *****
7      3   ***
8      3   ***
13     3   ***
14    16   *****
20     1   *

```

[End of measure]

[measure]: Execution time was 0.6 seconds.

> write_end_point_report -points 3 -paths 1

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:00:19 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time    RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AsrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup       ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold        ClkGHld     ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width   ClkTPW     ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                    Setup      ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                     Hold       ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle               EndOfC     ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth          ClkPW     ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )

```

ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	-------------------------------------

```

--
1 dcd_succ_last_t1          R C3+R  2954 -1955  3847 1011 1 PO          0
dcd_succ_last_t1
RAT          999          0
----> BOX714/OUT          R C3+R  2954 -1955  3847 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          R C3+R  2954 -1955  3847 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y          R C3+R  2954 -1955  3847 1011 1 cs_invrn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          F C3+R  1092 -1955   55 139 4 cs_invrn  01c NOT
1862 N675
---->{a} C2738/y          F C3+R  1092 -1955   55 139 4 cs_nnd2n  14b NAND
0 N675
----> C2738/a          R C3+R  1063 -1955   71 108 1 cs_nnd2n  14b NAND
29 last_cycle
---->{b} C2487/y          R C3+R  1063 -1955   71 108 1 cs_nnd2n  14e NAND
0 last_cycle
----> C2487/b          F C3+R  1034 -1955   32 140 3 cs_nnd2n  14e NAND
29 N1587
----> C1952/y          F C3+R  1034 -1955   32 140 3 cs_invrn  19b NOT      0
N1587
----> C1952/a          R C3+R  1024 -1955   80 319 1 cs_invrn  19b NOT
10 num_dcd_cyl&0(1)
----> BOX679/OUT          R C3+R  1024 -1955   80 319 1 IOPAD      IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN          R C3+R  1024 -1955   80 319 1 IOPAD      IOPAD      0
num_dcd_cyl(1)
----> num_dcd_cyl(1)          R C3+R  1024 -1955   80 319 1 PI          0
num_dcd_cyl(1)

```

```

--
2 dcd_succ_last_t1          F C3+R  2644 -1645  2362 1011 1 PO          0
dcd_succ_last_t1
RAT          999          0
----> BOX714/OUT          F C3+R  2644 -1645  2362 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          F C3+R  2644 -1645  2362 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y          F C3+R  2644 -1645  2362 1011 1 cs_invrn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          R C3+R  1208 -1645   92 139 4 cs_invrn  01c NOT
1436 N675
---->{a} C2738/y          R C3+R  1208 -1645   92 139 4 cs_nnd2n  14b NAND
0 N675

```

Access	Address	Size	Offset	Value	Mask	Unit	Function	Notes
---->	C2738/b	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14b NAND
56	N1692							
---->	{b} C2725rwr/y	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14e NAND
0	N1692							
---->	C2725rwr/a	R C3+R	1097	-1645	148	166	2 cs_nnd2n	14e NAND
56	N1479							
---->	{c} C2721rwr/y	R C3+R	1097	-1645	148	166	2 cs_nnd3n	12b NAND
0	N1479							
---->	C2721rwr/c	F C3+R	994	-1645	125	95	2 cs_nnd3n	12b NAND
102	N1497							
---->	{d} C2709rwr/y	F C3+R	994	-1645	125	95	2 cs_nor3n	10e NOR
0	N1497							
---->	C2709rwr/c	R C3+R	898	-1645	137	68	2 cs_nor3n	10e NOR
96	N1781							
---->	{e} C2885/y	R C3+R	898	-1645	137	68	2 cs_nnd4n	10c NAND
0	N1781							
---->	C2885/d	F C3+R	825	-1645	44	50	1 cs_nnd4n	10c NAND
73	N1997							
---->	{f} C2886/y	F C3+R	825	-1645	44	50	1 cs_nnd2n	14c NAND
0	N1997							
---->	C2886/a	R C3+R	802	-1645	80	124	2 cs_nnd2n	14c NAND
23	op_serialize&0							
---->	BOX638/OUT	R C3+R	802	-1645	80	124	2 IOPAD	IOPAD
0	op_serialize&0							
---->	BOX638/IN	R C3+R	802	-1645	80	124	2 IOPAD	IOPAD
0	op_serialize							
---->	op_serialize	R C3+R	802	-1645	80	124	2 PI	0
0	op_serialize							
<hr/>								
3	iu_reset_op_c_t1	R C3+R	2431	-1432	3912	1011	1 PO	0
iu_reset_op_c_t1								
RAT			999				0	
---->	BOX716/OUT	R C3+R	2431	-1432	3912	1011	1 IOPAD	IOPAD
0	iu_reset_op_c_t1							
---->	BOX716/IN	R C3+R	2431	-1432	3912	1044	3 IOPAD	IOPAD
0	iu_reset_op_c_t1&0							
---->	{a} C2393/y	R C3+R	2431	-1432	3912	1044	3 cs_nnd2n	02c NAND
0	iu_reset_op_c_t1&0							
---->	C2393/a	F C3+R	473	-1432	78	137	3 cs_nnd2n	02c NAND
1958	gbfonet_6							
---->	gbfocell_6/y	F C3+R	473	-1432	78	137	3 cs_invvn	09c NOT
0	gbfonet_6							
---->	gbfocell_6/a	R C3+R	410	-1432	217	43	1 cs_invvn	09c NOT
64	N2031							
---->	{b} C2162/y	R C3+R	410	-1432	217	43	1 cs_nnd3n	02c NAND
0	N2031							
---->	C2162/b	F C3+R	303	-1432	57	49	3 cs_nnd3n	02c NAND
107	rcvry_reset_q							
---->	rcvry_reset.reg_n.lat_0/12_out_n	F C3+R	303	-1432	57	49	3 cl_invvn	07d SRL
0	rcvry_reset_q							
---->	rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13 cl_invvn	07d SRL
143								

```

-----
--
    > reset_critical_slack_limit
-1955.13 Avg: -188.47
resetting the current slack to -1955.1339
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1), ...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
    > hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao...
    > hide -no_clear -cells { cs_buffe }
    > hide -no_clear -cells { cs_invvn cs_invvv }
    > hide -no_clear -cells { cs_nnd2f cs_nnd2g cs_nnd2n cs_nn...
    > hide -no_clear -cells { cs_nnd3f cs_nnd3g cs_nnd3h cs_nn...
    > hide -no_clear -cells { cs_nnd4n cs_nnd4v }
    > hide -no_clear -cells { cs_nor2f cs_nor2g cs_nor2n cs_no...
    > hide -no_clear -cells { cs_nor3f cs_nor3g cs_nor3h cs_no...
    > hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
    > hide -no_clear -cells { cs_ao21n cs_ao21v }
    > hide -no_clear -cells { cs_ao22n cs_ao22v }
    > hide -no_clear -cells { cs_xbn2n cs_xbn2v }
    > hide -no_clear -cells { cs_xbo2n cs_xbo2v }
    > find cell cs_*
    > hide -no_clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f0...
    > find cell cs_buffe*
    > hide -no_clear -cells {cs_buffe01a cs_buffe02a cs_buffe0...
    > hide -clear -cells { "cs_invvn" }
    > find cell cs_invvn*c
    > hide -clear -cells {cs_invvn01c cs_invvn02c cs_invvn03c ...
    > hide -clear -cells { "cs_nnd2n" }
    > find cell cs_nnd2n*c
    > hide -clear -cells {cs_nnd2n02c cs_nnd2n03c cs_nnd2n04c ...
    > hide -clear -cells { "cs_nnd3n" }
    > find cell cs_nnd3n*c
    > hide -clear -cells {cs_nnd3n02c cs_nnd3n03c cs_nnd3n04c ...
    > hide -clear -cells { "cs_nnd4n" }
    > find cell cs_nnd4n*c
    > hide -clear -cells {cs_nnd4n03c cs_nnd4n04c cs_nnd4n05c ...
    > hide -clear -cells { "cs_nor2n" }
    > find cell cs_nor2n*c
    > hide -clear -cells {cs_nor2n02c cs_nor2n03c cs_nor2n04c ...
    > hide -clear -cells { "cs_nor3n" }
    > find cell cs_nor3n*c
    > hide -clear -cells {cs_nor3n03c cs_nor3n04c cs_nor3n05c ...
    > hide -clear -cells { "cs_ao12n" }
    > find cell cs_ao12n*c
    > hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
    > hide -clear -cells { "cs_ao21n" }
    > find cell cs_ao21n*c

```

```

> hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*c
> hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*c
> hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*c
> hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*c
> hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
> hide -clear -cells { "cs_buffe" }
> find cell cs_buffe*
> hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*c
> hide -clear -cells {cs_xbo2n01c cs_xbo2n02c cs_xbo2n03c ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*c
> hide -clear -cells {cs_xbn2n01c cs_xbn2n02c cs_xbn2n03c ...

```

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/dll-rs6000/hier.dll
 hier.dll version 4.1 (Apr 14 1999 17:21:46)

BooleDozer Hierarchical Timing Correction

```

> scritflow {trestructure_tree( MAX_INPUTS( 16 ) MAX_DECOM...

```

[critflow]: Compiled on Mar 10 1999 at 07:07:06.

```

[critflow]: trestructure_tree( MAX_INPUTS( 16 ) MAX_DECOMPOSE( 4 ) SORT_PINS CHECK_INPUTS
MIN_INPUTS( 2 ) )

```

[trestructure]: Thresholds: Inputs=2 Slack=-0.000

[trestructure]: MaxInputs=16 MaxDecompose=4 DoubleInverters=true

[trestructure]: SortPins=true ReduceArea=false

[trestructure]: CheckInputs=true PartialTrees=false

[trestructure]: IgnoreHideFlags=false TibOnly=false

[trestructure]: MatchEffort=2 DebugNet=none

[trestructure]: Compiled on Apr 13 1999 at 18:34:22.

[critflow]: Critical Slack = -1955.134

[padnet]: Compiled on Mar 10 1999 at 05:18:12.

[padnet]: Added 9 IOPADs.

```

[
>>]: nextbox( genmark() );

```

```

[
>>]: nextnet( geninv() );

```

```

[
>>]: nextbox( twoin() onein() invrem() );

```

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 24 signals, 14 usage boxes and 22 connections.

[unpadnet]: Compiled on Mar 10 1999 at 05:21:34.

[unpadnet]: Removed 9 IOPADs.

[cleanup]: 2 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 13 signals, 3 usage boxes and 11 connections.

[Hdecompose]: Inserted 11 pairs of double inverters.

[ET-0203]: Timing top level created for design: SINGLE_SINK_INFO, analysis mode: default.

[ET-0112]: Deleting timing for design: SINGLE_SINK_INFO, analysis mode: default, and below.

[Hdecompose]: Single Sink: Load=12.000 Delay=0.000

[Hdecompose]: Max Inputs: 4

[Hdecompose]: Stage Delay: AND=144.431 XOR=259.360

[cleanup]: 49 boxes disconnected

[sweep]: sweep deleted 38 signals and 5 usage boxes.

The model has 17 signals, 7 usage boxes and 15 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(1)

[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(0)

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode: default, and below.

[padnet]: Added 7 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 22 signals, 14 usage boxes and 20 connections.

[unpadnet]: Removed 7 IOPADs.

[cleanup]: 4 boxes disconnected

[sweep]: sweep deleted 4 signals and 0 usage boxes.

The model has 11 signals, 3 usage boxes and 9 connections.

[Hdecompose]: Inserted 5 pairs of double inverters.

[cleanup]: 50 boxes disconnected

[sweep]: sweep deleted 32 signals and 2 usage boxes.

The model has 13 signals, 5 usage boxes and 11 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input ireg_valid&0

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode: default, and below.

[padnet]: Added 7 IOPADs.

[

>>]: nextbox(genmark());

[

```

>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
        The model has 20 signals; 12 usage boxes and 18 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
        The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 9 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 31 signals and 6 usage boxes.
        The model has 18 signals, 10 usage boxes and 16 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input op_cmp_raw&0

[trestructure]: (W) Covering is invalid due to electrical violation at input frc_blk_1cyc_q

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 3 IOPADs.
[
>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 8 signals, 4 usage boxes and 6 connections.
[unpadnet]: Removed 3 IOPADs.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 5 signals, 1 usage boxes and 3 connections.
[Hdecompose]: Inserted 3 pairs of double inverters.
[cleanup]: 7 boxes disconnected
[sweep]: sweep deleted 6 signals and 0 usage boxes.
        The model has 5 signals, 1 usage boxes and 3 connections.
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 4 IOPADs.
[

```

```

>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
      The model has 12 signals, 7 usage boxes and 10 connections.
[unpadnet]: Removed 4 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
      The model has 6 signals, 1 usage boxes and 4 connections.
[Hdecompose]: Inserted 4 pairs of double inverters.
[cleanup]: 16 boxes disconnected
[sweep]: sweep deleted 12 signals and 2 usage boxes.
      The model has 8 signals, 3 usage boxes and 6 connections.
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 14 IOPADs.
[
>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 3 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 9 signals and 6 usage boxes.
      The model has 42 signals, 27 usage boxes and 40 connections.
[unpadnet]: Removed 14 IOPADs.
[cleanup]: 4 boxes disconnected
[sweep]: sweep deleted 4 signals and 0 usage boxes.
      The model has 24 signals, 9 usage boxes and 22 connections.
[Hdecompose]: Inserted 20 pairs of double inverters.
[cleanup]: 92 boxes disconnected
[sweep]: sweep deleted 66 signals and 5 usage boxes.
      The model has 28 signals, 13 usage boxes and 26 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input op_dsbl_before&0

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[trestructure]: Rebuilt 0 logic trees

```


[trestructure]: Execution time was 38.6 seconds.

> sweep

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1142 signals, 919 usage boxes and 1757 connections.

```
> hide -clear -cells { "cs_invvn" }
> find cell cs_invvn*
> hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...
> hide -clear -cells { "cs_nnd2n" }
> find cell cs_nnd2n*
> hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...
> hide -clear -cells { "cs_nnd3n" }
> find cell cs_nnd3n*
> hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
> hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*
> hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
> hide -clear -cells { "cs_nor2n" }
> find cell cs_nor2n*
> hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
> hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*
> hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*
> hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*
> hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*
> hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*
> hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*
> hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*
> hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
> hide -clear -cells { "cs_buffe" }
> find cell cs_buffe*
> hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*
> hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*
> hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
> hide -clear -cells { cs_ao12f }
> find cell cs_ao12f*
> hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
> hide -clear -cells { cs_nnd2f cs_nnd2w }
> find cell cs_nnd2f*
> hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
```

```

> find cell cs_nnd2w*
> hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
> hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
> find cell cs_nnd3f*
> hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
> find cell cs_nnd3h*
> hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
> find cell cs_nnd3w*
> hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
> find cell cs_nnd3y*
> hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
> hide -clear -cells { cs_nor2f cs_nor2w }
> find cell cs_nor2f*
> hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...
> find cell cs_nor2w*
> hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...
> hide -clear -cells { cs_nor3f cs_nor3h }
> find cell cs_nor3f*
> hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
> find cell cs_nor3h*
> hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
> hide -clear -cells { cs_oa12f }
> find cell cs_oa12f*
> hide -clear -cells {cs_oa12f03b cs_oa12f03c cs_oa12f03d ...
> hide -clear -cells { "cs_invvv" }
> find cell cs_invvv*
> hide -clear -cells {cs_invvv01b cs_invvv01c cs_invvv01d ...
> hide -clear -cells { cs_ao12v cs_ao12g }
> find cell cs_ao12v*
> hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
> find cell cs_ao12g*
> hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
> hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
> find cell cs_nnd2v*
> hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
> find cell cs_nnd2g*
> hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
> find cell cs_nnd2x*
> hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
> hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
> find cell cs_nnd3v*
> hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
> find cell cs_nnd3g*
> hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
> find cell cs_nnd3i*
> hide -clear -cells {cs_nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
> find cell cs_nnd3x*
> hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
> find cell cs_nnd3z*
> hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
> hide -clear -cells { cs_nnd4v }
> find cell cs_nnd4v*
> hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
> hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
> find cell cs_nor2v*

```

```

> hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
> find cell cs_nor2g*
> hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
> find cell cs_nor2x*
> hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
> hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
> find cell cs_nor3v*
> hide -clear -cells {cs_nor3v03b cs_nor3v03c cs_nor3v03d ...
> find cell cs_nor3g*
> hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...
> find cell cs_nor3i*
> hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
> hide -clear -cells { cs_oa12v cs_oa12g }
> find cell cs_oa12v*
> hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
> find cell cs_oa12g*
> hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
> critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
> critical tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,UP...
critical( tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,UP,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tsteal]: CMVC version 1.24 compiled on Apr 13 1999 at 18:28:20.
[tsteal]: setting SCORE option to ALL.
[tsteal]: setting RE_POWER option.
[tsteal]: setting FASTEST mode.
[tsteal]: setting SORT_PINS option.
[tsteal]: setting UP option.
[tsteal]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tsteal]: tsteal applied 0 times
[tsteal]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
> critical tpushl(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO...
critical( tpushl(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tpushl]: CMVC version 1.16 Compiled on Apr 1 1999 at 05:20:40.
[tpushl]: setting SCORE option to ALL.
[tpushl]: setting RE_POWER option.
[tpushl]: setting FASTEST mode.

```

```

[tpushl]: setting SORT_PINS option.
[tpushl]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tpushl]: applied 0 times
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > critical tpushr(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO...
critical( tpushr(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tpushr]: CMVC version 1.17 compiled on Mar 31 1999 at 11:36:43.
[tpushr]: setting SCORE option to ALL.
[tpushr]: setting RE_POWER option.
[tpushr]: setting FASTEST mode.
[tpushr]: setting SORT_PINS option.
[tpushr]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tpushr]: applied 0 times
[tpushr eval]: Execution time was 0.0 seconds.
[tpushr exec]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > critical tpushb(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO...
critical( tpushb(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tpushb]: CMVC version 1.15 compiled on Mar 31 1999 at 11:36:11.
[tpushb]: setting SCORE option to ALL.
[tpushb]: setting RE_POWER option.
[tpushb]: setting FASTEST mode.
[tpushb]: setting SORT_PINS option.
[tpushb]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tpushb]: applied 0 times
[tpushb eval]: Execution time was 0.5 seconds.
[tpushb exec]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > critical {texpand(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_...
critical( {texpand(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,SIMILAR,
VIEW(TRUE_BASE_AUTOGEN),NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[txpand]: setting SCORE option to ALL.
[txpand]: setting PUSH option.
[txpand]: setting RE_POWER option.
[txpand]: setting FASTEST mode.
[txpand]: setting SORT_PINS option.
[txpand]: setting SIMILAR option.
[txpand]: explicit VIEWS used.
[txpand]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47

```

[texpand]: TRULE view TRULE_BASE_AUTOGEN was found.

-1955.13 Avg: -188.47

ArrayNum: 6 ArrayMax: 919

Pattern hint flag is inactive

[cleanup]: 0 boxes disconnected

[texpand]: Execution time was 0.0 seconds.

[BD-502600]: 0 gates checked and 0 expanded.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical {texpand(SCORE(ALL),PUSH,COMPLEMENT,RE_POWER,FA...

critical(texpand(SCORE(ALL),PUSH,COMPLEMENT,RE_POWER,FASTEST,SORT_PINS,SIMILAR,
VIEW(TRULE_BASE_AUTOGEN),NO_VIOLATIONS));

-1955.13 Avg: -188.47

maximum area for proto box IDCDSUC is 4648

[texpand]: setting SCORE option to ALL.

[texpand]: setting PUSH option.

[texpand]: setting COMPLEMENT option.

[texpand]: setting RE_POWER option.

[texpand]: setting FASTEST mode.

[texpand]: setting SORT_PINS option.

[texpand]: setting SIMILAR option.

[texpand]: explicit VIEWs used.

[texpand]: setting NO_VIOLATIONS option.

-1955.13 Avg: -188.47

[texpand]: TRULE view TRULE_BASE_AUTOGEN was found.

-1955.13 Avg: -188.47

ArrayNum: 6 ArrayMax: 919

Pattern hint flag is inactive

[cleanup]: 0 boxes disconnected

[texpand]: Execution time was 0.0 seconds.

[BD-502600]: 0 gates checked and 0 expanded.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical {texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PI...

critical(texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS));

-1955.13 Avg: -188.47

maximum area for proto box IDCDSUC is 4648

[texpao]: CMVC version 1.9 compiled on Mar 31 1999 at 11:28:36.

-1955.13 Avg: -188.47

-1955.13 Avg: -188.47

ArrayNum: 6 ArrayMax: 919

[texpao]: applied 0 times

[texpao]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical {tbmove(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,M...

critical(tbmove(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,MULTIPLE_CRITICAL;
INVERTC,CLONE,NO_VIOLATIONS));

-1955.13 Avg: -188.47

maximum area for proto box IDCDSUC is 4648

[tbmove]: CMVC version 1.28 compiled on Apr 13 1999 at 18:25:40.

[tbmove]: setting SCORE option to ALL.

[tbmove]: setting RE_POWER option.

[tbmove]: setting FASTEST mode.

[tbmove]: setting SORT_PINS option.

[tbmove]: setting MULTIPLE_CRITICAL option.

[tbmove]: setting INVERTC option.

[tbmove]: setting CLONE option.

```

[tbmove]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
[tbmove]: WORST SLACK in this network: -1955.18
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tbmove_analysis]: working on box C167.
[tbmove_match_qualify]: box is hidden
[tbmove_match_pattern]: boxC is rejected.
[tbmove_analysis]: working on box C1952.
[tbmove_match_qualify]: boxD def box not base type or complement
[tbmove_match_qualify]: boxD def box not base type or complement
[[tbmove]]: 1 sinks moved to clone TBMOVE.
[tbmove_match_qualify]: boxC def box not base type or complementary base type
[tbmove_match_pattern]: boxC is rejected.
[tbmove_analysis]: working on box C2487.
[tbmove_match_pattern]: critB array max increased to 64
[tbmove_match_pattern]: boxB has 1 input.
[tbmove_match_pattern]: critA array max increased to 64
[tbmove_match_pattern]: boxA is rejected.
[tbmove_analysis]: working on box C2738.
[tbmove_match_qualify]: box is hidden
[tbmove_match_qualify]: box is hidden
[[tbmove]]: 1 sinks moved to clone TBMOVE.
[tbmove_save_arrays]: save arrays box max increased to 256
[tbmove_save_arrays]: save arrays pin max increased to 256
[tbmove_analysis]: before transform.
y:N675<3> = C2738:cs_nnd2n14b (a:last_cycle , b:N1692 )
y:N1692<4> = C2725rwr:cs_nnd2n14e (a:N1479 , b:N1681 )
y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892 , b:N1858 , c:N1497 )
[tbmove]: 1 boundary move
[tbmove_analysis]: after transform.
y:N1689<2> = C2742:cs_nnd3f02c (a:N1652 , b:N1479&0 , c:N675 )
y:N648<1> = C2743:cs_nnd3f02c (a:N675 , b:N1479&0 , c:N1862 )
y:N2086&0<7> = C2744:cs_nnd2f13c (a:N675 , b:N1479&0 )
y:N675&0<1> = TBMOVE:cs_nnd2n14b (a:last_cycle , b:N1692 )
y:N675<3> = C2738:cs_nnd2n14b (a:N1692&0 , b:last_cycle )
y:N1692<3> = C2725rwr:cs_nnd2n14e (a:N1479 , b:N1681 )
y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892 , b:N1858 , c:N1497 )
y:N1479&0<3> = TBMOVE799:cs_nnd4n06c (a:N1858 , b:N1497 , c:last_cycle
, d:N892 )
y:N1692&0<1> = TBMOVE798:cs_inwv07c (a:N1681 )
[tbmove_analysis]: original
slack=-1955.1339,new_total_slack=-1881.8721,old_slack=-1955.1339,new_slack=-382.4436
[tbmove_analysis]: transform_cost = 9999 transform_slack = -1955.1339 restore flag 1 violation 1
[tbmove_analysis]: before restore arrays.
[tbmove_analysis]: save_box_array[ 0 ]
y:N1689<2> = C2742:cs_nnd3f02c (a:N1652 , b:- , c:N675 )
[tbmove_analysis]: save_box_array[ 1 ]
y:N648<1> = C2743:cs_nnd3f02c (a:N675 , b:- , c:N1862 )
[tbmove_analysis]: save_box_array[ 2 ]
y:N2086&0<7> = C2744:cs_nnd2f13c (a:N675 , b:N1479 )
[tbmove_analysis]: save_box_array[ 3 ]
y:N675&0<1> = TBMOVE:cs_nnd2n14b (a:last_cycle , b:N1692 )
[tbmove_analysis]: save_box_array[ 4 ]
y:N675<3> = C2738:cs_nnd2n14b (a:N1692 , b:last_cycle )

```

```

[tbmove_analysis]: save_box_array[ 5 ]
y:N1692<4> = C2725rwr:cs_nnd2n14e (a:N1479 , b:N1681 )
[tbmove_analysis]: save_box_array[ 6 ]
y:N1479<3> = C2721rwr:cs_nnd3n12b (a:N892 , b:N1858 , c:N1497 )
Unbinding usage[0] C2742 cs_nnd3f02c
Binding usage C2742 to cs_nnd2n02c
Unbinding usage[1] C2743 cs_nnd3f02c
Binding usage C2743 to cs_nnd2n02c
Unbinding usage[2] C2744 cs_nnd2f13c
Binding usage C2744 to cs_invvn13c
Unbinding usage[3] TBMOVE cs_nnd2n14b
Binding usage TBMOVE to cs_nnd2n14b
Unbinding usage[4] C2738 cs_nnd2n14b
Binding usage C2738 to cs_nnd2n14b
Unbinding usage[5] C2725rwr cs_nnd2n14e
Binding usage C2725rwr to cs_nnd2n14e
Unbinding usage[6] C2721rwr cs_nnd3n12b
Binding usage C2721rwr to cs_nnd3n12b
[tbmove_restore_arrays]: after deleting pins.
[tbmove_restore_arrays]: save_box_array[ 0 ]
y:N1689<2> = C2742:cs_nnd2n02c (a:N1652 , b:N675 )
[tbmove_restore_arrays]: save_box_array[ 1 ]
y:N648<1> = C2743:cs_nnd2n02c (a:N1862 , b:N675 )
[tbmove_restore_arrays]: save_box_array[ 2 ]
y:N2086<0><7> = C2744:cs_invvn13c (a:N675 )
[tbmove_restore_arrays]: save_box_array[ 3 ]
y:N675<0><1> = TBMOVE:cs_nnd2n14b (a:last_cycle , b:N1692 )
[tbmove_restore_arrays]: save_box_array[ 4 ]
y:N675<3> = C2738:cs_nnd2n14b (a:last_cycle , b:N1692 )
[tbmove_restore_arrays]: save_box_array[ 5 ]
y:N1692<4> = C2725rwr:cs_nnd2n14e (a:N1479 , b:N1681 )
[tbmove_restore_arrays]: save_box_array[ 6 ]
y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892 , b:N1858 , c:N1497 )
[tbmove_analysis]: after restoration.
y:N675<4> = C2738:cs_nnd2n14b (a:last_cycle , b:N1692 )
y:N1692<3> = C2725rwr:cs_nnd2n14e (a:N1479 , b:N1681 )
y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892 , b:N1858 , c:N1497 )
[tbmove]: C2738 <=
[tbmove]: slack = -1955.13
[tbmove]: slack = -1950.22
[tbmove_analysis]: slack = -382.44, old slack = -1955.13, cost = 35.
[tbmove_analysis]: working on box BOX679.
[tbmove_match_pattern]: boxC is rejected.
[tbmove_analysis]: working on box BOX714.
[tbmove_match_pattern]: boxC is rejected.
[tbmove]: tbmove applied 0 times
[tbmove eval]: Execution time was 0.6 seconds.
[tbmove exec]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > critical tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,DO...
critical( tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,DOWN,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tsteal]: setting SCORE option to ALL.
[tsteal]: setting RE_POWER option.

```

```

[tsreal]: setting FASTEST mode.
[tsreal]: setting SORT_PINS option.
[tsreal]: setting DOWN option.
[tsreal]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tsreal]: tsreal applied 0 times
[tsreal]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > critical tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tnc...
critical( tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tncube(SCORE(ALL),NO_VIOLATIONS)
);
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
setting SCORE option to ALL.
setting ACTUAL option.
setting ORD2 option.
setting NO_VIOLATIONS option.
[tncube]: CMVC version 1.11 compiled on Mar 31 1999 at 11:35:50.
[tncube]: setting SCORE option to ALL.
[tncube]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[tncube]: 0 pins swapped in 0 chains of gates
[tncube]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
    > repower_paths FUZZY(0.02)
initial slack is -1955
after repower paths slack is -1955
    > repower_paths {FUZZY(0.02), SIMULTANEOUS_REPOWER}
initial slack is -1955
after repower paths slack is -1955
    > critical {repower(SCORE(ALL),FASTEST,NO_VIOLATIONS), rep...
critical( repower(SCORE(ALL),FASTEST,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1955.13 Avg: -188.11
maximum area for proto box IDCDSUC is 4656
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.11
ArrayNum: 6 ArrayMax: 919
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
    > critical clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIO...

```


critical(clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS));

-1955.13 Avg: -188.11

maximum area for proto box IDCDSUC is 4656

setting SCORE option to ALL.

setting ACTUAL option.

setting RE_POWER option.

setting FASTEST mode.

setting NO_VIOLATIONS option.

-1955.13 Avg: -188.11

ArrayNum: 6 ArrayMax: 919

[BD-500100]: 0 parallel copies of gates were made.

[clone]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical {onebuff(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATI...

critical(onebuff(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS),

dinv(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS));

-1955.13 Avg: -188.11

maximum area for proto box IDCDSUC is 4656

[onebuff]: setting SCORE option to ALL.

[onebuff]: setting RE_POWER option.

[onebuff]: setting FASTEST mode.

[onebuff]: setting NO_VIOLATIONS option.

-1955.13 Avg: -188.11

setting SCORE option to ALL.

setting RE_POWER option.

setting FASTEST mode.

setting NO_VIOLATIONS option.

-1955.13 Avg: -188.11

-1955.13 Avg: -188.11

ArrayNum: 6 ArrayMax: 919

[onebuff]: was applied 0 times

[BD-500500]: Moved 0 sinks and removed 0 inverters.

[BD-502000]: Called transforms 12 times and applied 0 of them.

> critical tcte(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS)

critical(tcte(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS));

-1955.13 Avg: -188.11

maximum area for proto box IDCDSUC is 4656

-1955.13 Avg: -188.11

-1955.13 Avg: -188.11

ArrayNum: 6 ArrayMax: 919

[BD-502200]: Combined 0 gates.

[tcte]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical speedreg(RE_POWER),absrbreg()

critical(speedreg(RE_POWER),absrbreg());

-1955.13 Avg: -188.11

maximum area for proto box IDCDSUC is 4656

[speedreg]: Compiled on Mar 31 1999 at 11:35:02.

[BD-500000]: absrbreg CMVC version 1.9 compiled on Apr 13 1999 at 18:19:51

-1955.13 Avg: -188.11

ArrayNum: 6 ArrayMax: 919

[speedreg]: 0 registers checked 0 changed

[BD-502800]: 0 registers checked 0 absorbed logic.

[absrbreg]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 12 times and applied 0 of them.

```

> noncritical speedreg(RE_POWER),absrbreg()
[noncritical]: CMVC version 1.17 compiled on Mar 31 1999 at 11:26:31.
maximum area for proto box IDCDSUC is 4656
-1955.13 Avg: -188.11
[noncritical]: noncritical applied to boxes with slack > -0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -188.01
[speedreg]: 263 registers checked 28 changed
[BD-502800]: 0 registers checked 0 absorbed logic.
[absrbreg]: Execution time was 0.0 seconds.
> hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
> hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao...
> hide -no_clear -cells { cs_buffe }
> hide -no_clear -cells { cs_invv n cs_invv v }
> hide -no_clear -cells { cs_nnd2f cs_nnd2g cs_nnd2n cs_nn...
> hide -no_clear -cells { cs_nnd3f cs_nnd3g cs_nnd3h cs_nn...
> hide -no_clear -cells { cs_nnd4n cs_nnd4v }
> hide -no_clear -cells { cs_nor2f cs_nor2g cs_nor2n cs_no...
> hide -no_clear -cells { cs_nor3f cs_nor3g cs_nor3h cs_no...
> hide -no_clear -cells { cs_oa12f cs_oa12g cs_oa12n cs_oa...
> hide -no_clear -cells { cs_oa21n cs_oa21v }
> hide -no_clear -cells { cs_oa22n cs_oa22v }
> hide -no_clear -cells { cs_xbn2n cs_xbn2v }
> hide -no_clear -cells { cs_xbo2n cs_xbo2v }
> find cell cs_*
> hide -no_clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f0...
> find cell cs_buffe*
> hide -no_clear -cells {cs_buffe01a cs_buffe02a cs_buffe0...
> hide -clear -cells { "cs_invv n" }
> find cell cs_invv n*c
> hide -clear -cells {cs_invv n01c cs_invv n02c cs_invv n03c ...
> hide -clear -cells { "cs_nnd2n" }
> find cell cs_nnd2n*c
> hide -clear -cells {cs_nnd2n02c cs_nnd2n03c cs_nnd2n04c ...
> hide -clear -cells { "cs_nnd3n" }
> find cell cs_nnd3n*c
> hide -clear -cells {cs_nnd3n02c cs_nnd3n03c cs_nnd3n04c ...
> hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*c
> hide -clear -cells {cs_nnd4n03c cs_nnd4n04c cs_nnd4n05c ...
> hide -clear -cells { "cs_nor2n" }
> find cell cs_nor2n*c
> hide -clear -cells {cs_nor2n02c cs_nor2n03c cs_nor2n04c ...
> hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*c
> hide -clear -cells {cs_nor3n03c cs_nor3n04c cs_nor3n05c ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*c
> hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*c
> hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*c

```

```

> hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*c
> hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*c
> hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*c
> hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
> hide -clear -cells { "cs_buffe" }
> find cell cs_buffe*
> hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*c
> hide -clear -cells {cs_xbo2n01c cs_xbo2n02c cs_xbo2n03c ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*c
> hide -clear -cells {cs_xbn2n01c cs_xbn2n02c cs_xbn2n03c ...
> scritflow {trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMP...
[critflow]: trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS CHECK_INPUTS
MIN_INPUTS( 2 ) )
[trestructure]: Thresholds: Inputs=2 Slack=-0.000
[trestructure]: MaxInputs=4 MaxDecompose=4 DoubleInverters=true
[trestructure]: SortPins=true ReduceArea=false
[trestructure]: CheckInputs=true PartialTrees=false
[trestructure]: IgnoreHideFlags=false TibOnly=false
[trestructure]: MatchEffort=2 DebugNet=none
[critflow]: Critical Slack = -1955.134
[padnet]: Added 9 IOPADs.
[
>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin().onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 24 signals, 14 usage boxes and 22 connections.
[unpadnet]: Removed 9 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
The model has 13 signals, 3 usage boxes and 11 connections.
[Hdecompose]: Inserted 11 pairs of double inverters.
[cleanup]: 49 boxes disconnected
[sweep]: sweep deleted 38 signals and 5 usage boxes.
The model has 17 signals, 7 usage boxes and 15 connections.

```

[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(1)

[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(0)

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 7 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

using pattern information

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 22 signals, 14 usage boxes and 20 connections.

[unpadnet]: Removed 7 IOPADs.

[cleanup]: 4 boxes disconnected

[sweep]: sweep deleted 4 signals and 0 usage boxes.

The model has 11 signals, 3 usage boxes and 9 connections.

[Hdecompose]: Inserted 5 pairs of double inverters.

[cleanup]: 50 boxes disconnected

[sweep]: sweep deleted 32 signals and 2 usage boxes.

The model has 13 signals, 5 usage boxes and 11 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input ireg_valid&0

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 7 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

using pattern information

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 20 signals, 12 usage boxes and 18 connections.

[unpadnet]: Removed 7 IOPADs.

[cleanup]: 2 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 11 signals, 3 usage boxes and 9 connections.

[Hdecompose]: Inserted 9 pairs of double inverters.

[cleanup]: 50 boxes disconnected

[sweep]: sweep deleted 31 signals and 6 usage boxes.

The model has 18 signals, 10 usage boxes and 16 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input op_cmp_raw&0

[trestructure]: (W) Covering is invalid due to electrical violation at input frc_blk_1cyc_q

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 3 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

using pattern information

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 8 signals, 4 usage boxes and 6 connections.

[unpadnet]: Removed 3 IOPADs.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 5 signals, 1 usage boxes and 3 connections.

[Hdecompose]: Inserted 3 pairs of double inverters.

[cleanup]: 7 boxes disconnected

[sweep]: sweep deleted 6 signals and 0 usage boxes.

The model has 5 signals, 1 usage boxes and 3 connections.

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 4 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

using pattern information

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 12 signals, 7 usage boxes and 10 connections.

[unpadnet]: Removed 4 IOPADs.

[cleanup]: 2 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 6 signals, 1 usage boxes and 4 connections.

[Hdecompose]: Inserted 4 pairs of double inverters.

[cleanup]: 16 boxes disconnected

[sweep]: sweep deleted 12 signals and 2 usage boxes.

The model has 8 signals, 3 usage boxes and 6 connections.

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 9 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

using pattern information

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 1 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 2 signals and 2 usage boxes.

The model has 27 signals, 17 usage boxes and 25 connections.

[unpadnet]: Removed 9 IOPADs.

[cleanup]: 2 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 16 signals, 6 usage boxes and 14 connections.

[Hdecompose]: Inserted 10 pairs of double inverters.

[cleanup]: 62 boxes disconnected

[sweep]: sweep deleted 42 signals and 8 usage boxes.

The model has 20 signals, 10 usage boxes and 18 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input op_dsbl_before&0

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[trestructure]: Rebuilt 0 logic trees

[trestructure]: Execution time was 31.8 seconds.

> sweep

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1142 signals, 919 usage boxes and 1757 connections.

> hide -clear -cells { "cs_invvn" }

> find cell cs_invvn*

> hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...

> hide -clear -cells { "cs_nnd2n" }

> find cell cs_nnd2n*

> hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...

```

> hide -clear -cells { "cs_nnd3n" }
> find cell cs_nnd3n*
> hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
> hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*
> hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
> hide -clear -cells { "cs_nor2n" }
> find cell cs_nor2n*
> hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
> hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*
> hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*
> hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*
> hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*
> hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
> hide -clear -cells { "cs_oa12n" }
> find cell cs_oa12n*
> hide -clear -cells {cs_oa12n03b cs_oa12n03c cs_oa12n03d ...
> hide -clear -cells { "cs_oa21n" }
> find cell cs_oa21n*
> hide -clear -cells {cs_oa21n03b cs_oa21n03c cs_oa21n03d ...
> hide -clear -cells { "cs_oa22n" }
> find cell cs_oa22n*
> hide -clear -cells {cs_oa22n03b cs_oa22n03c cs_oa22n03d ...
> hide -clear -cells { "cs_buiffe" }
> find cell cs_buiffe*
> hide -clear -cells {cs_buiffe01a cs_buiffe02a cs_buiffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*
> hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*
> hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
> hide -clear -cells { cs_ao12f }
> find cell cs_ao12f*
> hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
> hide -clear -cells { cs_nnd2f cs_nnd2w }
> find cell cs_nnd2f*
> hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
> find cell cs_nnd2w*
> hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
> hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
> find cell cs_nnd3f*
> hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
> find cell cs_nnd3h*
> hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
> find cell cs_nnd3w*
> hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
> find cell cs_nnd3y*

```

```

> hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
> hide -clear -cells { cs_nor2f cs_nor2w }
> find cell cs_nor2f*
> hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...
> find cell cs_nor2w*
> hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...
> hide -clear -cells { cs_nor3f cs_nor3h }
> find cell cs_nor3f*
> hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
> find cell cs_nor3h*
> hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
> hide -clear -cells { cs_oa12f }
> find cell cs_oa12f*
> hide -clear -cells {cs_oa12f03b cs_oa12f03c cs_oa12f03d ...
> hide -clear -cells { "cs_invvv" }
> find cell cs_invvv*
> hide -clear -cells {cs_invvv01b cs_invvv01c cs_invvv01d ...
> hide -clear -cells { cs_ao12v cs_ao12g }
> find cell cs_ao12v*
> hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
> find cell cs_ao12g*
> hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
> hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
> find cell cs_nnd2v*
> hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
> find cell cs_nnd2g*
> hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
> find cell cs_nnd2x*
> hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
> hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
> find cell cs_nnd3v*
> hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
> find cell cs_nnd3g*
> hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
> find cell cs_nnd3i*
> hide -clear -cells {cs_nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
> find cell cs_nnd3x*
> hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
> find cell cs_nnd3z*
> hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
> hide -clear -cells { cs_nnd4v }
> find cell cs_nnd4v*
> hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
> hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
> find cell cs_nor2v*
> hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
> find cell cs_nor2g*
> hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
> find cell cs_nor2x*
> hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
> hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
> find cell cs_nor3v*
> hide -clear -cells {cs_nor3v03b cs_nor3v03c cs_nor3v03d ...
> find cell cs_nor3g*
> hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...

```



```

> find cell cs_nor3i*
> hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
> hide -clear -cells { cs_oa12v cs_oa12g }
> find cell cs_oa12v*
> hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
> find cell cs_oa12g*
> hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
> compare_critical_slack_limit
-1955.13 Avg: -188.01
comparing new slack -1955.1339 to saved slack -1935.5825
> tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
> noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
repower: setting SCORE option to ALL.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.01
maximum area for proto box IDCDSUC is 4656
-1955.13 Avg: -188.01
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -181.26
[BD-500026]: repower was applied 73 times.
[repower]: Execution time was 5.7 seconds.
> tc_parm MARGIN(10000000)
> fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}
[
>>]: ltorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.26
[BD-500300]: 16 pins on 7 gates swapped.
-1955.13 Avg: -181.16
[fanmatch]: Execution time was 3.6 seconds.
> tc_parm OFFSET(0)
> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
> tc_parm REGALL
> repower_paths FUZZY(0.02)
initial slack is -1955
after repower paths slack is -1955
> critical {repower(SCORE(ALL ),FASTEST ,NO_VIOLATIONS)...
critical( repower(SCORE(ALL ),FASTEST ,NO_VIOLATIONS),
repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1955.13 Avg: -181.15
maximum area for proto box IDCDSUC is 4655
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO_VIOLATIONS option.

```

repower: setting SCORE option to ALL.
 repower: setting FASTEST mode.
 repower: setting NO_VIOLATIONS option.
 -1955.13 Avg: -181.15
 ArrayNum: 6 ArrayMax: 919
 [BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.1 seconds.
 [BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.1 seconds.
 [BD-502000]: Called transforms 12 times and applied 0 of them.
 > compare_critical_slack_limit
 -1955.13 Avg: -181.15
 comparing new slack -1955.1339 to saved slack -1935.5825
 > measure

The model <IDCDSUC> has:

Primary Inputs = 122
 Primary Outputs = 73
 Primary BIDs = 0
 Signals = 1142
 Gate Count = 919
 Connections = 1757
 Master REG Bits = 83
 Slave REG Bits = 83
 Internal Area = 4655
 External Area = 0
 Gates/Connects = 0.523051
 Fanout Count = 1757
 Average Fanout = 1.538529
 Avg Tech Box Size = 5.065288
 Tech Box Size Stddev = 0.010915
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 767
 Real boxes = 544
 Real connections = 1382
 Real LSTs = 2149
 Real ICells/box = 8.556985
 Real LSTs/box = 3.950368
 Real nets/box = 1.409926

Cell Total
 Each Cell

Type	Cnt	Boxname	Power Level	Function	Int	Ext	Power	Int	Ext	Power
6		cs_ao22n03c	03c	> AOI	6	0	0.000	36	0	0.000
2		cs_ao12n03c	03c	> AOI	4	0	0.000	8	0	0.000
1		cs_ao12n10c	10c	> AOI	12	0	0.000	12	0	0.000
1		cs_ao22n04c	04c	> AOI	6	0	0.000	6	0	0.000
1		cs_ao22n10c	10c	> AOI	18	0	0.000	18	0	0.000
1		cs_ao12n05c	05c	> AOI	6	0	0.000	6	0	0.000
180		BRKPT	>	BRKPT	0	0	0.000	0	0	0.000
195		IOPAD	>	IOPAD	0	0	0.000	0	0	0.000
144		cs_nnd2n02c	02c	> NAND	3	0	0.000	432	0	0.000
17		cs_nnd2n04c	04c	> NAND	3	0	0.000	51	0	0.000

1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
4	cs_nnd2n12c	12c	>	NAND	12	0	0.000	48	0	0.000
19	cs_nnd3n02c	02c	>	NAND	4	0	0.000	76	0	0.000
3	cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
2	cs_nnd3n03c	03c	>	NAND	4	0	0.000	8	0	0.000
3	cs_nnd2n11c	11c	>	NAND	11	0	0.000	33	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
2	cs_nnd2n14e	14e	>	NAND	19	0	0.000	38	0	0.000
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12b	12b	>	NAND	22	0	0.000	22	0	0.000
2	cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
1	cs_nnd2n08c	08c	>	NAND	7	0	0.000	7	0	0.000
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
8	cs_nor2n02c	02c	>	NOR	3	0	0.000	24	0	0.000
3	cs_nor2n04c	04c	>	NOR	3	0	0.000	9	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
60	cs_invvn01c	01c	>	NOT	2	0	0.000	120	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
7	cs_invvn10c	10c	>	NOT	4	0	0.000	28	0	0.000
21	cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
6	cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
50	cs_invvn07c	07c	>	NOT	2	0	0.000	100	0	0.000
5	cs_invvn15c	15c	>	NOT	10	0	0.000	50	0	0.000
6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvn19b	19b	>	NOT	28	0	0.000	28	0	0.000
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
5	cs_invvn02c	02c	>	NOT	2	0	0.000	10	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
10	cs_invvn04c	04c	>	NOT	2	0	0.000	20	0	0.000
8	cs_invvn05c	05c	>	NOT	2	0	0.000	16	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
1	cs_invvn16c	16c	>	NOT	14	0	0.000	14	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
22	cl_invvn07d	07d	>	REG	25	0	0.000	550	0	0.000
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000

2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of		
Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of		
Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
14	6	*****
15	9	*****
16	4	****
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	379	350* plus *****
2	202	200* plus **
3	35	*****
4	18	*****

The Histogram Of Fanout vs. Net

# of Fanout	Nets	
0	2	**
1	940	900* plus *****
2	97	50* plus *****
3	42	*****
4	17	*****
5	7	*****
6	11	*****
7	3	***
8	3	***
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds.

> critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...

critical(
repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED),faninv(LIMITED));

-1955.13 Avg: -181.15

maximum-area for proto box IDCDSUC is 4655

repower: setting SCORE option to ALL.

repower: setting INC mode.

repower: setting NO_VIOLATIONS option.

setting SCORE option to ALL.

setting ACTUAL option.

setting RE_POWER option.

setting INC mode.

setting NO_VIOLATIONS option.

fantom: Found 152 valid buffers or inverters.

[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.

[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.

-1955.13 Avg: -181.15

ArrayNum: 6 ArrayMax: 919

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.0 seconds.

[BD-500100]: 0 parallel copies of gates were made.

[clone]: Execution time was 0.0 seconds.

[BD-500700]: Added 0 buffers.

[fantom]: Execution time was 0.0 seconds.

[BD-500701]: Added 0 inverters.

[faninv]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 24 times and applied 0 of them.

> nextbox synexpand(XPANDVIEW)

[
>>]: nextbox(synexpand(XPANDVIEW));

[
>>]: nextbox(SASname(RESTORE));

[syndasname]: Restored 0 BRKPT net names

[syndasname]: Restored 189 REG and SEQUENTIAL output net names

[syndasname]: Execution time was 0.0 seconds.

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1142 signals, 919 usage boxes and 1757 connections.

```
[
>>]: nextbox( SASName(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
> measure
```

The model <IDCDSUC> has:

```
Primary Inputs      =      122
Primary Outputs     =       73
Primary BIDs        =       0
Signals             =     1142
Gate Count          =      919
Connections         =     1757
Master REG Bits     =       83
Slave REG Bits      =       83
Internal Area       =     4655
External Area       =       0
Gates/Connects     =     0.523051
Fanout Count        =     1757
Average Fanout      =     1.538529
Avg Tech Box Size   =     5.065288
Tech.Box Size Stddev =     0.010915
Power               =     0.000000
```

R-E-A-LS-T-A-T-I-S-T-I-C-S***

```
Real signals        =      767
Real boxes          =      544
Real connections    =     1382
Real LSTs           =     2149
Real ICells/box     =     8.556985
Real LSTs/box       =     3.950368
Real nets/box       =     1.409926
```

```
Cell              Total
Each              Cell
```

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
6	cs_ao22n03c	03c	>	AOI	6	0	0.000	36	0	0.000	
2	cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000	
1	cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000	
1	cs_ao22n04c	04c	>	AOI	6	0	0.000	6	0	0.000	
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000	
1	cs_ao12n05c	05c	>	AOI	6	0	0.000	6	0	0.000	
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
144	cs_nnd2n02c	02c	>	NAND	3	0	0.000	432	0	0.000	
17	cs_nnd2n04c	04c	>	NAND	3	0	0.000	51	0	0.000	
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000	
4	cs_nnd2n12c	12c	>	NAND	12	0	0.000	48	0	0.000	
19	cs_nnd3n02c	02c	>	NAND	4	0	0.000	76	0	0.000	
3	cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000	
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000	

2	cs_nnd3n03c	03c	>	NAND	4	0	0.000	8	0	0.000
3	cs_nnd2n11c	11c	>	NAND	11	0	0.000	33	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
2	cs_nnd2n14e	14e	>	NAND	19	0	0.000	38	0	0.000
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12b	12b	>	NAND	22	0	0.000	22	0	0.000
2	cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
1	cs_nnd2n08c	08c	>	NAND	7	0	0.000	7	0	0.000
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
8	cs_nor2n02c	02c	>	NOR	3	0	0.000	24	0	0.000
3	cs_nor2n04c	04c	>	NOR	3	0	0.000	9	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
60	cs_invvn01c	01c	>	NOT	2	0	0.000	120	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
7	cs_invvn10c	10c	>	NOT	4	0	0.000	28	0	0.000
21	cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
6	cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
50	cs_invvn07c	07c	>	NOT	2	0	0.000	100	0	0.000
5	cs_invvn15c	15c	>	NOT	10	0	0.000	50	0	0.000
6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvv19b	19b	>	NOT	28	0	0.000	28	0	0.000
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
5	cs_invvn02c	02c	>	NOT	2	0	0.000	10	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
10	cs_invvn04c	04c	>	NOT	2	0	0.000	20	0	0.000
8	cs_invvn05c	05c	>	NOT	2	0	0.000	16	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
1	cs_invvn16c	16c	>	NOT	14	0	0.000	14	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
22	cl_invvn07d	07d	>	REG	25	0	0.000	550	0	0.000
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000

1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of		
Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of		
Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
14	6	*****
15	9	*****
16	4	****
17	14	*****

The Histogram Of Fanin vs. Box

# of		
Fanin	Ops	
1	379	350* plus *****
2	202	200* plus **
3	35	*****
4	18	*****

The Histogram Of Fanout vs. Net

# of		
Fanout	Nets	
0	2	**


```

1  940  900* plus *****
2  97   50* plus *****
3  42   *****
4  17   *****
5  7    *****
6  11   *****
7  3    ***
8  3    ***
13 3    ***
14 16   *****
20 1    *

```

[End of measure]

[measure]: Execution time was 0.7 seconds.

> repower_paths FUZZY(0.02)

initial slack is -1955

after repower paths slack is -1955

> critical {repower(SCORE(ALL),FASTEST ,NO_VIOLATIONS)...

critical(repower(SCORE(ALL),FASTEST ,NO_VIOLATIONS),

repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA)));

-1955.13 Avg: -181.15

maximum area for proto box IDCDSUC is 4655

repower: setting SCORE option to ALL.

repower: setting FASTEST mode.

repower: setting NO_VIOLATIONS option.

repower: setting SCORE option to ALL.

repower: setting FASTEST mode.

repower: setting NO_VIOLATIONS option.

-1955.13 Avg: -181.15

ArrayNum: 6 ArrayMax: 919

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.1 seconds.

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.1 seconds.

[BD-502000]: Called transforms 12 times and applied 0 of them.

> write_end_point_report -points 3 -paths 1

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:03:06 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation

SlkCont

Slack due to a point downstream on path

Required Arrival Time

RAT

(ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT

(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

TIME)

Clock Gating Setup

ClkGSet

(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

ARRIVAL TIME + ADJUST)

Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 ARRIVAL TIME + ADJUST)
 Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 ADJUST)
 Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj
1 dcd_succ_last_t1	R C3+R	2954	-1955	3847	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	R C3+R	2954	-1955	3847	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2954	-1955	3847	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2954	-1955	3847	1011	1 cs_invv	01c NOT	
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1092	-1955	55	139	4 cs_invv	01c NOT	
1862 N675								
---->{a} C2738/y	F C3+R	1092	-1955	55	139	4 cs_nnd2n	14b NAND	
0 N675								
----> C2738/a	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14b NAND	
29 last_cycle								
---->{b} C2487/y	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14e NAND	
0 last_cycle								
----> C2487/b	F C3+R	1034	-1955	32	140	3 cs_nnd2n	14e NAND	
29 N1587								
----> C1952/y	F C3+R	1034	-1955	32	140	3 cs_invv	19b NOT	0
N1587								
----> C1952/a	R C3+R	1024	-1955	80	319	1 cs_invv	19b NOT	
10 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1955	80	319	1 IOPAD	IOPAD	
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1955	80	319	1 IOPAD	IOPAD	0
num_dcd_cyl(1)								
----> num_dcd_cyl(1)	R C3+R	1024	-1955	80	319	1 PI		0
num_dcd_cyl(1)								
2 dcd_succ_last_t1	F C3+R	2644	-1645	2362	1011	1 PO		0

dcdd_succ_last_t1	999	0					
RAT	F C3+R	2644	-1645	2362	1011	1 IOPAD	IOPAD
----> BOX714/OUT							
0 dcd_succ_last_t1	F C3+R	2644	-1645	2362	1011	1 IOPAD	IOPAD
----> BOX714/IN							
0 dcd_succ_last_t1&0	F C3+R	2644	-1645	2362	1011	1 cs_invrn	01c NOT
----> C167/y							
0 dcd_succ_last_t1&0	R C3+R	1208	-1645	92	139	4 cs_invrn	01c NOT
----> C167/a							
1436 N675	R C3+R	1208	-1645	92	139	4 cs_nnd2n	14b NAND
---->{a} C2738/y							
0 N675	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14b NAND
----> C2738/b							
56 N1692	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14e NAND
---->{b} C2725rwr/y							
0 N1692	R C3+R	1097	-1645	148	166	2 cs_nnd2n	14e NAND
----> C2725rwr/a							
56 N1479	R C3+R	1097	-1645	148	166	2 cs_nnd3n	12b NAND
---->{c} C2721rwr/y							
0 N1479	F C3+R	994	-1645	125	95	2 cs_nnd3n	12b NAND
----> C2721rwr/c							
102 N1497	F C3+R	994	-1645	125	95	2 cs_nor3n	10e NOR
---->{d} C2709rwr/y							
0 N1497	R C3+R	898	-1645	137	68	2 cs_nor3n	10e NOR
----> C2709rwr/c							
96 N1781	R C3+R	898	-1645	137	68	2 cs_nnd4n	10c NAND
---->{e} C2885/y							
0 N1781	F C3+R	825	-1645	44	50	1 cs_nnd4n	10c NAND
----> C2885/d							
73 N1997	F C3+R	825	-1645	44	50	1 cs_nnd2n	14c NAND
---->{f} C2886/y							
0 N1997	R C3+R	802	-1645	80	124	2 cs_nnd2n	14c NAND
----> C2886/a							
23 op_serialize&0	R C3+R	802	-1645	80	124	2 IOPAD	IOPAD
----> BOX638/OUT							
0 op_serialize&0	R C3+R	802	-1645	80	124	2 IOPAD	IOPAD 0
----> BOX638/IN							
op_serialize	R C3+R	802	-1645	80	124	2 PI	0
----> op_serialize							
op_serialize							

3 iu_reset_op_c_t1	R C3+R	2431	-1432	3912	1011	1 PO	0
iu_reset_op_c_t1							
RAT	999	0					
----> BOX716/OUT	R C3+R	2431	-1432	3912	1011	1 IOPAD	IOPAD
0 iu_reset_op_c_t1							
----> BOX716/IN	R C3+R	2431	-1432	3912	1044	3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0							
---->{a} C2393/y	R C3+R	2431	-1432	3912	1044	3 cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	473	-1432	78	137	3 cs_nnd2n	02c NAND
1958 gbfont_6							
----> gbfont_6/y	F C3+R	473	-1432	78	137	3 cs_invrn	09c NOT
gbfont_6							

```

----> gbfc0cell_6/a          R C3+R   410 -1432  217  43 1 cs_invrn  09c NOT
64 N2031
---->{b} C2162/y            R C3+R   410 -1432  217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b              F C3+R   303 -1432   57  49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R   303 -1432   57  49 3 cl_invrn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2        R C3+   160  N/C   60  222 13 cl_invrn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+   160  N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
> write_end_point_report -points 10
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:03:06 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 10

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time   RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup      ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold       ClkGHld      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width  ClkTPW      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                   Setup        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                     Hold          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle              EndOfC       ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth         ClkPW        ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
ClockSeparation         ClkSep       ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
Loop                     ALTest      ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
Arrival Time Limiting   ATLimit     Slack discontinuity due to failed test

```

```

-----
Num/                    LimitedAT/                    Delay/ Failed Test/
Test PinName            E Phase   AT   Slack   Slew   CL   FO Cell   P Func   T.Adj
NetName

```

```

--
1 dcd_succ_last_t1
dcd_succ_last_t1
RAT
----> BOX714/OUT
0 dcd_succ_last_t1
----> BOX714/IN
0 dcd_succ_last_t1&0
----> C167/y
0 dcd_succ_last_t1&0
----> C167/a
1862 N675
----> {a} C2738/y
0 N675
----> C2738/a
29 last_cycle
----> {b} C2487/y
0 last_cycle
----> C2487/b
29 N1587
----> C1952/y
N1587
----> C1952/a
10 num_dcd_cyl&0(1)
----> BOX679/OUT
0 num_dcd_cyl&0(1)
----> BOX679/IN
num_dcd_cyl(1)
----> num_dcd_cyl(1)
num_dcd_cyl(1)

```

```

R C3+R 2954 -1955 3847 1011 1 PO 0
999
R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
R C3+R 2954 -1955 3847 1011 1 cs_inwn 01c NOT
F C3+R 1092 -1955 55 139 4 cs_inwn 01c NOT
F C3+R 1092 -1955 55 139 4 cs_nnd2n 14b NAND
R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND
F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
F C3+R 1034 -1955 32 140 3 cs_invw 19b NOT 0
R C3+R 1024 -1955 80 319 1 cs_invw 19b NOT
R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
R C3+R 1024 -1955 80 319 1 PI 0

```

```

--
2 dcd_succ_last_t1
dcd_succ_last_t1
RAT
----> BOX714/OUT
0 dcd_succ_last_t1
----> BOX714/IN
0 dcd_succ_last_t1&0
----> C167/y
0 dcd_succ_last_t1&0
----> C167/a
1436 N675
----> {a} C2738/y
0 N675
----> C2738/b
56 N1692
----> {b} C2725rwr/y
0 N1692
----> C2725rwr/a
56 N1479
----> {c} C2721rwr/y
0 N1479
----> C2721rwr/c
102 N1497

```

```

F C3+R 2644 -1645 2362 1011 1 PO 0
999
F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
F C3+R 2644 -1645 2362 1011 1 cs_inwn 01c NOT
R C3+R 1208 -1645 92 139 4 cs_inwn 01c NOT
R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND
R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND
R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
F C3+R 994 -1645 125 95 2 cs_nnd3n 12b NAND

```

---->{d} C2709rwr/y
 0 N1497
 ----> C2709rwr/c
 96 N1781
 ---->{e} C2885/y
 0 N1781
 ----> C2885/d
 73 N1997
 ---->{f} C2886/y
 0 N1997
 ----> C2886/a
 23 op_serialize&0
 ----> BOX638/OUT
 0 op_serialize&0
 ----> BOX638/IN
 op_serialize
 ----> op_serialize
 op_serialize

F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
 R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR
 R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
 F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
 F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
 R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
 R C3+R 802 -1645 80 124 2 IOPAD IOPAD
 R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
 R C3+R 802 -1645 80 124 2 PI 0

3 iu_reset_op_c_t1
 iu_reset_op_c_t1
 RAT

----> BOX716/OUT
 0 iu_reset_op_c_t1
 ----> BOX716/IN
 0 iu_reset_op_c_t1&0
 ---->{a} C2393/y
 0 iu_reset_op_c_t1&0
 ----> C2393/a
 1958 gbfonet_6
 ----> gbfozell_6/y
 gbfonet_6
 ----> gbfozell_6/a
 64 N2031
 ---->{b} C2162/y
 0 N2031
 ----> C2162/b
 107 rcvry_reset_q
 ----> rcvry_reset.reg_n.lat_0/2_out_n
 0 rcvry_reset_q
 ----> rcvry_reset.reg_n.lat_0/c2
 143 slow_mode.c2_1
 ----> slow_mode.clockblock/c2
 0 slow_mode.c2_1

R C3+R 2431 -1432 3912 1011 1 PO 0
 999
 R C3+R 2431 -1432 3912 1011 1 IOPAD IOPAD
 R C3+R 2431 -1432 3912 1044 3 IOPAD IOPAD
 R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
 F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
 F C3+R 473 -1432 78 137 3 cs_invv n 09c NOT 0
 R C3+R 410 -1432 217 43 1 cs_invv n 09c NOT
 R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
 F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
 F C3+R 303 -1432 57 49 3 cl_invv n 07d SRL
 R C3+ 160 N/C 60 222 13 cl_invv n 07d SRL
 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB

4 local_milli_t2.reg_n.lat_0/a
 51 NET1056
 Setup local_milli_t2.reg_n.lat_0/c1
 1200 slow_mode.c1_4
 ---->{a} BOX789/y
 0 NET1056
 ----> BOX789/b
 55 NET1054

F C3+R 2675 -1366 103 92 3 cl_invv n 07c SRL
 F C3- 160 60 238 14 cl_invv n 07c
 F C3+R 2675 -1366 103 92 3 cs_nnd3z 07c NAND
 R C3+R 2620 -1366 139 36 1 cs_nnd3z 07c NAND

---->{b} BOX785/y	R C3+R	2620	-1366	139	36	1	cs_nnd2f	03c	NAND	
0 NET1054										
----> BOX785/a	F C3+R	2542	-1366	116	19	1	cs_nnd2f	03c	NAND	
78 N1866										
---->{c} C2555/y	F C3+R	2542	-1366	116	19	1	cs_ao12n	03c	AOI	
0 N1866										
----> C2555/b	R C3+R	2431	-1366	3912	1044	3	cs_ao12n	03c	AOI	
110 iu_reset_op_c_t1&0										
---->{d} C2393/y	R C3+R	2431	-1432	3912	1044	3	cs_nnd2n	02c	NAND	
0 iu_reset_op_c_t1&0										
----> C2393/a	F C3+R	473	-1432	78	137	3	cs_nnd2n	02c	NAND	
1958 gbfonet_6										
----> gbfozell_6/y	F C3+R	473	-1432	78	137	3	cs_invvn	09c	NOT	0
gbfonet_6										
----> gbfozell_6/a	R C3+R	410	-1432	217	43	1	cs_invvn	09c	NOT	
64 N2031										
---->{e} C2162/y	R C3+R	410	-1432	217	43	1	cs_nnd3n	02c	NAND	
0 N2031										
----> C2162/b	F C3+R	303	-1432	57	49	3	cs_nnd3n	02c	NAND	
107 rcvry_reset_q										
----> rcvry_reset.reg_n.lat_0/2_out_n	F C3+R	303	-1432	57	49	3	cl_invvn	07d	SRL	
0 rcvry_reset_q										
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_invvn	07d	SRL	
143 slow_mode.c2_1										
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB		
0 slow_mode.c2_1										
<hr/>										
5 local_milli_t1.reg_n.lat_0/a	F C3+R	2675	-1366	103	92	3	cl_invvn	07c	SRL	
51 NET1056										
Setup local_milli_t1.reg_n.lat_0/c1	F C3-	160		60	238	14	cl_invvn	07c		
1200 slow_mode.c1_4										
---->{a} BOX789/y	F C3+R	2675	-1366	103	92	3	cs_nnd3z	07c	NAND	
0 NET1056										
----> BOX789/b	R C3+R	2620	-1366	139	36	1	cs_nnd3z	07c	NAND	
55 NET1054										
---->{b} BOX785/y	R C3+R	2620	-1366	139	36	1	cs_nnd2f	03c	NAND	
0 NET1054										
----> BOX785/a	F C3+R	2542	-1366	116	19	1	cs_nnd2f	03c	NAND	
78 N1866										
---->{c} C2555/y	F C3+R	2542	-1366	116	19	1	cs_ao12n	03c	AOI	
0 N1866										
----> C2555/b	R C3+R	2431	-1366	3912	1044	3	cs_ao12n	03c	AOI	
110 iu_reset_op_c_t1&0										
---->{d} C2393/y	R C3+R	2431	-1432	3912	1044	3	cs_nnd2n	02c	NAND	
0 iu_reset_op_c_t1&0										
----> C2393/a	F C3+R	473	-1432	78	137	3	cs_nnd2n	02c	NAND	
1958 gbfonet_6										
----> gbfozell_6/y	F C3+R	473	-1432	78	137	3	cs_invvn	09c	NOT	0
gbfonet_6										
----> gbfozell_6/a	R C3+R	410	-1432	217	43	1	cs_invvn	09c	NOT	
64 N2031										
---->{e} C2162/y	R C3+R	410	-1432	217	43	1	cs_nnd3n	02c	NAND	
0 N2031										
----> C2162/b	F C3+R	303	-1432	57	49	3	cs_nnd3n	02c	NAND	

```

107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R    303 -1432   57  49 3 cl_invn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+      160   N/C   60  222 13 cl_invn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+      160   N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
   6 local_milli.reg_n.lat_0/a              F C3+R    2675 -1366   103  92 3 cl_invn  07c SRL
51 NET1056
Setup local_milli.reg_n.lat_0/c1           F C3-      160         60  238 14 cl_invn  07c    1200
slow_mode.c1_2
---->{a} BOX789/y                          F C3+R    2675 -1366   103  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/b                             R C3+R    2620 -1366   139  36 1 cs_nnd3z  07c NAND
55 NET1054
---->{b} BOX785/y                          R C3+R    2620 -1366   139  36 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                             F C3+R    2542 -1366   116  19 1 cs_nnd2f  03c NAND
78 N1866
---->{c} C2555/y                          F C3+R    2542 -1366   116  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                             R C3+R    2431 -1366  3912 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                          R C3+R    2431 -1432  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                             F C3+R    473 -1432   78  137 3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfozell_6/y                        F C3+R    473 -1432   78  137 3 cs_invn  09c NOT    0
gbfonet_6
----> gbfozell_6/a                        R C3+R    410 -1432   217  43 1 cs_invn  09c NOT
64 N2031
---->{e} C2162/y                          R C3+R    410 -1432   217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b                             F C3+R    303 -1432   57  49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R    303 -1432   57  49 3 cl_invn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+      160   N/C   60  222 13 cl_invn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+      160   N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
   7 local_milli_t2.reg_n.lat_0/a          R C3+R    2591 -1236   165  92 3 cl_invn  07c SRL
5 NET1056
Setup local_milli_t2.reg_n.lat_0/c1        F C3-      160         60  238 14 cl_invn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                          R C3+R    2591 -1236   165  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                             F C3+R    2511 -1236   107  32 1 cs_nnd3z  07c NAND
80 N639
---->{b} C2466/y                          F C3+R    2511 -1236   107  32 1 cs_nnd2n  02c NAND
0 N639

```



```

----> C2466/b R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
80 iu_reset_op_c_t1&0
---->{c} C2393/y R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6
----> gbfozell_6/y F C3+R 473 -1432 78 137 3 cs_invn 09c NOT 0
gbfonet_6
----> gbfozell_6/a R C3+R 410 -1432 217 43 1 cs_invn 09c NOT
64 N2031
---->{d} C2162/y R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cl_invn 07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invn 07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
8 local_milli_t1.reg_n.lat_0/a R C3+R 2591 -1236 165 92 3 cl_invn 07c SRL
5 NET1056
Setup local_milli_t1.reg_n.lat_0/c1 F C3- 160 60 238 14 cl_invn 07c
1200 slow_mode.c1_4
---->{a} BOX789/y R C3+R 2591 -1236 165 92 3 cs_nnd3z 07c NAND
0 NET1056
----> BOX789/a F C3+R 2511 -1236 107 32 1 cs_nnd3z 07c NAND
80 N639
---->{b} C2466/y F C3+R 2511 -1236 107 32 1 cs_nnd2n 02c NAND
0 N639
----> C2466/b R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
80 iu_reset_op_c_t1&0
---->{c} C2393/y R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6
----> gbfozell_6/y F C3+R 473 -1432 78 137 3 cs_invn 09c NOT 0
gbfonet_6
----> gbfozell_6/a R C3+R 410 -1432 217 43 1 cs_invn 09c NOT
64 N2031
---->{d} C2162/y R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cl_invn 07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invn 07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
9 local_milli.reg_n.lat_0/a R C3+R 2591 -1236 165 92 3 cl_invn 07c SRL

```

```

5 NET1056
Setup local_milli.reg_n.lat_0/c1      F C3-   160      60 238 14 cl_invvn 07c 1200
slow_mode.c1_2
---->{a} BOX789/y                      R C3+R   2591 -1236 165 92 3 cs_nnd3z 07c NAND
0 NET1056
----> BOX789/a                         F C3+R   2511 -1236 107 32 1 cs_nnd3z 07c NAND
80 N639
---->{b} C2466/y                       F C3+R   2511 -1236 107 32 1 cs_nnd2n 02c NAND
0 N639
----> C2466/b                          R C3+R   2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
80 iu_reset_op_c_t1&0
---->{c} C2393/y                      R C3+R   2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                          F C3+R   473 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6
----> gbfonet_6/y                     F C3+R   473 -1432 78 137 3 cs_invvn 09c NOT 0
gbfonet_6
----> gbfonet_6/a                     R C3+R   410 -1432 217 43 1 cs_invvn 09c NOT
64 N2031
---->{d} C2162/y                      R C3+R   410 -1432 217 43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b                          F C3+R   303 -1432 57 49 3 cs_nnd3n 02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   303 -1432 57 49 3 cl_invvn 07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2       R C3+    160  N/C  60 222 13 cl_invvn 07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2         R C3+    160  N/C  60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
-----
10 iu_reset_op_c_t1                    F C3+R   2130 -1131 2719 1011 1 PO 0
iu_reset_op_c_t1
RAT 999 0
----> BOX716/OUT                       F C3+R   2130 -1131 2719 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN                       F C3+R   2130 -1131 2719 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y                      F C3+R   2130 -1131 2719 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                          R C3+R   451 -1131 118 137 3 cs_nnd2n 02c NAND
1679 gbfonet_6
----> gbfonet_6/y                     R C3+R   451 -1131 118 137 3 cs_invvn 09c NOT
0 gbfonet_6
----> gbfonet_6/a                     F C3+R   370 -1131 158 43 1 cs_invvn 09c NOT
81 N2031
---->{b} C2162/y                      F C3+R   370 -1131 158 43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b                          R C3+R   290 -1131 46 49 3 cs_nnd3n 02c NAND
81 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n R C3+R   290 -1131 46 49 3 cl_invvn 07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2       R C3+    160  N/C  60 222 13 cl_invvn 07d SRL
130 slow_mode.c2_1
----> slow_mode.clockblock/c2         R C3+    160  N/C  60 222 13 cb_clk_32_1 LCB

```

0 slow_mode.c2_1

--
> measure

The model <IDCDSUC> has:

Primary Inputs = 122
Primary Outputs = 73
Primary BIDs = 0
Signals = 1142
Gate Count = 919
Connections = 1757
Master REG Bits = 83
Slave REG Bits = 83
Internal Area = 4655
External Area = 0
Gates/Connects = 0.523051
Fanout Count = 1757
Average Fanout = 1.538529
Avg Tech Box Size = 5.065288
Tech Box Size Stddev = 0.010915
Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 767
Real boxes = 544
Real connections = 1382
Real LSTs = 2149
Real ICells/box = 8.556985
Real LSTs/box = 3.950368
Real nets/box = 1.409926

Cell Total
Each Cell

Type Cnt Boxname

Power Level Function Int Ext Power Int Ext Power

6	cs_ao22n03c	03c	>	AOI	6	0	0.000	36	0	0.000
2	cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000
1	cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000
1	cs_ao22n04c	04c	>	AOI	6	0	0.000	6	0	0.000
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1	cs_ao12n05c	05c	>	AOI	6	0	0.000	6	0	0.000
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000	
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000	
144	cs_nnd2n02c	02c	>	NAND	3	0	0.000	432	0	0.000
17	cs_nnd2n04c	04c	>	NAND	3	0	0.000	51	0	0.000
1	cs_nnd2n10c	10c	>	NAND	8	0	0.000	8	0	0.000
4	cs_nnd2n12c	12c	>	NAND	12	0	0.000	48	0	0.000
19	cs_nnd3n02c	02c	>	NAND	4	0	0.000	76	0	0.000
3	cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5	cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
2	cs_nnd3n03c	03c	>	NAND	4	0	0.000	8	0	0.000
3	cs_nnd2n11c	11c	>	NAND	11	0	0.000	33	0	0.000
6	cs_nnd2n14c	14c	>	NAND	19	0	0.000	114	0	0.000
1	cs_nnd2n13c	13c	>	NAND	15	0	0.000	15	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000

2	cs_nnd2n14e	14e	>	NAND	19	0	0.000	38	0	0.000
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1	cs_nnd2n14b	14b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd3n12b	12b	>	NAND	22	0	0.000	22	0	0.000
2	cs_nnd4n10c	10c	>	NAND	20	0	0.000	40	0	0.000
1	cs_nnd2n08c	08c	>	NAND	7	0	0.000	7	0	0.000
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3n10c	10c	>	NAND	12	0	0.000	12	0	0.000
1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
8	cs_nor2n02c	02c	>	NOR	3	0	0.000	24	0	0.000
3	cs_nor2n04c	04c	>	NOR	3	0	0.000	9	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2n12c	12c	>	NOR	12	0	0.000	12	0	0.000
1	cs_nor3n10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2n11c	11c	>	NOR	11	0	0.000	11	0	0.000
60	cs_invvn01c	01c	>	NOT	2	0	0.000	120	0	0.000
4	cs_invvn11c	11c	>	NOT	6	0	0.000	24	0	0.000
7	cs_invvn10c	10c	>	NOT	4	0	0.000	28	0	0.000
21	cs_invvn12c	12c	>	NOT	6	0	0.000	126	0	0.000
6	cs_invvn09c	09c	>	NOT	4	0	0.000	24	0	0.000
50	cs_invvn07c	07c	>	NOT	2	0	0.000	100	0	0.000
5	cs_invvn15c	15c	>	NOT	10	0	0.000	50	0	0.000
6	cs_invvn13c	13c	>	NOT	8	0	0.000	48	0	0.000
1	cs_invvn19b	19b	>	NOT	28	0	0.000	28	0	0.000
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12	0	0.000
4	cs_invvn08c	08c	>	NOT	4	0	0.000	16	0	0.000
5	cs_invvn02c	02c	>	NOT	2	0	0.000	10	0	0.000
3	cs_invvn14c	14c	>	NOT	8	0	0.000	24	0	0.000
10	cs_invvn04c	04c	>	NOT	2	0	0.000	20	0	0.000
8	cs_invvn05c	05c	>	NOT	2	0	0.000	16	0	0.000
1	cs_invvn19c	19c	>	NOT	25	0	0.000	25	0	0.000
1	cs_invvn16c	16c	>	NOT	14	0	0.000	14	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
2	cs_oa21n10c	10c	>	OAI	14	0	0.000	28	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
22	cl_invvn07d	07d	>	REG	25	0	0.000	550	0	0.000
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output	
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register	
0	7	*****
2	20	*****
3	1	*
4	5	*****
5	3	***
6	10	*****
7	3	***
9	1	*
10	6	*****
12	1	*
14	6	*****
15	9	*****
16	4	***
17	14	*****

The Histogram Of Fanin vs. Box

# of Fanin	Ops	
1	379	350* plus *****
2	202	200* plus **
3	35	*****
4	18	*****

The Histogram Of Fanout vs. Net

# of Fanout	Nets	
0	2	**
1	940	900* plus *****
2	97	50* plus *****
3	42	*****
4	17	*****
5	7	*****

6	11	*****
7	3	***
8	3	***
13	3	***
14	16	*****
20	1	*

[End of measure]

[measure]: Execution time was 0.6 seconds.

> randsim q

[

>>]: randsim(q);

> tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...

> noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...

repower: setting SCORE option to ALL.

repower: setting LOWEST_NOT_EQUAL mode.

repower: setting NO_VIOLATIONS option.

-1955.13 Avg: -181.15

maximum area for proto box IDCDSUC is 4655

-1955.13 Avg: -181.15

[noncritical]: noncritical applied to boxes with slack > 0.00

[noncritical]: Number of boxes to process is 919.

[noncritical]: Number of boxes processed is 0.

-1955.13 Avg: -181.07

[BD-500026]: repower was applied 5 times.

[repower]: Execution time was 5.4 seconds.

> tc_parm MARGIN(10000000)

> bufmatch ESTIMATED,TWO_LEVEL,NO_VIOLATIONS

[

>>]: ltorbox(dbufmatch(ESTIMATED,TWO_LEVEL,NO_VIOLATIONS));

[BD-500000]: bufmatch CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32

setting ESTIMATED option.

setting TWO_LEVEL option.

setting NO_VIOLATIONS option.

-1955.13 Avg: -181.07

[BD-500302]: 2 pins in 1 trees swapped, 9 trees tried

-1955.13 Avg: -181.05

[bufmatch]: Execution time was 0.1 seconds.

> fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}

[

>>]: ltorbox(dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS));

setting ACTUAL option.

setting ONE_LEVEL option.

setting NO_VIOLATIONS option.

-1955.13 Avg: -181.05

[BD-500300]: 2 pins on 1 gates swapped.

-1955.13 Avg: -181.08

[fanmatch]: Execution time was 3.6 seconds.

> get_default_delay_synlimit

> tc_parm OFFSET(0)

> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

```

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > quick tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1955.13 Avg: -181.08
[tdual_correct]: CMVC version 1.8 compiled on Mar 31 1999 at 11:35:12.
[tdual_correct]: setting SCORE option to ALL.
[tdual_correct]: setting RE_POWER option.
[tdual_correct]: setting INC mode.
[tdual_correct]: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.08
Selected 398 critical boxes of 919 total.
[quick]: Number of boxes to process is 398.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -181.08
[tdual_correct]: applied 0 times
        > tc_parm OFFSET(0)
        > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > reset_critical_slack_limit
-1955.13 Avg: -181.08
resetting the current slack to -1955.1339
        > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
setting SCORE option to ALL.
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.08
ArrayNum: 6 ArrayMax: 919
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > tc_parm REGALL
        > repower_paths FUZZY(0.02)
initial slack is -1955
after repower paths slack is -1955
        > critical {repower(SCORE(ALL ),INC ,NO_VIOLATIONS), re...
critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
repower: setting SCORE option to ALL.
repower: setting INC mode.

```

repower: setting NO_VIOLATIONS option.
 repower: setting SCORE option to ALL.
 repower: setting INC mode.
 repower: setting NO_VIOLATIONS option.
 -1955.13 Avg: -181.08
 ArrayNum: 6 ArrayMax: 919
 [BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.1 seconds.
 [BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.1 seconds.
 [BD-502000]: Called transforms 12 times and applied 0 of them.
 > compare_critical_slack_limit
 -1955.13 Avg: -181.08
 comparing new slack -1955.1339 to saved slack -1935.5825
 > write_end_point_report -points 3 -paths 1
 [ET-0018]: >Begin...New EndPoint Report
 for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:03:36 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST)		
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST)		
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)		
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST)		
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST)		
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST)		
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)		
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST)		
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST)		
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test

Num/	LimitedAT/	Delay/	Failed Test/
Test PinName	E Phase	AT	Slack
NetName	Slew	CL	FO Cell
		P Func	T.Adj


```

--
1 dcd_succ_last_t1          R C3+R  2954 -1955  3847 1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT            R C3+R  2954 -1955  3847 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            R C3+R  2954 -1955  3847 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y              R C3+R  2954 -1955  3847 1011 1 cs_invrn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a              F C3+R  1092 -1955   55 139 4 cs_invrn  01c NOT
1862 N675
----> {a} C2738/y         F C3+R  1092 -1955   55 139 4 cs_nnd2n  14b NAND
0 N675
----> C2738/a            R C3+R  1063 -1955   71 108 1 cs_nnd2n  14b NAND
29 last_cycle
----> {b} C2487/y         R C3+R  1063 -1955   71 108 1 cs_nnd2n  14e NAND
0 last_cycle
----> C2487/b            F C3+R  1034 -1955   32 140 3 cs_nnd2n  14e NAND
29 N1587
----> C1952/y            F C3+R  1034 -1955   32 140 3 cs_invrn  19b NOT      0
N1587
----> C1952/a            R C3+R  1024 -1955   80 319 1 cs_invrn  19b NOT
10 num_dcd_cyl&0(1)
----> BOX679/OUT         R C3+R  1024 -1955   80 319 1 IOPAD      IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN         R C3+R  1024 -1955   80 319 1 IOPAD      IOPAD      0
num_dcd_cyl(1)
----> num_dcd_cyl(1)     R C3+R  1024 -1955   80 319 1 PI          0
num_dcd_cyl(1)
-----
2 dcd_succ_last_t1          F C3+R  2644 -1645  2362 1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT            F C3+R  2644 -1645  2362 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            F C3+R  2644 -1645  2362 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y              F C3+R  2644 -1645  2362 1011 1 cs_invrn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a              R C3+R  1208 -1645   92 139 4 cs_invrn  01c NOT
1436 N675
----> {a} C2738/y         R C3+R  1208 -1645   92 139 4 cs_nnd2n  14b NAND
0 N675
----> C2738/b            F C3+R  1152 -1645   76 159 3 cs_nnd2n  14b NAND
56 N1692
----> {b} C2725rwr/y      F C3+R  1152 -1645   76 159 3 cs_nnd2n  14e NAND
0 N1692
----> C2725rwr/a         R C3+R  1097 -1645  148 166 2 cs_nnd2n  14e NAND
56 N1479
----> {c} C2721rwr/y      R C3+R  1097 -1645  148 166 2 cs_nnd3n  12b NAND
0 N1479
----> C2721rwr/c         F C3+R  994 -1645  125 95 2 cs_nnd3n  12b NAND
102 N1497

```

```

---->{d} C2709rwr/y          F C3+R   994 -1645  125  95 2 cs_nor3n  10e NOR
0 N1497
----> C2709rwr/c             R C3+R   898 -1645  137  68 2 cs_nor3n  10e NOR
96 N1781
---->{e} C2885/y             R C3+R   898 -1645  137  68 2 cs_nnd4n  10c NAND
0 N1781
----> C2885/d                 F C3+R   825 -1645  44  50 1 cs_nnd4n  10c NAND
73 N1997
---->{f} C2886/y             F C3+R   825 -1645  44  50 1 cs_nnd2n  14c NAND
0 N1997
----> C2886/a                 R C3+R   802 -1645  80 124 2 cs_nnd2n  14c NAND
23 op_serialize&0
----> BOX638/OUT              R C3+R   802 -1645  80 124 2 IOPAD    IOPAD
0 op_serialize&0
----> BOX638/IN              R C3+R   802 -1645  80 124 2 IOPAD    IOPAD    0
op_serialize
----> op_serialize            R C3+R   802 -1645  80 124 2 PI          0
op_serialize

```

```

3 iu_reset_op_c_t1          R C3+R  2431 -1432 3912 1011 1 PO          0
iu_reset_op_c_t1
RAT                          999                                0
----> BOX716/OUT              R C3+R  2431 -1432 3912 1011 1 IOPAD    IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN              R C3+R  2431 -1432 3912 1044 3 IOPAD    IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y             R C3+R  2431 -1432 3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                 F C3+R   473 -1432  78 137 3 cs_nnd2n  02c NAND
1958 gbfonet_6
----> gbfozell_6/y           F C3+R   473 -1432  78 137 3 cs_invn  09c NOT    0
gbfonet_6
----> gbfozell_6/a           R C3+R   410 -1432 217  43 1 cs_invn  09c NOT
64 N2031
---->{b} C2162/y             R C3+R   410 -1432 217  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b                 F C3+R   303 -1432  57  49 3 cs_nnd3n  02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   303 -1432  57  49 3 cl_invn  07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+    160  N/C   60 222 13 cl_invn  07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+    160  N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

> nextbox chklegal

```

[
>>]: nextbox( chklegal );
[BD-40000]: chklegal CMVC version 1.2.1.12 compiled on Apr 8 1999 at 05:03:03
[BD-41212]: (E) Gate 'slow_mode.clockblock' is bound to cell 'cb_clk_32_1' which is not a proper parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_1' is bound to cell 'cb_clk_32_1' which is not a proper parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_2' is bound to cell 'cb_clk_32_1' which is not a proper

```

```

parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_3' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_4' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_5' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41200]: No illegal DOT gates found.
[BD-41202]: No illegal pin drops found.
    > nextnet chklegal
[
>>]: nextnet( chklegal );
[BD-41206]: No illegal pin drops found.
[BD-41204]: No illegally dotted nets found.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/late_area.tcl
    > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
    > noncritical repower(SCORE(FAST),LOWEST_NOT_EQUAL,NO_VIOL...
repower: setting SCORE option to FAST.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.08
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -181.07
[BD-500026]: repower was applied 1 times.
[BD-500287]: score changed to OUT 0 of 0 times
[repower]: Execution time was 5.3 seconds.
    > bufmatch ESTIMATED,TWO_LEVEL,NO_VIOLATIONS
[
>>]: ltorbox( dbufmatch(ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.07
[BD-500302]: 0 pins in 0 trees swapped, 9 trees tried
-1955.13 Avg: -181.07
[bufmatch]: Execution time was 0.1 seconds.
    > fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}
[
>>]: ltorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.07
[BD-500300]: 0 pins on 0 gates swapped.
-1955.13 Avg: -181.07
[fanmatch]: Execution time was 3.6 seconds.
    > get_default_delay_synlimit
    > get_default_delay_synlimit
    > tc_parm OFFSET(0)
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

```

```

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > quick tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1955.13 Avg: -181.07
[tdual_correct]: setting SCORE option to ALL.
[tdual_correct]: setting RE_POWER option.
[tdual_correct]: setting INC mode.
[tdual_correct]: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.07
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.07
Selected 398 critical boxes of 919 total.
[quick]: Number of boxes to process is 398.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -181.07
[tdual_correct]: applied 0 times
    > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
    > compare_critical_slack_limit
-1955.13 Avg: -181.07
comparing new slack -1955.1339 to saved slack -1935.5825
    > get_default_synlimit
    > get_default_synlimit
    > get_default_synlimit
    > get_default_synlimit
    > get_default_synlimit
    > get_default_synlimit
    > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
    > noncritical onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_...
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting LOWEST mode.
[onebuff]: setting WORST option.
[onebuff]: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.07
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.07
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -181.07
[onebuff]: was applied 0 times
    > noncritical divv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIO...
setting SCORE option to ALL.
setting RE_POWER option.

```

```

setting LOWEST mode.
setting WORST option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.07
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.07
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -192.43
[BD-500500]: Moved 15 sinks and removed 10 inverters.
    > get_default_synlimit
    > get_default_synlimit
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/time_redund.tcl
    > is_parm no_tech_redund
    > str_parm tgfs_effort
    > is_parm no_tech_redund
    > is_parm remove_redundant_regs
    > make_constants_in nonreg_only
    > ignore_trivial_expansions EQNVIEW
    > expansions_from_tib EQNVIEW
    > expansions_from_eqn EQNVIEW
    > copy_def_to_proto EQNVIEW
    > apply_decide_boolean(EQNVIEW)
generated 1 paths in 70 milliseconds
    > apply Hstructure(TRUE_BASE_AUTOGEN)
generated 1 paths in 40 milliseconds
    > gen_nonreg_tib_expns TIB_EXPANSIONS
    > apply Hunstructure()
    > expandable_name
        > set_nochange
        > constmod
        > is_parm keep_bad_pgroups
        > bad_pgroups_expandable
    > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
[
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(TRUE_BASE_AUTOGEN)) );
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 909 objects as matching keyword criteria.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 1132 signals, 909 usage boxes and 1747 connections.
[simple_expand]: Modified 0 gates.
    > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
[
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )

```

VIEW(TIB_EXPANSIONS)));

[

>>]: nextbox(SASname(RESTORE));

[synsasname]: Restored 0 BRKPT net names

[synsasname]: Restored 189 REG and SEQUENTIAL output net names

[synsasname]: Execution time was 0.0 seconds.

[BD-354200]: Selected 0 out of 909 objects as matching keyword criteria.

[

>>]: nextbox(SASname(PROTECT));

[synsasname]: Protected 180 BRKPT net names

[synsasname]: Protected 189 REG and SEQUENTIAL output net names

[synsasname]: Execution time was 0.0 seconds.

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1132 signals, 909 usage boxes and 1747 connections.

[simple_expand]: Modified 0 gates.

> headless

[headless]: Removed 0 boxes

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1132 signals, 909 usage boxes and 1747 connections.

> cleanse1

Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1132 signals, 909 usage boxes and 1747 connections.

[

>>]: nextbox(invrem(),onein(),twoin());

using pattern information

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1132 signals, 909 usage boxes and 1747 connections.

[

>>]: nextbox(twoin());

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

> nochange

> set_nochange

> apply {Hstructure(TRULE_BASE_AUTOGEN TIB_EXPANSIONS)}

generated 1 paths in 60 milliseconds

> rtolbox {Htgfsredund(100)}

[

>>]: rtolbox(Htgfsredund(100));

[BD-330500]: Out of 2359 faults found 0 redundancies, eliminated 0, could not decide 0 in 1 seconds.

> apply Hunstructure()

> nochange

> DeleteAllProtosUnderView TIB_EXPANSIONS

[SRULE-17175]: Deleted 0 Proto Boxes

> randsim q

[

>>]: randsim(q);

> randsim q

```

[
>>]: randsim( q );
      > is_parm keep_bad_pgroups
      > copyinfo
      > fix_bad_pgroups
[BD-82400]: Added 0 terminators, deleted 0 pins and tied 0 pins.
      > basetype
[
>>]: nextbox_with_test( test_syn_hide(!HIDE_MAP),genmark );
[test_syn_hide]: Number of objects selected was 909 of 909 checked.
[
>>]: nextnet( geninv );
      > copyinfo
      > nextbox {mapprim, mapterm}
[
>>]: nextbox( mapprim, mapterm );
[mapprim]: Execution time was 0.0 seconds.
[BD-83600]: 0 terminators processed 0 dummy nets removed.
      > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
      The model has 1132 signals, 909 usage boxes and 1747 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
using pattern information
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
      The model has 1132 signals, 909 usage boxes and 1747 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
      The model has 1132 signals, 909 usage boxes and 1747 connections.
[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
      > nextbox tchname(NOERR)
[
>>]: nextbox( tchname(NOERR) );
NOERR option set
[BD-85300]: Looked at 909 gates, bound 0, 0 had hints.
[tchname]: Execution time was 0.0 seconds.
Pattern hint flag is inactive
      > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
      The model has 1132 signals, 909 usage boxes and 1747 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
using pattern information

```

[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1132 signals, 909 usage boxes and 1747 connections.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1132 signals, 909 usage boxes and 1747 connections.

[

>>]: nextbox(twoin());

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

> copyinfo

> has_children CONSTANT

> tiegen FOLIM(8)

> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000

[tc_parm]: =====

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000

> compare_key_slack_limit TIME_REDUND

-1955.13 Avg: -192.43

comparing keyed new slack -1955.1339 to keyed saved slack

-11229317540483502000000000000000000000000.0000

> reset_key_slack_limit TIME_REDUND

-1955.13 Avg: -192.43

resetting keyed current slack to -1955.1339

> critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)

critical(tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS));

-1955.13 Avg: -192.43

maximum area for proto box IDCDSUC is 4635

setting SCORE option to ALL.

setting ACTUAL option.

setting TWO_LEVEL option.

setting NO_VIOLATIONS option.

-1955.13 Avg: -192.43

ArrayNum: 6 ArrayMax: 909

[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.

[tswap]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}

critical(repower(SCORE(ALL),INC ,NO_VIOLATIONS));

-1955.13 Avg: -192.43

maximum area for proto box IDCDSUC is 4635

repower: setting SCORE option to ALL.

repower: setting INC mode.

repower: setting NO_VIOLATIONS option.


```

-1955.13 Avg: -192.43
ArrayNum: 6 ArrayMax: 909
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > compare_key_slack_limit TIME_REDUND
-1955.13 Avg: -192.43
comparing keyed new slack -1955.1339 to keyed saved slack -1935.5825
    > delete_key_slack_limit TIME_REDUND
    > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1955.13 Avg: -192.43
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting INC mode.
[onebuff]: setting NO_VIOLATIONS option.
-1955.13 Avg: -192.43
maximum area for proto box IDCDSUC is 4635
[quick]: Number of boxes to process is 909.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -192.43
[onebuff]: was applied 0 times
    > quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1955.13 Avg: -192.43
setting SCORE option to ALL.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
-1955.13 Avg: -192.43
maximum area for proto box IDCDSUC is 4635
[quick]: Number of boxes to process is 909.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -188.21
[BD-500500]: Moved 5 sinks and removed 3 inverters.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/opt_delay.tcl
    > syntrace
    > logic_report

```

Model Summary of Network 'IDCDSUC'

```

Input Ports: 122
Output Ports: 73
Bidi Ports: 0
Gates: 906
Nets: 1127
Connections: 1671
Sequential Area: 2726
Total Area: 4614

```

Cell Distribution of Network 'IDCDSUC'

Count	Cell	Function	Area	TotalArea
-------	------	----------	------	-----------

1	cs_ao12n05c	AOI	6	6
1	cs_ao22n04c	AOI	6	6
1	cs_ao12n10c	AOI	12	12
1	cs_ao22n10c	AOI	18	18
2	cs_ao12n03c	AOI	4	8
6	cs_ao22n03c	AOI	6	36
180	BRKPT	BRKPT	0	0
195	IOPAD	IOPAD	0	0
17	cs_nnd2n04c	NAND	3	51
3	cs_nnd2n11c	NAND	11	33
1	cs_nnd2n05c	NAND	4	4
1	cs_nnd2n08c	NAND	7	7
2	cs_nnd3n05c	NAND	6	12
6	cs_nnd2n14c	NAND	19	114
1	cs_nnd2n10c	NAND	8	8
2	cs_nnd4v06c	NAND	8	16
1	cs_nnd2n13c	NAND	15	15
1	cs_nnd3z07c	NAND	10	10
1	cs_nnd3n07c	NAND	6	6
1	cs_nnd2f03c	NAND	4	4
4	cs_nnd2n12c	NAND	12	48
19	cs_nnd3n02c	NAND	4	76
2	cs_nnd2n14e	NAND	19	38
144	cs_nnd2n02c	NAND	3	432
3	cs_nnd2n03c	NAND	3	9
1	cs_nnd3n10c	NAND	12	12
5	cs_nnd4n03c	NAND	5	25
2	cs_nnd2n07c	NAND	4	8
1	cs_nnd2n14b	NAND	20	20
2	cs_nnd3n03c	NAND	4	8
1	cs_nnd3n12b	NAND	22	22
2	cs_nnd4n10c	NAND	20	40
1	cs_nor2n12c	NOR	12	12
1	cs_nor3n03c	NOR	4	4
1	cs_nor3n10e	NOR	16	16
8	cs_nor2n02c	NOR	3	24
3	cs_nor2n04c	NOR	3	9
1	cs_nor2n11c	NOR	11	11
6	cs_invvn13c	NOT	8	48
1	cs_invvv19b	NOT	28	28
7	cs_invvn06c	NOT	2	14
4	cs_invvn08c	NOT	4	16
3	cs_invvn02c	NOT	2	6
3	cs_invvn14c	NOT	8	24
8	cs_invvn04c	NOT	2	16
8	cs_invvn05c	NOT	2	16
46	cs_invvn07c	NOT	2	92
7	cs_invvn10c	NOT	4	28
1	cs_invvn01e	NOT	2	2
54	cs_invvn01c	NOT	2	108
22	cs_invvn12c	NOT	6	132
6	cs_invvn09c	NOT	4	24
1	cs_invvn16c	NOT	14	14

6	cs_invvn15c	NOT	10	60
3	cs_invvn11c	NOT	6	18
1	cs_oa22n10c	OAI	18	18
2	cs_oa21n10c	OAI	14	28
18	cl_nnd2n07c	REG	26	468
1	cl_invvn05c	REG	25	25
8	cl_ao22n07c	REG	33	264
14	cl_invvn06d	REG	25	350
1	cl_invvn05d	REG	25	25
2	cl_nnd3n07c	REG	29	58
12	cl_invvn07c	REG	25	300
1	cl_nor2n06c	REG	26	26
22	cl_invvn07d	REG	25	550
1	cl_ao21n07c	REG	30	30
2	cl_invvn06c	REG	25	50
1	cl_ao21n07c	REG	30	30
1	cb_mode_block	SEQUENTIAL	70	70
6	cb_clk_32_1	SEQUENTIAL	80	480
1	cs_xbn2n01b	XNOR	8	8
1	cs_xbo2n01d	XOR	8	8

> write_end_point_report -points 3

[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:03:52 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release-Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AsstrRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM

CLOCK + ADJUST)

Arrival Time Limiting

ATLimit

Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj

--								
1 dcd_succ_last_t1	R C3+R	2954	-1955	3847	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	R C3+R	2954	-1955	3847	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2954	-1955	3847	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2954	-1955	3847	1011	1 cs_invv	01c	NOT
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1092	-1955	55	139	4 cs_invv	01c	NOT
1862 N675								
---->{a} C2738/y	F C3+R	1092	-1955	55	139	4 cs_nnd2n	14b	NAND
0 N675								
----> C2738/a	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14b	NAND
29 last_cycle								
---->{b} C2487/y	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14e	NAND
0 last_cycle								
----> C2487/b	F C3+R	1034	-1955	32	140	3 cs_nnd2n	14e	NAND
29 N1587								
----> C1952/y	F C3+R	1034	-1955	32	140	3 cs_invv	19b	NOT
N1587								0
----> C1952/a	R C3+R	1024	-1955	80	319	1 cs_invv	19b	NOT
10 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1955	80	319	1 IOPAD		IOPAD
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1955	80	319	1 IOPAD		IOPAD
num_dcd_cyl(1)								0
----> num_dcd_cyl(1)	R C3+R	1024	-1955	80	319	1 PI		0
num_dcd_cyl(1)								

--								
2 dcd_succ_last_t1	F C3+R	2644	-1645	2362	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	F C3+R	2644	-1645	2362	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1								
----> BOX714/IN	F C3+R	2644	-1645	2362	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1&0								
----> C167/y	F C3+R	2644	-1645	2362	1011	1 cs_invv	01c	NOT
0 dcd_succ_last_t1&0								
----> C167/a	R C3+R	1208	-1645	92	139	4 cs_invv	01c	NOT
1436 N675								
---->{a} C2738/y	R C3+R	1208	-1645	92	139	4 cs_nnd2n	14b	NAND
0 N675								
----> C2738/b	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14b	NAND
56 N1692								
---->{b} C2725rwr/y	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14e	NAND

```

0 N1692
----> C2725rwr/a      R C3+R   1097 -1645  148  166 2 cs_nnd2n  14e NAND
56 N1479
---->{c} C2721rwr/y    R C3+R   1097 -1645  148  166 2 cs_nnd3n  12b NAND
0 N1479
----> C2721rwr/c      F C3+R   994 -1645  125   95 2 cs_nnd3n  12b NAND
102 N1497
---->{d} C2709rwr/y    F C3+R   994 -1645  125   95 2 cs_nor3n  10e NOR
0 N1497
----> C2709rwr/c      R C3+R   898 -1645  137   68 2 cs_nor3n  10e NOR
96 N1781
---->{e} C2885/y       R C3+R   898 -1645  137   68 2 cs_nnd4n  10c NAND
0 N1781
----> C2885/d          F C3+R   825 -1645   44   50 1 cs_nnd4n  10c NAND
73 N1997
---->{f} C2886/y       F C3+R   825 -1645   44   50 1 cs_nnd2n  14c NAND
0 N1997
----> C2886/a          R C3+R   802 -1645   80  124 2 cs_nnd2n  14c NAND
23 op_serialize&0
----> BOX638/OUT       R C3+R   802 -1645   80  124 2 IOPAD    IOPAD
0 op_serialize&0
----> BOX638/IN        R C3+R   802 -1645   80  124 2 IOPAD    IOPAD  0
op_serialize
----> op_serialize     R C3+R   802 -1645   80  124 2 PI      0
op_serialize

-----
3 iu_reset_op_c_t1    R C3+R   2610 -1611  3912 1011 1 PO      0
iu_reset_op_c_t1
RAT 999 0
----> BOX716/OUT       R C3+R   2610 -1611  3912 1011 1 IOPAD    IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN        R C3+R   2610 -1611  3912 1044 3 IOPAD    IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y       R C3+R   2610 -1611  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   568 -1611   96  196 6 cs_nnd2n  02c NAND
2043 gbfonet_6
----> gbfonet_6/y      F C3+R   568 -1611   96  196 6 cs_invvn  09c NOT  0
gbfonet_6
----> gbfonet_6/a      R C3+R   490 -1611  217   43 1 cs_invvn  09c NOT
78 N2031
---->{b} C2162/y       R C3+R   490 -1611  217   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b          F C3+R   358 -1611  144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n F C3+R   358 -1611  144  216 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160  N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160  N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
> tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...

```

```

> noncritical repower(SCORE(FAST),LOWEST_NOT_EQUAL,NO_VIOL...
repower: setting SCORE option to FAST.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.21
maximum area for proto box IDCDSUC is 4614
-1955.13 Avg: -188.21
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -188.21
[BD-500026]: repower was applied 0 times.
[BD-500287]: score changed to OUT 0 of 0 times
[repower]: Execution time was 5.1 seconds.
> syntrace
> logic_report

```

Model Summary of Network 'IDCDSUC'

```

Input Ports: 122
Output Ports: 73
Bidi Ports: 0
Gates: 906
Nets: 1127
Connections: 1671
Sequential Area: 2726
Total Area: 4614

```

Cell Distribution of Network 'IDCDSUC'

Count	Cell	Function	Area	TotalArea
1	cs_ao12n05c	AOI	6	6
1	cs_ao22n04c	AOI	6	6
1	cs_ao12n10c	AOI	12	12
1	cs_ao22n10c	AOI	18	18
2	cs_ao12n03c	AOI	4	8
6	cs_ao22n03c	AOI	6	36
180	BRKPT	BRKPT	0	0
195	IOPAD	IOPAD	0	0
17	cs_nnd2n04c	NAND	3	51
3	cs_nnd2n11c	NAND	11	33
1	cs_nnd2n05c	NAND	4	4
1	cs_nnd2n08c	NAND	7	7
2	cs_nnd3n05c	NAND	6	12
6	cs_nnd2n14c	NAND	19	114
1	cs_nnd2n10c	NAND	8	8
2	cs_nnd4v06c	NAND	8	16
1	cs_nnd2n13c	NAND	15	15
1	cs_nnd3z07c	NAND	10	10
1	cs_nnd3n07c	NAND	6	6
1	cs_nnd2f03c	NAND	4	4
4	cs_nnd2n12c	NAND	12	48
19	cs_nnd3n02c	NAND	4	76

2	cs_nnd2n14e	NAND	19	38
144	cs_nnd2n02c	NAND	3	432
3	cs_nnd2n03c	NAND	3	9
1	cs_nnd3n10c	NAND	12	12
5	cs_nnd4n03c	NAND	5	25
2	cs_nnd2n07c	NAND	4	8
1	cs_nnd2n14b	NAND	20	20
2	cs_nnd3n03c	NAND	4	8
1	cs_nnd3n12b	NAND	22	22
2	cs_nnd4n10c	NAND	20	40
1	cs_nor2n12c	NOR	12	12
1	cs_nor3n03c	NOR	4	4
1	cs_nor3n10e	NOR	16	16
8	cs_nor2n02c	NOR	3	24
3	cs_nor2n04c	NOR	3	9
1	cs_nor2n11c	NOR	11	11
6	cs_invvn13c	NOT	8	48
1	cs_invvn19b	NOT	28	28
7	cs_invvn06c	NOT	2	14
4	cs_invvn08c	NOT	4	16
3	cs_invvn02c	NOT	2	6
3	cs_invvn14c	NOT	8	24
8	cs_invvn04c	NOT	2	16
8	cs_invvn05c	NOT	2	16
46	cs_invvn07c	NOT	2	92
7	cs_invvn10c	NOT	4	28
1	cs_invvn01e	NOT	2	2
54	cs_invvn01c	NOT	2	108
22	cs_invvn12c	NOT	6	132
6	cs_invvn09c	NOT	4	24
1	cs_invvn16c	NOT	14	14
6	cs_invvn15c	NOT	10	60
3	cs_invvn11c	NOT	6	18
1	cs_oa22n10c	OAI	18	18
2	cs_oa21n10c	OAI	14	28
18	cl_nnd2n07c	REG	26	468
1	cl_invvn05c	REG	25	25
8	cl_ao22n07c	REG	33	264
14	cl_invvn06d	REG	25	350
1	cl_invvn05d	REG	25	25
2	cl_nnd3n07c	REG	29	58
12	cl_invvn07c	REG	25	300
1	cl_nor2n06c	REG	26	26
22	cl_invvn07d	REG	25	550
1	cl_ao21n07c	REG	30	30
2	cl_invvn06c	REG	25	50
1	cl_ao21n07c	REG	30	30
1	cb_mode_block	SEQUENTIAL	70	70
6	cb_clk_32_1	SEQUENTIAL	80	480
1	cs_xbn2n01b	XNOR	8	8
1	cs_xbo2n01d	XOR	8	8

> write_end_point_report -points 3
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:03:58 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path
Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ LimitedAT/ Delay/ Failed Test/
Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj
NetName

1 dcd_succ_last_t1 R C3+R 2954 -1955 3847 1011 1 PO 0
dcd_succ_last_t1
RAT 999 0
----> BOX714/OUT R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1
----> BOX714/IN R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&0
----> C167/y R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0
----> C167/a F C3+R 1092 -1955 55 139 4 cs_invvn 01c NOT
1862 N675
---->{a} C2738/y F C3+R 1092 -1955 55 139 4 cs_nnd2n 14b NAND
0 N675
----> C2738/a R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
29 last_cycle
---->{b} C2487/y R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND


```

0 last_cycle
----> C2487/b          F C3+R   1034 -1955   32  140 3 cs_nnd2n  14e NAND
29 N1587
----> C1952/y          F C3+R   1034 -1955   32  140 3 cs_invvv  19b NOT    0
N1587
----> C1952/a          R C3+R   1024 -1955   80  319 1 cs_invvv  19b NOT
10 num_dcd_cyl&0(1)
----> BOX679/OUT        R C3+R   1024 -1955   80  319 1 IOPAD    IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN        R C3+R   1024 -1955   80  319 1 IOPAD    IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1) .  R C3+R   1024 -1955   80  319 1 PI          0
num_dcd_cyl(1)
-----
--
2 dcd_succ_last_t1    F C3+R   2644 -1645  2362 1011 1 PO          0
dcd_succ_last_t1
RAT                    999                                0
----> BOX714/OUT        F C3+R   2644 -1645  2362 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1
----> BOX714/IN        F C3+R   2644 -1645  2362 1011 1 IOPAD    IOPAD
0 dcd_succ_last_t1&0
----> C167/y           F C3+R   2644 -1645  2362 1011 1 cs_invvn  01c NOT
0 dcd_succ_last_t1&0
----> C167/a           R C3+R   1208 -1645   92  139 4 cs_invvn  01c NOT
1436 N675
---->{a} C2738/y       R C3+R   1208 -1645   92  139 4 cs_nnd2n  14b NAND
0 N675
----> C2738/b          F C3+R   1152 -1645   76  159 3 cs_nnd2n  14b NAND
56 N1692
---->{b} C2725rwr/y    F C3+R   1152 -1645   76  159 3 cs_nnd2n  14e NAND
0 N1692
----> C2725rwr/a       R C3+R   1097 -1645   148 166 2 cs_nnd2n  14e NAND
56 N1479
---->{c} C2721rwr/y    R C3+R   1097 -1645   148 166 2 cs_nnd3n  12b NAND
0 N1479
----> C2721rwr/c       F C3+R   994 -1645   125  95 2 cs_nnd3n  12b NAND
102 N1497
---->{d} C2709rwr/y    F C3+R   994 -1645   125  95 2 cs_nor3n  10e NOR
0 N1497
----> C2709rwr/c       R C3+R   898 -1645   137  68 2 cs_nor3n  10e NOR
96 N1781
---->{e} C2885/y       R C3+R   898 -1645   137  68 2 cs_nnd4n  10c NAND
0 N1781
----> C2885/d          F C3+R   825 -1645   44  50 1 cs_nnd4n  10c NAND
73 N1997
---->{f} C2886/y       F C3+R   825 -1645   44  50 1 cs_nnd2n  14c NAND
0 N1997
----> C2886/a          R C3+R   802 -1645   80  124 2 cs_nnd2n  14c NAND
23 op_serialize&0
----> BOX638/OUT        R C3+R   802 -1645   80  124 2 IOPAD    IOPAD
0 op_serialize&0
----> BOX638/IN        R C3+R   802 -1645   80  124 2 IOPAD    IOPAD    0
op_serialize
----> op_serialize      R C3+R   802 -1645   80  124 2 PI          0

```

op_serialize

```
--
3 iu_reset_op_c_t1          R C3+R  2610 -1611  3912 1011 1 PO          0
iu_reset_op_c_t1
RAT          999          0
----> BOX716/OUT            R C3+R  2610 -1611  3912 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN            R C3+R  2610 -1611  3912 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R  2610 -1611  3912 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a             F C3+R  568 -1611   96  196 6 cs_nnd2n  02c NAND
2043 gbfonet_6
----> gbfonet_6/y         F C3+R  568 -1611   96  196 6 cs_invvn  09c NOT      0
gbfonet_6
----> gbfonet_6/a         R C3+R  490 -1611  217   43 1 cs_invvn  09c NOT
78 N2031
---->{b} C2162/y          R C3+R  490 -1611  217   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b             F C3+R  358 -1611  144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R  358 -1611  144  216 5 cl_invvn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+   160   N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+   160   N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
```

```
--
> write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
          for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
```

Sun Apr 18 22:03:58 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

```
-----
Slack Continuation      SlkCont  Slack due to a point downstream on path
Required Arrival Time   RAT        ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup      ClkGSet   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold       ClkGHld   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width  ClkTPW   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                   Setup     ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
```

Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	-------------------------------------

--							
1 dcd_succ_last_t1	R C3+R	2954	-1955	3847	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	R C3+R	2954	-1955	3847	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	2954	-1955	3847	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	2954	-1955	3847	1011	1 cs_invv	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1092	-1955	55	139	4 cs_invv	01c NOT
1862 N675							
---->{a} C2738/y	F C3+R	1092	-1955	55	139	4 cs_nnd2n	14b NAND
0 N675							
----> C2738/a	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14b NAND
29 last_cycle							
---->{b} C2487/y	R C3+R	1063	-1955	71	108	1 cs_nnd2n	14e NAND
0 last_cycle							
----> C2487/b	F C3+R	1034	-1955	32	140	3 cs_nnd2n	14e NAND
29 N1587							
----> C1952/y	F C3+R	1034	-1955	32	140	3 cs_invv	19b NOT
N1587							
----> C1952/a	R C3+R	1024	-1955	80	319	1 cs_invv	19b NOT
10 num_dcd_cyl&0(1)							
----> BOX679/OUT	R C3+R	1024	-1955	80	319	1 IOPAD	IOPAD
0 num_dcd_cyl&0(1)							
----> BOX679/IN	R C3+R	1024	-1955	80	319	1 IOPAD	IOPAD
num_dcd_cyl(1)							
----> num_dcd_cyl(1)	R C3+R	1024	-1955	80	319	1 PI	0
num_dcd_cyl(1)							

--							
2 dcd_succ_last_t1	F C3+R	2644	-1645	2362	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	F C3+R	2644	-1645	2362	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	F C3+R	2644	-1645	2362	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							

----> C167/y	F C3+R	2644	-1645	2362	1011	1 cs_inwvn	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	R C3+R	1208	-1645	92	139	4 cs_inwvn	01c NOT
1436 N675							
---->{a} C2738/y	R C3+R	1208	-1645	92	139	4 cs_nnd2n	14b NAND
0 N675							
----> C2738/b	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14b NAND
56 N1692							
---->{b} C2725rwr/y	F C3+R	1152	-1645	76	159	3 cs_nnd2n	14e NAND
0 N1692							
----> C2725rwr/a	R C3+R	1097	-1645	148	166	2 cs_nnd2n	14e NAND
56 N1479							
---->{c} C2721rwr/y	R C3+R	1097	-1645	148	166	2 cs_nnd3n	12b NAND
0 N1479							
----> C2721rwr/c	F C3+R	994	-1645	125	95	2 cs_nnd3n	12b NAND
102 N1497							
---->{d} C2709rwr/y	F C3+R	994	-1645	125	95	2 cs_nor3n	10e NOR
0 N1497							
----> C2709rwr/c	R C3+R	898	-1645	137	68	2 cs_nor3n	10e NOR
96 N1781							
---->{e} C2885/y	R C3+R	898	-1645	137	68	2 cs_nnd4n	10c NAND
0 N1781							
----> C2885/d	F C3+R	825	-1645	44	50	1 cs_nnd4n	10c NAND
73 N1997							
---->{f} C2886/y	F C3+R	825	-1645	44	50	1 cs_nnd2n	14c NAND
0 N1997							
----> C2886/a	R C3+R	802	-1645	80	124	2 cs_nnd2n	14c NAND
23 op_serialize&0							
----> BOX638/OUT	R C3+R	802	-1645	80	124	2 IOPAD	IOPAD
0 op_serialize&0							
----> BOX638/IN	R C3+R	802	-1645	80	124	2 IOPAD	IOPAD
op_serialize							
----> op_serialize	R C3+R	802	-1645	80	124	2 PI	0
op_serialize							

3 iu_reset_op_c_t1

iu_reset_op_c_t1

RAT

----> BOX716/OUT

0 iu_reset_op_c_t1

----> BOX716/IN

0 iu_reset_op_c_t1&0

---->{a} C2393/y

0 iu_reset_op_c

----> C2393/a

2043 gbfonet_6

```
----> gbfozell_6/y
```

gbfonet_6

----> gbfozell_6/a

78 N2031

---->{b} C2162/y

0 N2031

----> C2162/b

132 rcvry_reset q

102-103, 104-105, 106-107, 108-109, 110-111, 112-113, 114-115, 116-117, 118-119, 120-121, 122-123, 124-125, 126-127, 128-129, 130-131, 132-133, 134-135, 136-137, 138-139, 140-141, 142-143, 144-145, 146-147, 148-149, 150-151, 152-153, 154-155, 156-157, 158-159, 160-161, 162-163, 164-165, 166-167, 168-169, 170-171, 172-173, 174-175, 176-177, 178-179, 180-181, 182-183, 184-185, 186-187, 188-189, 190-191, 192-193, 194-195, 196-197, 198-199, 200-201, 202-203, 204-205, 206-207, 208-209, 210-211, 212-213, 214-215, 216-217, 218-219, 220-221, 222-223, 224-225, 226-227, 228-229, 230-231, 232-233, 234-235, 236-237, 238-239, 240-241, 242-243, 244-245, 246-247, 248-249, 250-251, 252-253, 254-255, 256-257, 258-259, 260-261, 262-263, 264-265, 266-267, 268-269, 270-271, 272-273, 274-275, 276-277, 278-279, 280-281, 282-283, 284-285, 286-287, 288-289, 290-291, 292-293, 294-295, 296-297, 298-299, 300-301, 302-303, 304-305, 306-307, 308-309, 310-311, 312-313, 314-315, 316-317, 318-319, 320-321, 322-323, 324-325, 326-327, 328-329, 330-331, 332-333, 334-335, 336-337, 338-339, 340-341, 342-343, 344-345, 346-347, 348-349, 350-351, 352-353, 354-355, 356-357, 358-359, 360-361, 362-363, 364-365, 366-367, 368-369, 370-371, 372-373, 374-375, 376-377, 378-379, 380-381, 382-383, 384-385, 386-387, 388-389, 390-391, 392-393, 394-395, 396-397, 398-399, 400-401, 402-403, 404-405, 406-407, 408-409, 410-411, 412-413, 414-415, 416-417, 418-419, 420-421, 422-423, 424-425, 426-427, 428-429, 430-431, 432-433, 434-435, 436-437, 438-439, 440-441, 442-443, 444-445, 446-447, 448-449, 450-451, 452-453, 454-455, 456-457, 458-459, 460-461, 462-463, 464-465, 466-467, 468-469, 470-471, 472-473, 474-475, 476-477, 478-479, 480-481, 482-483, 484-485, 486-487, 488-489, 490-491, 492-493, 494-495, 496-497, 498-499, 500-501, 502-503, 504-505, 506-507, 508-509, 510-511, 512-513, 514-515, 516-517, 518-519, 520-521, 522-523, 524-525, 526-527, 528-529, 530-531, 532-533, 534-535, 536-537, 538-539, 540-541, 542-543, 544-545, 546-547, 548-549, 550-551, 552-553, 554-555, 556-557, 558-559, 560-561, 562-563, 564-565, 566-567, 568-569, 570-571, 572-573, 574-575, 576-577, 578-579, 580-581, 582-583, 584-585, 586-587, 588-589, 590-591, 592-593, 594-595, 596-597, 598-599, 600-601, 602-603, 604-605, 606-607, 608-609, 610-611, 612-613, 614-615, 616-617, 618-619, 620-621, 622-623, 624-625, 626-627, 628-629, 630-631, 632-633, 634-635, 636-637, 638-639, 640-641, 642-643, 644-645, 646-647, 648-649, 650-651, 652-653, 654-655, 656-657, 658-659, 660-661, 662-663, 664-665, 666-667, 668-669, 670-671, 672-673, 674-675, 676-677, 678-679, 680-681, 682-683, 684-685, 686-687, 688-689, 690-691, 692-693, 694-695, 696-697, 698-699, 700-701, 702-703, 704-705, 706-707, 708-709, 710-711, 712-713, 714-715, 716-717, 718-719, 720-721, 722-723, 724-725, 726-727, 728-729, 730-731, 732-733, 734-735, 736-737, 738-739, 740-741, 742-743, 744-745, 746-747, 748-749, 750-751, 752-753, 754-755, 756-757, 758-759, 760-761, 762-763, 764-765, 766-767, 768-769, 770-771, 772-773, 774-775, 776-777, 778-779, 780-781, 782-783, 784-785, 786-787, 788-789, 790-791, 792-793, 794-795, 796-797, 798-799, 800-801, 802-803, 804-805, 806-807, 808-809, 810-811, 812-813, 814-815, 816-817, 818-819, 820-821, 822-823, 824-825, 826-827, 828-829, 830-831, 832-833, 834-835, 836-837, 838-839, 840-841, 842-843, 844-845, 846-847, 848-849, 850-851, 852-853, 854-855, 856-857, 858-859, 860-861, 862-863, 864-865, 866-867, 868-869, 870-871, 872-873, 874-875, 876-877, 878-879, 880-881, 882-883, 884-885, 886-887, 888-889, 890-891, 892-893, 894-895, 896-897, 898-899, 900-901, 902-903, 904-905, 906-907, 908-909, 910-911, 912-913, 914-915, 916-917, 918-919, 920-921, 922-923, 924-925, 926-927, 928-929, 930-931, 932-933, 934-935, 936-937, 938-939, 940-941, 942-943, 944-945, 946-947, 948-949, 950-951, 952-953, 954-955, 956-957, 958-959, 960-961, 962-963, 964-965, 966-967, 968-969, 970-971, 972-973, 974-975, 976-977, 978-979, 980-981, 982-983, 984-985, 986-987, 988-989, 990-991, 992-993, 994-995, 996-997, 998-999, 1000-1001, 1002-1003, 1004-1005, 1006-1007, 1008-1009

```

----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R   358 -1611  144  216 5 cl_invvn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+    160   N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+    160   N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
    > is_parm new_assert
    > set_slew_prop ON
[set_slew_prop]: Setting slew propagation to 1 (ON)
    > tc_parm {CHK_SINKSLEW( Y )}
    > tc_parm SLEW_LIM(100)
    > tc_parm CAP_LIM(100)
    > critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...
critical(
repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS),fantom(LIMITED),faninv(LIMITED));
-1873.06 Avg: -169.23
maximum area for proto box IDCDSUC is 4614
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
fantom: Found 152 valid buffers or inverters.
[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.
[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
-1873.06 Avg: -169.23
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.2 seconds.
[BD-500700]: Added 0 buffers.
[fantom]: Execution time was 0.0 seconds.
[BD-500701]: Added 0 inverters.
[faninv]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 24 times and applied 0 of them.
    > nextbox synexpand(XPANDVIEW)
[
>>]: nextbox( synexpand(XPANDVIEW) );
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names

```

```

[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
    > reset_critical_slack_limit
-1873.06 Avg: -169.23
resetting the current slack to -1873.0634
    > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
-1873.06 Avg: -169.23
maximum area for proto box IDCDSUC is 4614
setting SCORE option to ALL.
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1873.06 Avg: -169.23
ArrayNum: 6 ArrayMax: 906
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > tc_parm REGALL
    > repower_paths FUZZY(0.02)
initial slack is -1873
after repower paths slack is -1873
    > critical {repower(SCORE(ALL ),INC ,NO_VIOLATIONS), re...
critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))) );
-1873.06 Avg: -169.73
maximum area for proto box IDCDSUC is 4606
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1873.06 Avg: -169.73
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.2 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.2 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
    > compare_critical_slack_limit
-1873.06 Avg: -169.73
comparing new slack -1873.0634 to saved slack -1854.3328
    > reset_critical_slack_limit
-1873.06 Avg: -169.73
resetting the current slack to -1873.0634
    > quick tswap(SCORE(ALL),ACTUAL,ONE_LEVEL)
[
>>]: [quick]:( tswap(SCORE(ALL),ACTUAL,ONE_LEVEL) );
-1873.06 Avg: -169.73
setting SCORE option to ALL.
setting ACTUAL option.
setting ONE_LEVEL option.
maximum area for proto box IDCDSUC is 4606

```

[quick]: Number of boxes to process is 906.

[quick]: Number of boxes processed is 0.

-1865.06 Avg: -167.73

[BD-500304]: 52 pins swapped on 30 gates and 0 gates cloned.

[tswap]: Execution time was 5.6 seconds.

> tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),R...

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000

[tc_parm]: =====

*****POU92000-0107US1***** code invocation

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000

> critical repower(SCORE(ALL),REPOWER_GROUP(TAPERED),TAPER...

critical(repower(SCORE(ALL),REPOWER_GROUP(TAPERED),TAPERED_PIN_SWAP));

-1865.06 Avg: -167.73

maximum area for proto box IDCDSUC is 4606

repower: setting SCORE option to ALL.

repower: setting TAPERED_PIN_SWAP option.

Number of paths is 5

[BD-500278]: (W) Timing inconsistency box C2738

old slack = -1865.0580, new slack = -1866.9469

after reset, slack = -1866.9469

[BD-500278]: (W) Timing inconsistency box C2721.rwr

old slack = -1858.8082, new slack = -1863.1361

after reset, slack = -1863.1361

[BD-500278]: (W) Timing inconsistency box C2885

old slack = -1838.0586, new slack = -1843.3768

after reset, slack = -1843.3768

Number of paths is 5

[BD-502005]: The transform 1 reported a slack of -1828.6331, but made the worst slack worse

-1866.9470 from -1865.0580.

Number of paths is 5

Number of paths is 5

Number of paths is 5

Number of paths is 5

Number of paths is 5

Number of paths is 5

Number of paths is 5

Number of paths is 5

[BD-500026]: repower was applied 9 times.

Number of Tapered Cells = 11

[repower]: Execution time was 4.7 seconds.

[BD-502000]: Called transforms 66 times and applied 9 of them.

> critical repower(SCORE(ALL),NO_VIOLATIONS)

critical(repower(SCORE(ALL),NO_VIOLATIONS));

-1859.99 Avg: -165.68

maximum area for proto box IDCDSUC is 4654

repower: setting SCORE option to ALL.

repower: setting NO_VIOLATIONS option.

Number of paths is 5

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.2 seconds.

[BD-502000]: Called transforms 24 times and applied 0 of them.

```

> critical repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(...
critical( repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1859.99 Avg: -165.68
maximum area for proto box IDCDSUC is 4654
repower: setting SCORE option to ALL.
repower: setting NO_VIOLATIONS option.
Number of paths is 5
Number of paths is 5
Number of paths is 5
Number of paths is 5
Number of paths is 5
Number of paths is 5
Number of paths is 5
[BD-500026]: repower was applied 7 times.
[repower]: Execution time was 2.6 seconds.
[BD-502000]: Called transforms 46 times and applied 7 of them.
> tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFF...
> noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
repower: setting SCORE option to ALL.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -165.35
maximum area for proto box IDCDSUC is 4653.
-1859.99 Avg: -165.35
[noncritical]: noncritical applied to boxes with slack > 0.00.
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1859.99 Avg: -164.52
[BD-500026]: repower was applied 12 times.
[repower]: Execution time was 7.3 seconds.
> tc_parm MARGIN(10000000)
> compare_critical_slack_limit
-1859.99 Avg: -164.52
comparing new slack -1859.9940 to saved slack -1854.3328
> tc_parm OFFSET(0)
> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
> nextbox tkern
[
>>]: nextbox( tkern );
[tkern]: (W) No AND def - tkern will not apply.

[tkern]: generated patterns for 0 nets
> nextbox powerize
[
>>]: nextbox( powerize );
[BD-85000]: Changed power level of 0 patterns, added 0 patterns.
> quick_trecovery(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,NO...
[

```



```

>>]: [quick]:( trecover(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,NO1FAN,NO_VIOLATIONS) );
-1859.99 Avg: -164.52
[trecover]: setting SCORE option to ALL.
[trecover]: setting RE_POWER option.
[trecover]: setting INC mode.
[trecover]: setting PUSH option.
[trecover]: setting SORT_PINS option.
[trecover]: setting NO1FAN option.
[trecover]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.52
maximum area for proto box IDCDSUC is 4653
-1859.99 Avg: -164.52
Selected 384 critical boxes of 906 total.
[quick]: Number of boxes to process is 384.
[quick]: Number of boxes processed is 0.
-1859.99 Avg: -164.52
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[trecover]: 300 boxes checked 0 recovered
[trecover]: Execution time was 0.0 seconds.
    > reset_critical_slack_limit
-1859.99 Avg: -164.52
resetting the current slack to -1859.9940
    > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
-1859.99 Avg: -164.52
maximum area for proto box IDCDSUC is 4653
setting SCORE option to ALL.
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1859.99 Avg: -164.52
ArrayNum: 6 ArrayMax: 906
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > tc_parm REGALL
    > repower_paths FUZZY(0.02)
initial slack is -1860
after repower paths slack is -1860
    > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS), repower...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.

```

```
0 dcd succ last t1&0
```

```

----> C167/y          R C3+R  2859 -1860  3626 1011 1 cs_invv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          F C3+R  1079 -1860   30 139 4 cs_invv  01c NOT
1780 N675
---->{a} C2738/y      F C3+R  1079 -1860   30 139 4 cs_nnd2w  14b NAND
0 N675
----> C2738/a          R C3+R  1057 -1860   36 111 1 cs_nnd2w  14b NAND
22 last_cycle
---->{b} C2487/y      R C3+R  1057 -1860   36 111 1 cs_nnd2w  14e NAND
0 last_cycle
----> C2487/a          F C3+R  1035 -1860   21 142 3 cs_nnd2w  14e NAND
23 N1587
----> C1952/y          F C3+R  1035 -1860   21 142 3 cs_invv  19b NOT    0
N1587
----> C1952/a          R C3+R  1024 -1860   80 319 1 cs_invv  19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT       R C3+R  1024 -1860   80 319 1 IOPAD    IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN       R C3+R  1024 -1860   80 319 1 IOPAD    IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)   R C3+R  1024 -1860   80 319 1 PI      0
num_dcd_cyl(1)

```

```

2 iu_reset_op_c_t1    R C3+R  2671 -1672  3658 1011 1 PO      0
iu_reset_op_c_t1
RAT 999 0
----> BOX716/OUT       R C3+R  2671 -1672  3658 1011 1 IOPAD    IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN       R C3+R  2671 -1672  3658 1044 3 IOPAD    IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y      R C3+R  2671 -1672  3658 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R  566 -1672   109 196 6 cs_nnd2n  02c NAND
2104 gbfonet_6
----> gbfonet_6/y      F C3+R  566 -1672   109 196 6 cs_invv  09c NOT
0 gbfonet_6
----> gbfonet_6/a      R C3+R  490 -1672   206 43 1 cs_invv  09c NOT
77 N2031
---->{b} C2162/y      R C3+R  490 -1672   206 43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b          F C3+R  358 -1672   144 216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R  358 -1672   144 216 5 cl_invv  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2    R C3+  160  N/C   60 222 13 cl_invv  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2    R C3+  160  N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

3 local_milli_t2.reg_n.lat_0/a    F C3+R  2922 -1612   96 92 3 cl_invv  07c SRL
50 NET1056
Setup local_milli_t2.reg_n.lat_0/c1 F C3-  160      60 238 14 cl_invv  07c
1200 slow_mode.c1_4

```

```

---->{a} BOX789/y          F C3+R   2922  -1612   96   92  3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a             R C3+R   2862  -1612   120   32  1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y          R C3+R   2862  -1612   120   32  1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a             F C3+R   2781  -1612   158   19  1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y           F C3+R   2781  -1612   158   19  1 cs_ao12n  03c AOI
0 N1866
----> C2555/b              R C3+R   2671  -1612  3658  1044  3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y           R C3+R   2671  -1672  3658  1044  3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a              F C3+R   566   -1672   109   196  6 cs_nnd2n  02c NAND
2104 gbfonet_6
----> gbfozell_6/y         F C3+R   566   -1672   109   196  6 cs_invvn  09c NOT
0 gbfonet_6
----> gbfozell_6/a         R C3+R   490   -1672   206    43  1 cs_invvn  09c NOT
77 N2031
---->{e} C2162/y           R C3+R   490   -1672   206    43  1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b              F C3+R   358   -1672   144   216  5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/i2_out_n F C3+R   358   -1672   144   216  5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60   222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+    160   N/C    60   222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

-----
> hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
> hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao...
> hide -no_clear -cells { cs_buffe }
> hide -no_clear -cells { cs_invvn cs_invvv }
> hide -no_clear -cells { cs_nnd2f cs_nnd2g cs_nnd2n cs_nn...
> hide -no_clear -cells { cs_nnd3f cs_nnd3g cs_nnd3h cs_nn...
> hide -no_clear -cells { cs_nnd4n cs_nnd4v }
> hide -no_clear -cells { cs_nor2f cs_nor2g cs_nor2n cs_no...
> hide -no_clear -cells { cs_nor3f cs_nor3g cs_nor3h cs_no...
> hide -no_clear -cells { cs_oa12f cs_oa12g cs_oa12n cs_oa...
> hide -no_clear -cells { cs_oa21n cs_oa21v }
> hide -no_clear -cells { cs_oa22n cs_oa22v }
> hide -no_clear -cells { cs_xbn2n cs_xbn2v }
> hide -no_clear -cells { cs_xbo2n cs_xbo2v }
> find cell cs_*
> hide -no_clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f0...
> find cell cs_buffe*
> hide -no_clear -cells {cs_buffe01a cs_buffe02a cs_buffe0...
> hide -clear -cells { "cs_invvn" }
> find cell cs_invvn*c
> hide -clear -cells {cs_invvn01c cs_invvn02c cs_invvn03c ...
> hide -clear -cells { "cs_nnd2n" }
> find cell cs_nnd2n*c

```

```

> hide -clear -cells {cs_nnd2n02c cs_nnd2n03c cs_nnd2n04c ...
> hide -clear -cells { "cs_nnd3n" }
> find cell cs_nnd3n*c
> hide -clear -cells {cs_nnd3n02c cs_nnd3n03c cs_nnd3n04c ...
> hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*c
> hide -clear -cells {cs_nnd4n03c cs_nnd4n04c cs_nnd4n05c ...
> hide -clear -cells { "cs_nor2n" }
> find cell cs_nor2n*c
> hide -clear -cells {cs_nor2n02c cs_nor2n03c cs_nor2n04c ...
> hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*c
> hide -clear -cells {cs_nor3n03c cs_nor3n04c cs_nor3n05c ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*c
> hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*c
> hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*c
> hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
> hide -clear -cells { "cs_oa12n" }
> find cell cs_oa12n*c
> hide -clear -cells {cs_oa12n03c cs_oa12n04c cs_oa12n05c ...
> hide -clear -cells { "cs_oa21n" }
> find cell cs_oa21n*c
> hide -clear -cells {cs_oa21n03c cs_oa21n04c cs_oa21n05c ...
> hide -clear -cells { "cs_oa22n" }
> find cell cs_oa22n*c
> hide -clear -cells {cs_oa22n03c cs_oa22n04c cs_oa22n05c ...
> hide -clear -cells { "cs_buffe" }
> find cell cs_buffe*
> hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*c
> hide -clear -cells {cs_xbo2n01c cs_xbo2n02c cs_xbo2n03c ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*c
> hide -clear -cells {cs_xbn2n01c cs_xbn2n02c cs_xbn2n03c ...
> scritflow {trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMP...
[critflow]: trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS CHECK_INPUTS
MIN_INPUTS( 2 ) )
[Hpattern]: (W) Unable to build pattern for 'AND1 (AND)'
[trestructure]: Thresholds: Inputs=2 Slack=-0.000
[trestructure]: MaxInputs=4 MaxDecompose=4 DoubleInverters=true
[trestructure]: SortPins=true ReduceArea=false
[trestructure]: CheckInputs=true PartialTrees=false
[trestructure]: IgnoreHideFlags=false TibOnly=false
[trestructure]: MatchEffort=2 DebugNet=none
[critflow]: Critical Slack = -1859.994
[padnet]: Added 9 IOPADs.
[
>>]: nextbox( genmark() );
[

```

```

>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 24 signals, 14 usage boxes and 22 connections.
[unpadnet]: Removed 9 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
        The model has 13 signals, 3 usage boxes and 11 connections.
[Hdecompose]: Inserted 11 pairs of double inverters.
[cleanup]: 46 boxes disconnected
[sweep]: sweep deleted 35 signals and 8 usage boxes.
        The model has 20 signals, 10 usage boxes and 18 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(1)
[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(0)
[trestructure]: (W) Covering is invalid due to electrical violation at input ia_to_if_q
[trestructure]: (W) Covering is invalid due to electrical violation at input mia_to_if_q
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
[
>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 22 signals, 14 usage boxes and 20 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 4 boxes disconnected
[sweep]: sweep deleted 4 signals and 0 usage boxes.
        The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 5 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 32 signals and 2 usage boxes.

```

The model has 13 signals, 5 usage boxes and 11 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input ireg_valid&0

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 7 IOPADs.

```
[
>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
```

The model has 20 signals, 12 usage boxes and 18 connections.

```
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
```

The model has 11 signals, 3 usage boxes and 9 connections.

```
[Hdecompose]: Inserted 9 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 31 signals and 6 usage boxes.
```

The model has 18 signals, 10 usage boxes and 16 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input op_cmp_raw&0

[trestructure]: (W) Covering is invalid due to electrical violation at input frc_blk_1cyc_q

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 3 IOPADs.

```
[
>>]: nextbox( genmark() );
[
>>]: nextnet( geninv() );
[
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
```

The model has 8 signals, 4 usage boxes and 6 connections.

```
[unpadnet]: Removed 3 IOPADs.
[cleanup]: 0 boxes disconnected
```

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 5 signals, 1 usage boxes and 3 connections.

[Hdecompose]: Inserted 3 pairs of double inverters.

[cleanup]: 7 boxes disconnected

[sweep]: sweep deleted 6 signals and 0 usage boxes.

The model has 5 signals, 1 usage boxes and 3 connections.

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 4 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 12 signals, 7 usage boxes and 10 connections.

[unpadnet]: Removed 4 IOPADs.

[cleanup]: 2 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 6 signals, 1 usage boxes and 4 connections.

[Hdecompose]: Inserted 4 pairs of double inverters.

[cleanup]: 16 boxes disconnected

[sweep]: sweep deleted 12 signals and 2 usage boxes.

The model has 8 signals, 3 usage boxes and 6 connections.

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[padnet]: Added 4 IOPADs.

[

>>]: nextbox(genmark());

[

>>]: nextnet(geninv());

[

>>]: nextbox(twoin() onein() invrem());

[BD-40550]: Removed 0 redundant pins.

[twoin]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.

[onein]: Execution time was 0.0 seconds.

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[cleanup]: 0 boxes disconnected

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 14 signals, 9 usage boxes and 12 connections.

[unpadnet]: Removed 4 IOPADs.

[cleanup]: 2 boxes disconnected

[sweep]: sweep deleted 2 signals and 0 usage boxes.

The model has 8 signals, 3 usage boxes and 6 connections.

[Hdecompose]: Inserted 2 pairs of double inverters.

[cleanup]: 11 boxes disconnected

[sweep]: sweep deleted 8 signals and 5 usage boxes.

The model has 10 signals, 5 usage boxes and 8 connections.

[trestructure]: (W) Covering is invalid due to electrical violation at input blk_mkend_q

[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.

[trestructure]: Rebuilt 0 logic trees

[trestructure]: Execution time was 22.9 seconds.

> sweep

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 1129 signals, 906 usage boxes and 1744 connections.

```
> hide -clear -cells { "cs_invvn" }
> find cell cs_invvn*
> hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...
> hide -clear -cells { "cs_nnd2n" }
> find cell cs_nnd2n*
> hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...
> hide -clear -cells { "cs_nnd3n" }
> find cell cs_nnd3n*
> hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
> hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*
> hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
> hide -clear -cells { "cs_nor2n" }
> find cell cs_nor2n*
> hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
> hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*
> hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
> hide -clear -cells { "cs_ao12n" }
> find cell cs_ao12n*
> hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
> hide -clear -cells { "cs_ao21n" }
> find cell cs_ao21n*
> hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
> hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*
> hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
> hide -clear -cells { "cs_oa12n" }
> find cell cs_oa12n*
> hide -clear -cells {cs_oa12n03b cs_oa12n03c cs_oa12n03d ...
> hide -clear -cells { "cs_oa21n" }
> find cell cs_oa21n*
> hide -clear -cells {cs_oa21n03b cs_oa21n03c cs_oa21n03d ...
> hide -clear -cells { "cs_oa22n" }
> find cell cs_oa22n*
> hide -clear -cells {cs_oa22n03b cs_oa22n03c cs_oa22n03d ...
> hide -clear -cells { "cs_buffe" }
> find cell cs_buffe*
> hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
> hide -clear -cells { "cs_xbo2n" }
> find cell cs_xbo2n*
```

```

> hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
> hide -clear -cells { "cs_xbn2n" }
> find cell cs_xbn2n*
> hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
  > hide -clear -cells { cs_ao12f }
  > find cell cs_ao12f*
  > hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
  > hide -clear -cells { cs_nnd2f cs_nnd2w }
  > find cell cs_nnd2f*
  > hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
  > find cell cs_nnd2w*
  > hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
  > hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
  > find cell cs_nnd3f*
  > hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
  > find cell cs_nnd3h*
  > hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
  > find cell cs_nnd3w*
  > hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
  > find cell cs_nnd3y*
  > hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
  > hide -clear -cells { cs_nor2f cs_nor2w }
  > find cell cs_nor2f*
  > hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...
  > find cell cs_nor2w*
  > hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...
  > hide -clear -cells { cs_nor3f cs_nor3h }
  > find cell cs_nor3f*
  > hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
  > find cell cs_nor3h*
  > hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
  > hide -clear -cells { cs_ao12f }
  > find cell cs_ao12f*
  > hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
  > hide -clear -cells { "cs_invvv" }
  > find cell cs_invvv*
  > hide -clear -cells {cs_invvv01b cs_invvv01c cs_invvv01d ...
  > hide -clear -cells { cs_ao12v cs_ao12g }
  > find cell cs_ao12v*
  > hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
  > find cell cs_ao12g*
  > hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
  > hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
  > find cell cs_nnd2v*
  > hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
  > find cell cs_nnd2g*
  > hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
  > find cell cs_nnd2x*
  > hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
  > hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
  > find cell cs_nnd3v*
  > hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
  > find cell cs_nnd3g*
  > hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
  > find cell cs_nnd3i*

```

```

> hide -clear -cells {cs_nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
> find cell cs_nnd3x*
> hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
> find cell cs_nnd3z*
> hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
> hide -clear -cells { cs_nnd4v }
> find cell cs_nnd4v*
> hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
> hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
> find cell cs_nor2v*
> hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
> find cell cs_nor2g*
> hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
> find cell cs_nor2x*
> hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
> hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
> find cell cs_nor3v*
> hide -clear -cells {cs_nor3v03b cs_nor3v03c cs_nor3v03d ...
> find cell cs_nor3g*
> hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...
> find cell cs_nor3i*
> hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
> hide -clear -cells { cs_oa12v cs_oa12g }
> find cell cs_oa12v*
> hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
> find cell cs_oa12g*
> hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
> tc_parm OFFSET(0)
> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1)
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: =====
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
> critical texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PI...
critical( texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
-1859.99 Avg: -164.32
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[txpao]: applied 0 times
[txpao]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
> critical texpand(SCORE(ALL),PUSH,RE_POWER,INC,SORT_PINS,...
critical(
txpand(SCORE(ALL),PUSH,RE_POWER,INC,SORT_PINS,SIMILAR,VIEW(TRUE_BASE_AUTOGEN)
,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
[txpand]: setting SCORE option to ALL.
[txpand]: setting PUSH option.
[txpand]: setting RE_POWER option.
[txpand]: setting INC mode.

```

```

[teexpand]: setting SORT_PINS option.
[teexpand]: setting SIMILAR option.
[teexpand]: explicit VIEWS used.
[teexpand]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
[teexpand]: TRUE view TRUE_BASE_AUTOGEN was found.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[teexpand]: Execution time was 0.0 seconds.
[BD-502600]: 0 gates checked and 0 expanded.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > tc_parm REGALL
    > critical repower(SCORE(ALL),INC,NO_VIOLATIONS)
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
    > echo {doing last techredund}
doing last techredund
    > traceset {syntrace HOWMANY}
[traceset]: trace string = syntrace HOWMANY
[tracing]: set trace variable syntrace to 20
    > str_parm tgfs_effort
    > is_parm no_tech_redund
    > is_parm remove_redundant_regs
    > make_constants_in nonreg_only
    > ignore_trivial_expansions EQNVIEW
    > expansions_from_tib EQNVIEW
    > expansions_from_eqn EQNVIEW
    > copy_def_to_proto EQNVIEW
    > apply_decide_boolean(EQNVIEW)
generated 1 paths in 70 milliseconds
    > apply Hstructure(EQNVIEW)
generated 1 paths in 30 milliseconds
    > gen_nonreg_tib_expns TIB_EXPANSIONS
    > apply Hunstructure()
    > expandable_name
        > set_nochange
        > constmod
        > is_parm keep_bad_pgroups
        > bad_pgroups_expandable
        > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
[
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(EQNVIEW)) );
[

```

```

>>]: nextbox( SASname(RESTORE) );
[sysasname]: Restored 0 BRKPT net names
[sysasname]: Restored 189 REG and SEQUENTIAL output net names
[sysasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 906 objects as matching keyword criteria.
[
>>]: nextbox( SASname(PROTECT) );
[sysasname]: Protected 180 BRKPT net names
[sysasname]: Protected 189 REG and SEQUENTIAL output net names
[sysasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 1129 signals, 906 usage boxes and 1744 connections.
[simple_expand]: Modified 0 gates.
        > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
[
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(TIB_EXPANSIONS)) );
[
>>]: nextbox( SASname(RESTORE) );
[sysasname]: Restored 0 BRKPT net names
[sysasname]: Restored 189 REG and SEQUENTIAL output net names
[sysasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 906 objects as matching keyword criteria.
[
>>]: nextbox( SASname(PROTECT) );
[sysasname]: Protected 180 BRKPT net names
[sysasname]: Protected 189 REG and SEQUENTIAL output net names
[sysasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 1129 signals, 906 usage boxes and 1744 connections.
[simple_expand]: Modified 0 gates.
        > headless
[headless]: Removed 0 boxes
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 1129 signals, 906 usage boxes and 1744 connections.
        > cleanse1
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
        The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
        > nochange

```

```

    > set_nochange
    > apply {Hstructure( EQNVIEW TIB_EXPANSIONS)}
generated 1 paths in 60 milliseconds
    > rtolbox {Htgfsredund( 100 )}
[
>>]: rtolbox( Htgfsredund( 100 ) );
[BD-330500]: Out of 2890 faults found 0 redundancies, eliminated 0, could not decide 0 in 2 seconds.
    > apply Hunstructure()
    > nochange
    > DeleteAllProtosUnderView TIB_EXPANSIONS
[SRULE-17175]: Deleted 5 Proto Boxes
    > randsim q
[
>>]: randsim( q );
    > randsim q
[
>>]: randsim( q );
    > is_parm keep_bad_pgroups
    > copyinfo
    > fix_bad_pgroups
[BD-82400]: Added 0 terminators, deleted 0 pins and tied 0 pins.
    > basetype
[
>>]: nextbox_with_test( test_syn_hide(!HIDE_MAP),genmark );
[test_syn_hide]: Number of objects selected was 906 of 906 checked.
[
>>]: nextnet( geninv );
    > copyinfo
    > nextbox {mapprim, mapterm}
[
>>]: nextbox( mapprim, mapterm );
[mapprim]: Execution time was 0.0 seconds.
[BD-83600]: 0 terminators processed 0 dummy nets removed.
    > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1129 signals, 906 usage boxes and 1744 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
    The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.

```

[twain]: Execution time was 0.0 seconds.

setting NO_VIOLATIONS option.

-1859.99 Avg: -164.32

ArrayNum: 6 ArrayMax: 906

[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.

[tswap]: Execution time was 0.1 seconds.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> critical {repower(SCORE(ALL),INC,NO_VIOLATIONS)}

critical(repower(SCORE(ALL),INC,NO_VIOLATIONS));

-1859.99 Avg: -164.32

maximum area for proto box IDCDSUC is 4664

repower: setting SCORE option to ALL.

repower: setting INC mode.

repower: setting NO_VIOLATIONS option.

-1859.99 Avg: -164.32

ArrayNum: 6 ArrayMax: 906

[BD-500026]: repower was applied 0 times.

[repower]: Execution time was 0.0 seconds.

[BD-502000]: Called transforms 6 times and applied 0 of them.

> compare_key_slack_limit TIME_REDUND

-1859.99 Avg: -164.32

comparing keyed new slack -1859.9940 to keyed saved slack -1841.3940

> delete_key_slack_limit TIME_REDUND

> quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)

[

>>]: [quick]:(onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS));

-1859.99 Avg: -164.32

[onebuff]: setting SCORE option to ALL:

[onebuff]: setting RE_POWER option.

[onebuff]: setting INC mode.

[onebuff]: setting NO_VIOLATIONS option.

-1859.99 Avg: -164.32

maximum area for proto box IDCDSUC is 4664

[quick]: Number of boxes to process is 906.

[quick]: Number of boxes processed is 0.

-1859.99 Avg: -164.32

[onebuff]: was applied 0 times

> quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)

[

>>]: [quick]:(dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS));

-1859.99 Avg: -164.32

setting SCORE option to ALL.

setting RE_POWER option.

setting INC mode.

setting NO_VIOLATIONS option.

-1859.99 Avg: -164.32

maximum area for proto box IDCDSUC is 4664

[quick]: Number of boxes to process is 906.

[quick]: Number of boxes processed is 0.

-1859.99 Avg: -164.32

[BD-500500]: Moved 0 sinks and removed 0 inverters.

> critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...

critical(

repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOLATIONS),fantom(LIMITED),faninv(LIMITED));

-1859.99 Avg: -164.32

maximum area for proto box IDCDSUC is 4664
 repower: setting SCORE option to ALL.
 repower: setting INC mode.
 repower: setting NO_VIOLATIONS option.
 setting SCORE option to ALL.
 setting ACTUAL option.
 setting RE_POWER option.
 setting INC mode.
 setting NO_VIOLATIONS option.
 phantom: Found 152 valid buffers or inverters.
 [BD-500718]: phantom too many buffers and/or inverters 152, may slow down optimizations.
 [BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
 -1859.99 Avg: -164.32
 ArrayNum: 6 ArrayMax: 906
 [BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.0 seconds.
 [BD-500100]: 0 parallel copies of gates were made.
 [clone]: Execution time was 0.1 seconds.
 [BD-500700]: Added 0 buffers.
 [phantom]: Execution time was 0.0 seconds.
 [BD-500701]: Added 0 inverters.
 [faninv]: Execution time was 0.0 seconds.
 [BD-502000]: Called transforms 24 times and applied 0 of them.
 > nextbox synexpand(XPANDVIEW)
 [
 >>]: nextbox(synexpand(XPANDVIEW));
 [
 >>]: nextbox(SASname(RESTORE));
 [synsasname]: Restored 0 BRKPT net names
 [synsasname]: Restored 189 REG and SEQUENTIAL output net names
 [synsasname]: Execution time was 0.0 seconds.
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
 The model has 1129 signals, 906 usage boxes and 1744 connections.
 [
 >>]: nextbox(SASname(PROTECT));
 [synsasname]: Protected 180 BRKPT net names
 [synsasname]: Protected 189 REG and SEQUENTIAL output net names
 [synsasname]: Execution time was 0.0 seconds.
 [synexpand]: expanded 0 boxes
 > reset_critical_slack_limit
 -1859.99 Avg: -164.32
 resetting the current slack to -1859.9940
 > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
 critical(tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS));
 -1859.99 Avg: -164.32
 maximum area for proto box IDCDSUC is 4664
 setting SCORE option to ALL.
 setting ESTIMATED option.
 setting TWO_LEVEL option.
 setting NO_VIOLATIONS option.
 -1859.99 Avg: -164.32
 ArrayNum: 6 ArrayMax: 906
 [BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
 [tswap]: Execution time was 0.0 seconds.
 [BD-502000]: Called transforms 6 times and applied 0 of them.

```

    > tc_parm REGALL
    > repower_paths FUZZY(0.02)
initial slack is -1860
after repower paths slack is -1860
    > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS), re...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
    > compare_critical_slack_limit
-1859.99 Avg: -164.32
comparing new slack -1859.9940 to saved slack -1841.3940
    > tc_parm {SLEW_LIM(120),CAP_LIM(120), SINK_LIM(120)}
    > critical onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),...
critical(
onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),dinv(SCORE(ALL),RE_POWER,INC,NO_VI
OLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting INC mode.
[onebuff]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
    setting SCORE option to ALL.
    setting RE_POWER option.
    setting INC mode.
    setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[onebuff]: was applied 0 times
[BD-500500]: Moved 0 sinks and removed 0 inverters.
[BD-502000]: Called transforms 12 times and applied 0 of them.
    > tc_parm {SLEW_LIM(100),CAP_LIM(100), SINK_LIM(100)}
    > critical clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIO...
critical( clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.

```



```

----> BOX714/IN          R C3+R  2859 -1860  3626 1011 1 IOPAD  IOPAD
0 dcd_succ_last_t1&0
----> C167/y             R C3+R  2859 -1860  3626 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0
----> C167/a             F C3+R  1079 -1860   30  139 4 cs_invvn 01c NOT
1780 N675
----> {a} C2738/y        F C3+R  1079 -1860   30  139 4 cs_nnd2w 14b NAND
0 N675
----> C2738/a            R C3+R  1057 -1860   36  111 1 cs_nnd2w 14b NAND
22 last_cycle
----> {b} C2487/y        R C3+R  1057 -1860   36  111 1 cs_nnd2w 14e NAND
0 last_cycle
----> C2487/a            F C3+R  1035 -1860   21  142 3 cs_nnd2w 14e NAND
23 N1587
----> C1952/y            F C3+R  1035 -1860   21  142 3 cs_invvv 19b NOT    0
N1587
----> C1952/a            R C3+R  1024 -1860   80  319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT          R C3+R  1024 -1860   80  319 1 IOPAD  IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN          R C3+R  1024 -1860   80  319 1 IOPAD  IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)      R C3+R  1024 -1860   80  319 1 PI      0
num_dcd_cyl(1)

```

```

--
2 iu_reset_op_c_t1      R C3+R  2671 -1672  3658 1011 1 PO      0
iu_reset_op_c_t1
RAT 999 0
----> BOX716/OUT          R C3+R  2671 -1672  3658 1011 1 IOPAD  IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN          R C3+R  2671 -1672  3658 1044 3 IOPAD  IOPAD
0 iu_reset_op_c_t1&0
----> {a} C2393/y        R C3+R  2671 -1672  3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a            F C3+R  566 -1672   109  196 6 cs_nnd2n 02c NAND
2104 gbfonet_6
----> gbfozell_6/y       F C3+R  566 -1672   109  196 6 cs_invvn 09c NOT
0 gbfonet_6
----> gbfozell_6/a       R C3+R  490 -1672   206   43 1 cs_invvn 09c NOT
77 N2031
----> {b} C2162/y        R C3+R  490 -1672   206   43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b            F C3+R  358 -1672   144  216 5 cs_nnd3n 02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/12_out_n F C3+R  358 -1672   144  216 5 cl_invvn 07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+  160  N/C   60  222 13 cl_invvn 07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+  160  N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
3 local_milli_t2.reg_n.lat_0/a F C3+R  2922 -1612   96  92 3 cl_invvn 07c SRL
50 NET1056

```

Setup local_milli_t2.reg_n.lat_0/c1	F C3-	160	60	238	14	cl_invn	07c
1200 slow_mode.c1_4							
---->{a} BOX789/y	F C3+R	2922	-1612	96	92	3 cs_nnd3z	07c NAND
0 NET1056							
----> BOX789/a	R C3+R	2862	-1612	120	32	1 cs_nnd3z	07c NAND
60 NET1054							
---->{b} BOX785/y	R C3+R	2862	-1612	120	32	1 cs_nnd2f	03c NAND
0 NET1054							
----> BOX785/a	F C3+R	2781	-1612	158	19	1 cs_nnd2f	03c NAND
81 N1866							
---->{c} C2555/y	F C3+R	2781	-1612	158	19	1 cs_ao12n	03c AOI
0 N1866							
----> C2555/b	R C3+R	2671	-1612	3658	1044	3 cs_ao12n	03c AOI
110 iu_reset_op_c_t1&0							
---->{d} C2393/y	R C3+R	2671	-1672	3658	1044	3 cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	566	-1672	109	196	6 cs_nnd2n	02c NAND
2104 gbfonet_6							
----> gbfonet_6/y	F C3+R	566	-1672	109	196	6 cs_invn	09c NOT
0 gbfonet_6							
----> gbfonet_6/a	R C3+R	490	-1672	206	43	1 cs_invn	09c NOT
77 N2031							
---->{e} C2162/y	R C3+R	490	-1672	206	43	1 cs_nnd3n	02c NAND
0 N2031							
----> C2162/b	F C3+R	358	-1672	144	216	5 cs_nnd3n	02c NAND
132 rcvry_reset_q							
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R	358	-1672	144	216	5 cl_invn	07d
SRL 0 rcvry_reset_q							
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13 cl_invn	07d SRL
198 slow_mode.c2_1							
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13 cb_clk_32_1	LCB
0 slow_mode.c2_1							

```

> tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
> noncritical onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_...
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting LOWEST mode.
[onebuff]: setting WORST option.
[onebuff]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
-1859.99 Avg: -164.32
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1859.99 Avg: -164.32
[onebuff]: was applied 0 times
> noncritical dinv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIO...
setting SCORE option to ALL.
setting RE_POWER option.
setting LOWEST mode.
setting WORST option.
setting NO_VIOLATIONS option.

```

```
0 dcd_succ last t1
```


Setup local_milli_t2.reg_n.lat_0/c1	F C3-	160	60	238	14	cl_invv	07c
1200 slow_mode.c1_4							
---->{a} BOX789/y	F C3+R	2922	-1612	96	92	3 cs_nnd3z	07c NAND
0 NET1056							
----> BOX789/a	R C3+R	2862	-1612	120	32	1 cs_nnd3z	07c NAND
60 NET1054							
---->{b} BOX785/y	R C3+R	2862	-1612	120	32	1 cs_nnd2f	03c NAND
0 NET1054							
----> BOX785/a	F C3+R	2781	-1612	158	19	1 cs_nnd2f	03c NAND
81 N1866							
---->{c} C2555/y	F C3+R	2781	-1612	158	19	1 cs_ao12n	03c AOI
0 N1866							
----> C2555/b	R C3+R	2671	-1612	3658	1044	3 cs_ao12n	03c AOI
110 iu_reset_op_c_t1&0							
---->{d} C2393/y	R C3+R	2671	-1672	3658	1044	3 cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	566	-1672	109	196	6 cs_nnd2n	02c NAND
2104 gbfonet_6							
----> gbfonet_6/y	F C3+R	566	-1672	109	196	6 cs_invv	09c NOT
0 gbfonet_6							
----> gbfonet_6/a	R C3+R	490	-1672	206	43	1 cs_invv	09c NOT
77 N2031							
---->{e} C2162/y	R C3+R	490	-1672	206	43	1 cs_nnd3n	02c NAND
0 N2031							
----> C2162/b	F C3+R	358	-1672	144	216	5 cs_nnd3n	02c NAND
132 rcvry_reset_q							
----> rcvry_reset.reg_n.lat_0/2_out_n	F C3+R	358	-1672	144	216	5 cl_invv	07d
SRL 0 rcvry_reset_q							
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13 cl_invv	07d SRL
198 slow_mode.c2_1							
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13 cb_clk_32_1	LCB
0 slow_mode.c2_1							

> reset_critical_slack_limit
-1859.99 Avg: -164.32
resetting the current slack to -1859.9940
> write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:08:18 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

ARRIVAL TIME + ADJUST)
 Clock Gating Hold CkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 ARRIVAL TIME + ADJUST)
 Clock Tree Pulse Width CkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 ADJUST)
 Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth CkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 ClockSeparation CkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj
1 dcd_succ_last_t1	R C3+R	2859	-1860	3626	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	R C3+R	2859	-1860	3626	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2859	-1860	3626	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2859	-1860	3626	1011	1 cs_invvn	01c NOT	
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1079	-1860	30	139	4 cs_invvn	01c NOT	
1780 N675								
---->{a} C2738/y	F C3+R	1079	-1860	30	139	4 cs_nnd2w	14b NAND	
0 N675								
----> C2738/a	R C3+R	1057	-1860	36	111	1 cs_nnd2w	14b NAND	
22 last_cycle								
---->{b} C2487/y	R C3+R	1057	-1860	36	111	1 cs_nnd2w	14e NAND	
0 last_cycle								
----> C2487/a	F C3+R	1035	-1860	21	142	3 cs_nnd2w	14e NAND	
23 N1587								
----> C1952/y	F C3+R	1035	-1860	21	142	3 cs_invvv	19b NOT	0
N1587								
----> C1952/a	R C3+R	1024	-1860	80	319	1 cs_invvv	19b NOT	
11 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1860	80	319	1 IOPAD	IOPAD	
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1860	80	319	1 IOPAD	IOPAD	0
num_dcd_cyl(1)								
----> num_dcd_cyl(1)	R C3+R	1024	-1860	80	319	1 PI		0
num_dcd_cyl(1)								

2 iu_reset_op_c_t1	R C3+R	2671	-1672	3658	1011	1	PO	0
iu_reset_op_c_t1								
RAT	999					0		
----> BOX716/OUT	R C3+R	2671	-1672	3658	1011	1	IOPAD	IOPAD
0 iu_reset_op_c_t1								
----> BOX716/IN	R C3+R	2671	-1672	3658	1044	3	IOPAD	IOPAD
0 iu_reset_op_c_t1&0								
---->{a} C2393/y	R C3+R	2671	-1672	3658	1044	3	cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0								
----> C2393/a	F C3+R	566	-1672	109	196	6	cs_nnd2n	02c NAND
2104 gbfonet_6								
----> gbfonet_6/y	F C3+R	566	-1672	109	196	6	cs_invvn	09c NOT
0 gbfonet_6								
----> gbfonet_6/a	R C3+R	490	-1672	206	43	1	cs_invvn	09c NOT
77 N2031								
---->{b} C2162/y	R C3+R	490	-1672	206	43	1	cs_nnd3n	02c NAND
0 N2031								
----> C2162/b	F C3+R	358	-1672	144	216	5	cs_nnd3n	02c NAND
132 rcvry_reset_q								
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R	358	-1672	144	216	5	cl_invvn	07d
SRL 0 rcvry_reset_q								
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_invvn	07d SRL
198 slow_mode.c2_1								
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB
0 slow_mode.c2_1								

3 local_milli_t2.reg_n.lat_0/a	F C3+R	2922	-1612	96	92	3	cl_invvn	07c SRL
50 NET1056								
Setup local_milli_t2.reg_n.lat_0/c1	F C3-	160		60	238	14	cl_invvn	07c
1200 slow_mode.c1_4								
---->{a} BOX789/y	F C3+R	2922	-1612	96	92	3	cs_nnd3z	07c NAND
0 NET1056								
----> BOX789/a	R C3+R	2862	-1612	120	32	1	cs_nnd3z	07c NAND
60 NET1054								
---->{b} BOX785/y	R C3+R	2862	-1612	120	32	1	cs_nnd2f	03c NAND
0 NET1054								
----> BOX785/a	F C3+R	2781	-1612	158	19	1	cs_nnd2f	03c NAND
81 N1866								
---->{c} C2555/y	F C3+R	2781	-1612	158	19	1	cs_ao12n	03c AOI
0 N1866								
----> C2555/b	R C3+R	2671	-1612	3658	1044	3	cs_ao12n	03c AOI
110 iu_reset_op_c_t1&0								
---->{d} C2393/y	R C3+R	2671	-1672	3658	1044	3	cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0								
----> C2393/a	F C3+R	566	-1672	109	196	6	cs_nnd2n	02c NAND
2104 gbfonet_6								
----> gbfonet_6/y	F C3+R	566	-1672	109	196	6	cs_invvn	09c NOT
0 gbfonet_6								
----> gbfonet_6/a	R C3+R	490	-1672	206	43	1	cs_invvn	09c NOT
77 N2031								
---->{e} C2162/y	R C3+R	490	-1672	206	43	1	cs_nnd3n	02c NAND
0 N2031								
----> C2162/b	F C3+R	358	-1672	144	216	5	cs_nnd3n	02c NAND
132 rcvry_reset_q								

```

----> rcvry_reset.reg_n.lat_0/i2_out_n      F C3+R   358 -1672  144  216 5 cl_invn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2              R C3+    160   N/C   60  222 13 cl_invn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2                R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
    4 local_milli_t1.reg_n.lat_0/a          F C3+R   2922 -1612   96   92 3 cl_invn  07c SRL
50 NET1056
Setup local_milli_t1.reg_n.lat_0/c1        F C3-    160           60  238 14 cl_invn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                          F C3+R   2922 -1612   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                             R C3+R   2862 -1612  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                          R C3+R   2862 -1612  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                             F C3+R   2781 -1612  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                          F C3+R   2781 -1612  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                             R C3+R   2671 -1612  3658 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                          R C3+R   2671 -1672  3658 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                             F C3+R   566 -1672  109  196 6 cs_nnd2n  02c NAND
2104 gbfonet_6
----> gbfozell_6/y                        F C3+R   566 -1672  109  196 6 cs_invn  09c NOT
0 gbfonet_6
----> gbfozell_6/a                        R C3+R   490 -1672  206   43 1 cs_invn  09c NOT
77 N2031
---->{e} C2162/y                          R C3+R   490 -1672  206   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b                             F C3+R   358 -1672  144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/i2_out_n      F C3+R   358 -1672  144  216 5 cl_invn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2              R C3+    160   N/C   60  222 13 cl_invn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2                R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
    5 local_milli.reg_n.lat_0/a          F C3+R   2922 -1612   96   92 3 cl_invn  07c SRL
50 NET1056
Setup local_milli.reg_n.lat_0/c1          F C3-    160           60  238 14 cl_invn  07c  1200
slow_mode.c1_2
---->{a} BOX789/y                          F C3+R   2922 -1612   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                             R C3+R   2862 -1612  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                          R C3+R   2862 -1612  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                             F C3+R   2781 -1612  158   19 1 cs_nnd2f  03c NAND

```

```

81 N1866
---->{c} C2555/y          F C3+R   2781  -1612   158   19 1 cs_ao12n   03c AOI
0 N1866
----> C2555/b            R C3+R   2671  -1612   3658  1044 3 cs_ao12n   03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y          R C3+R   2671  -1672   3658  1044 3 cs_nnd2n   02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a            F C3+R   566   -1672   109   196 6 cs_nnd2n   02c NAND
2104 gbfonet_6
----> gbfonet_6/y        F C3+R   566   -1672   109   196 6 cs_invvn   09c NOT
0 gbfonet_6
----> gbfonet_6/a        R C3+R   490   -1672   206    43 1 cs_invvn   09c NOT
77 N2031
---->{e} C2162/y          R C3+R   490   -1672   206    43 1 cs_nnd3n   02c NAND
0 N2031
----> C2162/b            F C3+R   358   -1672   144   216 5 cs_nnd3n   02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R   358   -1672   144   216 5 cl_invvn   07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2        R C3+    160    N/C    60   222 13 cl_invvn   07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160    N/C    60   222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

> repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}

initial slack is -1860

total pct of low vt boxes initially is 0.6441

box count 621, pct of low vt boxes added is 0.9662

total pct of low vt boxes used is .1127

after repower paths slack is -1672

> write_end_point_report -points 5

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:08:19 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont   Slack due to a point downstream on path
Required Arrival Time    RAT        ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT   ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup       ClkGSet   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold        ClkGHld   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width   ClkTPW   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                    Setup     ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +

```

ADJUST)
 Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	-------------------------------------

1 iu_reset_op_c_t1	R C3+R	2671	-1672	3658	1011	1 PO	0
iu_reset_op_c_t1							
RAT	999					0	
----> BOX716/OUT	R C3+R	2671	-1672	3658	1011	1 IOPAD	IOPAD
0 iu_reset_op_c_t1							
----> BOX716/IN	R C3+R	2671	-1672	3658	1044	3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0							
---->{a} C2393/y	R C3+R	2671	-1672	3658	1044	3 cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	566	-1672	109	196	6 cs_nnd2n	02c NAND
2104 gbfonet_6							
----> gbfozell_6/y	F C3+R	566	-1672	109	196	6 cs_invvn	09c NOT
0 gbfonet_6							
----> gbfozell_6/a	R C3+R	490	-1672	206	43	1 cs_invvn	09c NOT
77 N2031							
---->{b} C2162/y	R C3+R	490	-1672	206	43	1 cs_nnd3n	02c NAND
0 N2031							
----> C2162/b	F C3+R	358	-1672	144	216	5 cs_nnd3n	02c NAND
132 rcvry_reset_q							
----> rcvry_reset.reg_n.lat_0/2_out_n	F C3+R	358	-1672	144	216	5 cl_invvn	07d
SRL 0 rcvry_reset_q							
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13 cl_invvn	07d SRL
198 slow_mode.c2_1							
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13 cb_clk_32_1	LCB
0 slow_mode.c2_1							

2 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT

```

1594 N675
---->{a} C2738/y      F C3+R   1075 -1669   27  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/a         R C3+R   1056 -1669   33  114 1 cs_nnd2x  14b NAND
19 last_cycle
---->{b} C2487/y      R C3+R   1056 -1669   33  114 1 cs_nnd2x  14e NAND
0 last_cycle
----> C2487/a         F C3+R   1035 -1669   22  145 3 cs_nnd2x  14e NAND
21 N1587
----> C1952/y         F C3+R   1035 -1669   22  145 3 cs_invvv  19b NOT    0
N1587
----> C1952/a         R C3+R   1024 -1669   80  319 1 cs_invvv  19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT      R C3+R   1024 -1669   80  319 1 IOPAD    IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN      R C3+R   1024 -1669   80  319 1 IOPAD    IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1) R C3+R   1024 -1669   80  319 1 PI          0
num_dcd_cyl(1)
-----
3 local_milli_t2.reg_n.lat_0/a      F C3+R   2922 -1612   96  92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t2.reg_n.lat_0/c1 F C3-    160          60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y      F C3+R   2922 -1612   96  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a         R C3+R   2862 -1612  120  32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y      R C3+R   2862 -1612  120  32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a         F C3+R   2781 -1612  158  19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y       F C3+R   2781 -1612  158  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b         R C3+R   2671 -1612  3658 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y       R C3+R   2671 -1672  3658 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a         F C3+R   566 -1672   109  196 6 cs_nnd2n  02c NAND
2104 gbfonet_6
----> gbfozell_6/y     F C3+R   566 -1672   109  196 6 cs_invvn  09c NOT
0 gbfonet_6
----> gbfozell_6/a     R C3+R   490 -1672   206  43 1 cs_invvn  09c NOT
77 N2031
---->{e} C2162/y       R C3+R   490 -1672   206  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b         F C3+R   358 -1672   144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   358 -1672   144  216 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

-----
--
    4 local_milli_t1.reg_n.lat_0/a      F C3+R  2922 -1612   96   92 3 cl_invn  07c SRL
50 NET1056
Setup local_milli_t1.reg_n.lat_0/c1    F C3-    160         60  238 14 cl_invn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                      F C3+R  2922 -1612   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R  2862 -1612  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                      R C3+R  2862 -1612  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R  2781 -1612  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                      F C3+R  2781 -1612  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R  2671 -1612 3658 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                      R C3+R  2671 -1672 3658 1044 3 cs_nnd2n  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                          F C3+R  566 -1672  109  196 6 cs_nnd2n  02c NAND
2104 gbfonet_6
----> gbfonet_6/y                      F C3+R  566 -1672  109  196 6 cs_invn  09c NOT
0 gbfonet_6
----> gbfonet_6/a                      R C3+R  490 -1672  206   43 1 cs_invn  09c NOT
77 N2031
---->{e} C2162/y                      R C3+R  490 -1672  206   43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b                          F C3+R  358 -1672  144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R  358 -1672  144  216 5 cl_invn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C   60  222 13 cl_invn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
-----

--
    5 local_milli.reg_n.lat_0/a      F C3+R  2922 -1612   96   92 3 cl_invn  07c SRL
50 NET1056
Setup local_milli.reg_n.lat_0/c1    F C3-    160         60  238 14 cl_invn  07c 1200
slow_mode.c1_2
---->{a} BOX789/y                      F C3+R  2922 -1612   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R  2862 -1612  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                      R C3+R  2862 -1612  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R  2781 -1612  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                      F C3+R  2781 -1612  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R  2671 -1612 3658 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                      R C3+R  2671 -1672 3658 1044 3 cs_nnd2n  02c NAND

```

```

0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   566 -1672  109  196 6 cs_nnd2n  02c NAND
2104 gbfontet_6
----> gbfontet_6/y     F C3+R   566 -1672  109  196 6 cs_invvn  09c NOT
0 gbfontet_6
----> gbfontet_6/a     R C3+R   490 -1672  206  43 1 cs_invvn  09c NOT
77 N2031
---->{e} C2162/y      R C3+R   490 -1672  206  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b         F C3+R   358 -1672  144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R   358 -1672  144  216 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
> compare_critical_slack_limit
-1671.77 Avg: -133.92
comparing new slack -1671.7745 to saved slack -1841.3940
> reset_critical_slack_limit
-1671.77 Avg: -133.92
resetting the current slack to -1671.7745
> write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:08:19 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont  Slack due to a point downstream on path
Required Arrival Time   RAT        ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup      ClkGSet  ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold       ClkGHld  ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width  ClkTPW  ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                   Setup    ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                    Hold      ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle              EndOfC  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth         ClkPW   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

```


TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)

Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)

Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO	Cell	Delay/ Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	----	------	----------------------------------	-------

--									
1 iu_reset_op_c_t1	R C3+R	2671	-1672	3658	1011	1	PO		0
iu_reset_op_c_t1									
RAT	999						0		
----> BOX716/OUT	R C3+R	2671	-1672	3658	1011	1	IOPAD		IOPAD
0 iu_reset_op_c_t1									
----> BOX716/IN	R C3+R	2671	-1672	3658	1044	3	IOPAD		IOPAD
0 iu_reset_op_c_t1&0									
---->{a} C2393/y	R C3+R	2671	-1672	3658	1044	3	cs_nnd2n	02c	NAND
0 iu_reset_op_c_t1&0									
----> C2393/a	F C3+R	566	-1672	109	196	6	cs_nnd2n	02c	NAND
2104 gbfonet_6									
----> gbfonet_6/y	F C3+R	566	-1672	109	196	6	cs_invvn	09c	NOT
0 gbfonet_6									
----> gbfonet_6/a	R C3+R	490	-1672	206	43	1	cs_invvn	09c	NOT
77 N2031									
---->{b} C2162/y	R C3+R	490	-1672	206	43	1	cs_nnd3n	02c	NAND
0 N2031									
----> C2162/b	F C3+R	358	-1672	144	216	5	cs_nnd3n	02c	NAND
132 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R	358	-1672	144	216	5	cl_invvn	07d	
SRL 0 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_invvn	07d	SRL
198 slow_mode.c2_1									
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1		LCB
0 slow_mode.c2_1									

--									
2 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1	PO		0
dcd_succ_last_t1									
RAT	999						0		
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1	IOPAD		IOPAD
0 dcd_succ_last_t1									
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1	IOPAD		IOPAD
0 dcd_succ_last_t1&0									
----> C167/y	R C3+R	2668	-1669	3294	1011	1	cs_invvv	01c	NOT
0 dcd_succ_last_t1&0									
----> C167/a	F C3+R	1075	-1669	27	139	4	cs_invvv	01c	NOT
1594 N675									
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4	cs_nnd2x	14b	NAND
0 N675									
----> C2738/a	R C3+R	1056	-1669	33	114	1	cs_nnd2x	14b	NAND
19 last_cycle									
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1	cs_nnd2x	14e	NAND

0 last_cycle	
----> C2487/a	F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
21 N1587	
----> C1952/y	F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
N1587	
----> C1952/a	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1)	
----> BOX679/OUT	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1)	
----> BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1)	
----> num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 PI 0
num_dcd_cyl(1)	

3 local_milli_t2.reg_n.lat_0/a	F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
50 NET1056	
Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	
---->{a} BOX789/y	F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND
0 NET1056	
----> BOX789/a	R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND
60 NET1054	
---->{b} BOX785/y	R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND
0 NET1054	
----> BOX785/a	F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND
81 N1866	
---->{c} C2555/y	F C3+R 2781 -1612 158 19 1 cs_ao12n 03c AOI
0 N1866	
----> C2555/b	R C3+R 2671 -1612 3658 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0	
---->{d} C2393/y	R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	
----> C2393/a	F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND
2104 gbfonet_6	
----> gbfozell_6/y	F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6	
----> gbfozell_6/a	R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
77 N2031	
---->{e} C2162/y	R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND
0 N2031	
----> C2162/b	F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND
132 rcvry_reset_q	
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R 358 -1672 144 216 5 cl_invvn 07d
SRL 0 rcvry_reset_q	
----> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
----> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	

4 local_milli_t1.reg_n.lat_0/a	F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
50 NET1056	
Setup local_milli_t1.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	

---->{a} BOX789/y	F C3+R	2922	-1612	96	92	3	cs_nnd3z	07c	NAND
0 NET1056									
----> BOX789/a	R C3+R	2862	-1612	120	32	1	cs_nnd3z	07c	NAND
60 NET1054									
---->{b} BOX785/y	R C3+R	2862	-1612	120	32	1	cs_nnd2f	03c	NAND
0 NET1054									
----> BOX785/a	F C3+R	2781	-1612	158	19	1	cs_nnd2f	03c	NAND
81 N1866									
---->{c} C2555/y	F C3+R	2781	-1612	158	19	1	cs_ao12n	03c	AOI
0 N1866									
----> C2555/b	R C3+R	2671	-1612	3658	1044	3	cs_ao12n	03c	AOI
110 iu_reset_op_c_t1&0									
---->{d} C2393/y	R C3+R	2671	-1672	3658	1044	3	cs_nnd2n	02c	NAND
0 iu_reset_op_c_t1&0									
----> C2393/a	F C3+R	566	-1672	109	196	6	cs_nnd2n	02c	NAND
2104 gbfonet_6									
----> gbfcocell_6/y	F C3+R	566	-1672	109	196	6	cs_invn	09c	NOT
0 gbfonet_6									
----> gbfcocell_6/a	R C3+R	490	-1672	206	43	1	cs_invn	09c	NOT
77 N2031									
---->{e} C2162/y	R C3+R	490	-1672	206	43	1	cs_nnd3n	02c	NAND
0 N2031									
----> C2162/b	F C3+R	358	-1672	144	216	5	cs_nnd3n	02c	NAND
132 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/i2_out_n	F C3+R	358	-1672	144	216	5	cl_invn	07d	
SRL 0 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_invn	07d	SRL
198 slow_mode.c2_1									
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB	
0 slow_mode.c2_1									

5 local_milli.reg_n.lat_0/a	F C3+R	2922	-1612	96	92	3	cl_invn	07c	SRL
50 NET1056									
Setup local_milli.reg_n.lat_0/c1	F C3-	160		60	238	14	cl_invn	07c	1200
slow_mode.c1_2									
---->{a} BOX789/y	F C3+R	2922	-1612	96	92	3	cs_nnd3z	07c	NAND
0 NET1056									
----> BOX789/a	R C3+R	2862	-1612	120	32	1	cs_nnd3z	07c	NAND
60 NET1054									
---->{b} BOX785/y	R C3+R	2862	-1612	120	32	1	cs_nnd2f	03c	NAND
0 NET1054									
----> BOX785/a	F C3+R	2781	-1612	158	19	1	cs_nnd2f	03c	NAND
81 N1866									
---->{c} C2555/y	F C3+R	2781	-1612	158	19	1	cs_ao12n	03c	AOI
0 N1866									
----> C2555/b	R C3+R	2671	-1612	3658	1044	3	cs_ao12n	03c	AOI
110 iu_reset_op_c_t1&0									
---->{d} C2393/y	R C3+R	2671	-1672	3658	1044	3	cs_nnd2n	02c	NAND
0 iu_reset_op_c_t1&0									
----> C2393/a	F C3+R	566	-1672	109	196	6	cs_nnd2n	02c	NAND
2104 gbfonet_6									
----> gbfcocell_6/y	F C3+R	566	-1672	109	196	6	cs_invn	09c	NOT
0 gbfonet_6									
----> gbfcocell_6/a	R C3+R	490	-1672	206	43	1	cs_invn	09c	NOT

```

77 N2031
---->{e} C2162/y          R C3+R    490 -1672  206  43 1 cs_nnd3n  02c NAND
0 N2031
----> C2162/b            F C3+R    358 -1672  144  216 5 cs_nnd3n  02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n    F C3+R    358 -1672  144  216 5 cl_invvn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2          R C3+    160  N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160  N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

-----
--
      > repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}
initial slack is -1672
total pct of low vt boxes initially is 1.127
box count 621, pct of low vt boxes added is 20.13
total pct of low vt boxes used is 5.475
after repower paths slack is -1669

```

```

      > write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
           for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:08:20 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time    RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup       ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold        ClkGHld      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width    ClkTPW      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                    Setup        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                     Hold          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle               EndOfC      ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth          ClkPW       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
ClockSeparation          ClkSep      ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
Loop                     ALTest      ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
Arrival Time Limiting    ATLimit     Slack discontinuity due to failed test

```

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
<hr/>							
--							
1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT
1594 N675							
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND
0 N675							
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND
19 last_cycle							
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e NAND
0 last_cycle							
----> C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e NAND
21 N1587							
----> C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b NOT 0
N1587							
----> C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b NOT
11 num_dcd_cyl&0(1)							
----> BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD
0 num_dcd_cyl&0(1)							
----> BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD 0
num_dcd_cyl(1)							
----> num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI	0
num_dcd_cyl(1)							
<hr/>							
--							
2 iu_reset_op_c_t1	R C3+R	2420	-1421	3327	1011	1 PO	0
iu_reset_op_c_t1							
RAT	999					0	
----> BOX716/OUT	R C3+R	2420	-1421	3327	1011	1 IOPAD	IOPAD
0 iu_reset_op_c_t1							
----> BOX716/IN	R C3+R	2420	-1421	3327	1044	3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0							
---->{a} C2393/y	R C3+R	2420	-1421	3327	1044	3 cs_nnd2v	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	545	-1421	102	196	6 cs_nnd2v	02c NAND
1875 gbfont_6							
----> gbfont_6/y	F C3+R	545	-1421	102	196	6 cs_invvv	09c NOT
0 gbfont_6							
----> gbfont_6/a	R C3+R	480	-1421	196	44	1 cs_invvv	09c NOT
65 N2031							
---->{b} C2162/y	R C3+R	480	-1421	196	44	1 cs_nnd3v	02c NAND
0 N2031							
----> C2162/b	F C3+R	358	-1421	144	217	5 cs_nnd3v	02c NAND

```

122 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R   358 -1421  144  217 5 cl_invvn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+    160  N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+    160  N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
      3 local_milli_t2.reg_n.lat_0/a      F C3+R   2671 -1361   96   92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t2.reg_n.lat_0/c1      F C3-    160          60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                        F C3+R   2671 -1361   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R   2611 -1361  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                        R C3+R   2611 -1361  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R   2530 -1361  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                        F C3+R   2530 -1361  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R   2420 -1361  3327 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                        R C3+R   2420 -1421  3327 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                          F C3+R   545 -1421  102  196 6 cs_nnd2v  02c NAND
1875 gbfonet_6
----> gbfonet_6/y                      F C3+R   545 -1421  102  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfonet_6/a                      R C3+R   480 -1421  196   44 1 cs_invvv  09c NOT
65 N2031
---->{e} C2162/y                      R C3+R   480 -1421  196   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/b                          F C3+R   358 -1421  144  217 5 cs_nnd3v  02c NAND
122 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R   358 -1421  144  217 5 cl_invvn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+    160  N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+    160  N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
      4 local_milli_t1.reg_n.lat_0/a      F C3+R   2671 -1361   96   92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t1.reg_n.lat_0/c1      F C3-    160          60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                        F C3+R   2671 -1361   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R   2611 -1361  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                        R C3+R   2611 -1361  120   32 1 cs_nnd2f  03c NAND
0 NET1054

```

----> BOX785/a	F C3+R	2530	-1361	158	19	1	cs_nnd2f	03c	NAND
81 N1866									
---->{c} C2555/y	F C3+R	2530	-1361	158	19	1	cs_ao12n	03c	AOI
0 N1866									
----> C2555/b	R C3+R	2420	-1361	3327	1044	3	cs_ao12n	03c	AOI
110 iu_reset_op_c_t1&0									
---->{d} C2393/y	R C3+R	2420	-1421	3327	1044	3	cs_nnd2v	02c	NAND
0 iu_reset_op_c_t1&0									
----> C2393/a	F C3+R	545	-1421	102	196	6	cs_nnd2v	02c	NAND
1875 gbfont_6									
----> gbfont_6/y	F C3+R	545	-1421	102	196	6	cs_invvv	09c	NOT
0 gbfont_6									
----> gbfont_6/a	R C3+R	480	-1421	196	44	1	cs_invvv	09c	NOT
65 N2031									
---->{e} C2162/y	R C3+R	480	-1421	196	44	1	cs_nnd3v	02c	NAND
0 N2031									
----> C2162/b	F C3+R	358	-1421	144	217	5	cs_nnd3v	02c	NAND
122 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R	358	-1421	144	217	5	cl_invvn	07d	
SRL 0 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/c2	R C3+	160	N/C	60	222	13	cl_invvn	07d	SRL
198 slow_mode.c2_1									
----> slow_mode.clockblock/c2	R C3+	160	N/C	60	222	13	cb_clk_32_1	LCB	
0 slow_mode.c2_1									

5 local_milli.reg_n.lat_0/a	F C3+R	2671	-1361	96	92	3	cl_invvn	07c	SRL
50 NET1056									
Setup local_milli.reg_n.lat_0/c1	F C3-	160		60	238	14	cl_invvn	07c	1200
slow_mode.c1_2									
---->{a} BOX789/y	F C3+R	2671	-1361	96	92	3	cs_nnd3z	07c	NAND
0 NET1056									
----> BOX789/a	R C3+R	2611	-1361	120	32	1	cs_nnd3z	07c	NAND
60 NET1054									
---->{b} BOX785/y	R C3+R	2611	-1361	120	32	1	cs_nnd2f	03c	NAND
0 NET1054									
----> BOX785/a	F C3+R	2530	-1361	158	19	1	cs_nnd2f	03c	NAND
81 N1866									
---->{c} C2555/y	F C3+R	2530	-1361	158	19	1	cs_ao12n	03c	AOI
0 N1866									
----> C2555/b	R C3+R	2420	-1361	3327	1044	3	cs_ao12n	03c	AOI
110 iu_reset_op_c_t1&0									
---->{d} C2393/y	R C3+R	2420	-1421	3327	1044	3	cs_nnd2v	02c	NAND
0 iu_reset_op_c_t1&0									
----> C2393/a	F C3+R	545	-1421	102	196	6	cs_nnd2v	02c	NAND
1875 gbfont_6									
----> gbfont_6/y	F C3+R	545	-1421	102	196	6	cs_invvv	09c	NOT
0 gbfont_6									
----> gbfont_6/a	R C3+R	480	-1421	196	44	1	cs_invvv	09c	NOT
65 N2031									
---->{e} C2162/y	R C3+R	480	-1421	196	44	1	cs_nnd3v	02c	NAND
0 N2031									
----> C2162/b	F C3+R	358	-1421	144	217	5	cs_nnd3v	02c	NAND
122 rcvry_reset_q									
----> rcvry_reset.reg_n.lat_0/l2_out_n	F C3+R	358	-1421	144	217	5	cl_invvn	07d	

```

SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+   160   N/C   60  222 13 cl_inwn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+   160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
      > compare_critical_slack_limit
-1669.49 Avg: -124.51
comparing new slack -1669.4933 to saved slack -1655.0568
      > traceset {repower_paths HOWMANY}
[traceset]: trace string = repower_paths HOWMANY
[tracing]: set trace variable repower_paths to 20
      > reset_critical_slack_limit
-1669.49 Avg: -124.51
resetting the current slack to -1669.4933
      > quick tswap(SCORE(ALL),ACTUAL,ONE_LEVEL)

```

```

[
>>]: [quick]:( tswap(SCORE(ALL),ACTUAL,ONE_LEVEL) );

```

```

-1669.49 Avg: -124.51

```

```

setting SCORE option to ALL.

```

```

setting ACTUAL option.

```

```

setting ONE_LEVEL option.

```

```

maximum area for proto box IDCDSUC is 4664

```

```

[quick]: Number of boxes to process is 906.

```

```

[quick]: Number of boxes processed is 0.

```

```

-1669.49 Avg: -124.48

```

```

[BD-500304]: 35 pins swapped on 22 gates and 0 gates cloned.

```

```

[tswap]: Execution time was 5.7 seconds.

```

```

      > tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),R...

```

```

[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000

```

```

[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172

```

```

[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000

```

```

[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000

```

```

[tc_parm]: =====

```

```

[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000

```

```

      > critical repower(SCORE(ALL),REPOWER_GROUP(TAPERED),TAPER...

```

```

critical( repower(SCORE(ALL),REPOWER_GROUP(TAPERED),TAPERED_PIN_SWAP) );

```

```

-1669.49 Avg: -124.48

```

```

maximum area for proto box IDCDSUC is 4664

```

```

repower: setting SCORE option to ALL.

```

```

repower: setting TAPERED_PIN_SWAP option.

```

```

Number of paths is 5

```

```

Number of paths is 5

```

```

Number of paths is 5

```

```

Number of paths is 5

```

```

[BD-500026]: repower was applied 3 times.

```

```

Number of Tapered Cells = 14

```

```

[repower]: Execution time was 0.8 seconds.

```

```

[BD-502000]: Called transforms 30 times and applied 3 of them.

```

```

      > critical repower(SCORE(ALL),NO_VIOLATIONS)

```

```

critical( repower(SCORE(ALL),NO_VIOLATIONS) );

```

```

-1669.49 Avg: -125.12

```

```

maximum area for proto box IDCDSUC is 4671

```



```

repower: setting SCORE option to ALL.
repower: setting NO_VIOLATIONS option.
Number of paths is 5
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 27 times and applied 0 of them.
    > critical repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(...
critical( repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1669.49 Avg: -125.12
maximum area for proto box IDCDSUC is 4671
repower: setting SCORE option to ALL.
repower: setting NO_VIOLATIONS option.
Number of paths is 5
Number of paths is 5
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 1.0 seconds.
[BD-502000]: Called transforms 27 times and applied 1 of them.
    > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFF...
    > noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
repower: setting SCORE option to ALL.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1669.49 Avg: -125.32
maximum area for proto box IDCDSUC is 4675
-1669.49 Avg: -125.32
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1669.49 Avg: -125.31
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 7.7 seconds.
    > tc_parm MARGIN(10000000)
    > compare_critical_slack_limit
-1669.49 Avg: -125.31
comparing new slack -1669.4933 to saved slack -1652.7983
    > reset_critical_slack_limit
-1669.49 Avg: -125.31
resetting the current slack to -1669.4933
    > write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
           for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:08:37 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

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Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time    RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)

```

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	------------------	-----------------------

--	1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO	0
	dcd_succ_last_t1							
	RAT	999					0	
----	BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0	dcd_succ_last_t1							
----	BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0	dcd_succ_last_t1&0							
----	C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT
0	dcd_succ_last_t1&0							
----	C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT
1594	N675							
----	{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND
0	N675							
----	C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND
19	last_cycle							
----	{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e NAND
0	last_cycle							
----	C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e NAND
21	N1587							
----	C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b NOT
N1587								0
----	C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b NOT
11	num_dcd_cyl&0(1)							
----	BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD
0	num_dcd_cyl&0(1)							
----	BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD
num_dcd_cyl(1)								0
----	num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI	0
num_dcd_cyl(1)								

```

--
2 iu_reset_op_c_t1          R C3+R  2399 -1400  3318 1011 1 PO          0
iu_reset_op_c_t1
RAT          999          0
----> BOX716/OUT          R C3+R  2399 -1400  3318 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN          R C3+R  2399 -1400  3318 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R  2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R  536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfozell_6/y          F C3+R  536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfozell_6/a          R C3+R  472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y          R C3+R  472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a          F C3+R  358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n          F C3+R  358 -1400   144  217 5 cl_invvv  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2          R C3+   160   N/C    60  222 13 cl_invvv  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+   160   N/C    60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

-----
3 dcd_succ_last_t1          F C3+R  2354 -1355  1874 1011 1 PO          0
dcd_succ_last_t1
RAT          999          0
----> BOX714/OUT          F C3+R  2354 -1355  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          F C3+R  2354 -1355  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y          F C3+R  2354 -1355  1874 1011 1 cs_invvv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          R C3+R  1146 -1355    69  139 4 cs_invvv  01c NOT
1208 N675
---->{a} C2738/y          R C3+R  1146 -1355    69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b          F C3+R  1097 -1355    64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y          F C3+R  1097 -1355    64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a          R C3+R  1051 -1355   116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y          R C3+R  1051 -1355   116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b          F C3+R  983 -1355    36  113 2 cs_nnd3i  11b NAND
68 N892
---->{d} C2338/y          F C3+R  983 -1355    36  113 2 cs_nnd2x  14c NAND
0 N892
----> C2338/a          R C3+R  959 -1355    71  159 3 cs_nnd2x  14c NAND
24 N1119

```

----> C2905/y N1119	R C3+R	959	-1355	71	159	3	cs_invvv	12b	NOT	0
----> C2905/a N2010	F C3+R	915	-1355	59	76	1	cs_invvv	12b	NOT	45
---->{e} C2906/y 0 N2010	F C3+R	915	-1355	59	76	1	cs_nor2g	12e	NOR	
----> C2906/b 47 dcd_blk_dsucc&0	R C3+R	868	-1355	80	124	1	cs_nor2g	12e	NOR	
----> BOX644/OUT 0 dcd_blk_dsucc&0	R C3+R	868	-1355	80	124	1	IOPAD		IOPAD	
----> BOX644/IN dcd_blk_dsucc	R C3+R	868	-1355	80	124	1	IOPAD		IOPAD	0
----> dcd_blk_dsucc dcd_blk_dsucc	R C3+R	868	-1355	80	124	1	PI			0

4 local_milli_t2.reg_n.lat_0/a 50 NET1056	F C3+R	2650	-1340	96	92	3	cl_invvn	07c	SRL	
Setup local_milli_t2.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3-	160		60	238	14	cl_invvn	07c		
---->{a} BOX789/y 0 NET1056	F C3+R	2650	-1340	96	92	3	cs_nnd3z	07c	NAND	
----> BOX789/a 60 NET1054	R C3+R	2590	-1340	120	32	1	cs_nnd3z	07c	NAND	
---->{b} BOX785/y 0 NET1054	R C3+R	2590	-1340	120	32	1	cs_nnd2f	03c	NAND	
----> BOX785/a 81 N1866	F C3+R	2510	-1340	158	19	1	cs_nnd2f	03c	NAND	
---->{c} C2555/y 0 N1866	F C3+R	2510	-1340	158	19	1	cs_ao12n	03c	AOI	
----> C2555/b 110 iu_reset_op_c_t1&0	R C3+R	2399	-1340	3318	1044	3	cs_ao12n	03c	AOI	
---->{d} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2399	-1400	3318	1044	3	cs_nnd2v	02c	NAND	
----> C2393/a 1863 gbfonet_6	F C3+R	536	-1400	100	196	6	cs_nnd2v	02c	NAND	
----> gbfozell_6/y 0 gbfonet_6	F C3+R	536	-1400	100	196	6	cs_invvv	09c	NOT	
----> gbfozell_6/a 64 N2031	R C3+R	472	-1400	184	44	1	cs_invvv	09c	NOT	
---->{e} C2162/y 0 N2031	R C3+R	472	-1400	184	44	1	cs_nnd3v	02c	NAND	
----> C2162/a 114 rcvry_reset_q	F C3+R	358	-1400	144	217	5	cs_nnd3v	02c	NAND	
----> rcvry_reset.reg_n.lat_0/l2_out_n SRL 0 rcvry_reset_q	F C3+R	358	-1400	144	217	5	cl_invvn	07d		
----> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1	R C3+	160	N/C	60	222	13	cl_invvn	07d	SRL	
----> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+	160	N/C	60	222	13	cb_clk_32_1		LCB	

5 local_milli_t1.reg_n.lat_0/a 50 NET1056	F C3+R	2650	-1340	96	92	3	cl_invvn	07c	SRL	
Setup local_milli_t1.reg_n.lat_0/c1	F C3-	160		60	238	14	cl_invvn	07c		

```

1200 slow_mode.c1_4
---->{a} BOX789/y          F C3+R  2650 -1340   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a            R C3+R  2590 -1340  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y          R C3+R  2590 -1340  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a            F C3+R  2510 -1340  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y           F C3+R  2510 -1340  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b             R C3+R  2399 -1340  3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0    R C3+R  2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
---->{d} C2393/y          R C3+R  2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0      F C3+R  536 -1400   100  196 6 cs_nnd2v  02c NAND
----> C2393/a            F C3+R  536 -1400   100  196 6 cs_invvv  09c NOT
1863 gbfonet_6            F C3+R  536 -1400   100  196 6 cs_invvv  09c NOT
----> gbfozell_6/y        R C3+R  472 -1400   184   44 1 cs_invvv  09c NOT
0 gbfonet_6
----> gbfozell_6/a        R C3+R  472 -1400   184   44 1 cs_nnd3v  02c NAND
64 N2031
---->{e} C2162/y          R C3+R  472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a            F C3+R  358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q         F C3+R  358 -1400   144  217 5 cl_invvn  07d
----> rcvry_reset.reg_n.lat_0/2_out_n  F C3+R  358 -1400   144  217 5 cl_invvn  07d
SRL 0 rcvry_reset_q       R C3+  160  N/C    60  222 13 cl_invvn  07d SRL
----> rcvry_reset.reg_n.lat_0/c2       R C3+  160  N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1        R C3+  160  N/C    60  222 13 cb_clk_32_1 LCB
----> slow_mode.clockblock/c2          R C3+  160  N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

--

> repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}

initial slack is -1669

total pct of low vt boxes initially is 5.475

box count 621, pct of low vt boxes added is 19.65

total pct of low vt boxes used is 5.475

after repower paths slack is -1669

> write_end_point_report -points 5

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:08:37 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation

SlkCont

Slack due to a point downstream on path

Required Arrival Time

RAT

(ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT

(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL


```

--
2 iu_reset_op_c_t1          R C3+R   2399 -1400  3318 1011 1 PO          0
iu_reset_op_c_t1
RAT                          999          0
----> BOX716/OUT            R C3+R   2399 -1400  3318 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN            R C3+R   2399 -1400  3318 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R   2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a              F C3+R   536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfont_6
----> gbfont_6/y          F C3+R   536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfont_6
----> gbfont_6/a          R C3+R   472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y          R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a              F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   358 -1400   144  217 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+   160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+   160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
3 dcd_succ_last_t1          F C3+R   2354 -1355  1874 1011 1 PO          0
dcd_succ_last_t1
RAT                          999          0
----> BOX714/OUT            F C3+R   2354 -1355  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            F C3+R   2354 -1355  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y              F C3+R   2354 -1355  1874 1011 1 cs_invvv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a              R C3+R   1146 -1355    69  139 4 cs_invvv  01c NOT
1208 N675
---->{a} C2738/y          R C3+R   1146 -1355    69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b              F C3+R   1097 -1355    64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y        F C3+R   1097 -1355    64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a          R C3+R   1051 -1355   116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y        R C3+R   1051 -1355   116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b          F C3+R   983 -1355    36  113 2 cs_nnd3i  11b NAND
68 N892
---->{d} C2338/y          F C3+R   983 -1355    36  113 2 cs_nnd2x  14c NAND
0 N892
----> C2338/a              R C3+R   959 -1355    71  159 3 cs_nnd2x  14c NAND

```



```

Setup local_milli_t1.reg_n.lat_0/c1      F C3-    160      60 238 14 cl_invn 07c
1200 slow_mode.c1_4
---->{a} BOX789/y      F C3+R    2650 -1340 96 92 3 cs_nnd3z 07c NAND
0 NET1056
----> BOX789/a      R C3+R    2590 -1340 120 32 1 cs_nnd3z 07c NAND
60 NET1054
---->{b} BOX785/y      R C3+R    2590 -1340 120 32 1 cs_nnd2f 03c NAND
0 NET1054
----> BOX785/a      F C3+R    2510 -1340 158 19 1 cs_nnd2f 03c NAND
81 N1866
---->{c} C2555/y      F C3+R    2510 -1340 158 19 1 cs_ao12n 03c AOI
0 N1866
----> C2555/b      R C3+R    2399 -1340 3318 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y      R C3+R    2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a      F C3+R    536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6
----> gbfonet_6/y      F C3+R    536 -1400 100 196 6 cs_invv 09c NOT
0 gbfonet_6
----> gbfonet_6/a      R C3+R    472 -1400 184 44 1 cs_invv 09c NOT
64 N2031
---->{e} C2162/y      R C3+R    472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031
----> C2162/a      F C3+R    358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R    358 -1400 144 217 5 cl_invn 07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C   60 222 13 cl_invn 07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+    160   N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

-----
> compare_critical_slack_limit
-1669.49 Avg: -125.31
comparing new slack -1669.4933 to saved slack -1652.7983
> traceset {repower_paths HOWMANY}
[traceset]: trace string = repower_paths HOWMANY
[tracing]: set trace variable repower_paths to 20
> write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:08:37 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation

SlkCont

Slack due to a point downstream on path

Required Arrival Time

RAT

(ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
 Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
 Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
 Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
 Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
 Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T Adj
1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO		0
dcd_succ_last_t1								
RAT		999				0		
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD		IOPAD
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c	NOT
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c	NOT
1594 N675								
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b	NAND
0 N675								
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b	NAND
19 last_cycle								
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e	NAND
0 last_cycle								
----> C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e	NAND
21 N1587								
----> C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b	NOT
N1587								0
----> C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b	NOT
11 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD		IOPAD
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD		IOPAD
num_dcd_cyl(1)								0
----> num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI		0

num_dcd_cyl(1)

```
--
2 iu_reset_op_c_t1          R C3+R  2399 -1400  3318 1011 1 PO          0
iu_reset_op_c_t1
RAT          999          0
----> BOX716/OUT          R C3+R  2399 -1400  3318 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN          R C3+R  2399 -1400  3318 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R  2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R  536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfonet_6/y          F C3+R  536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfonet_6/a          R C3+R  472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y          R C3+R  472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a          F C3+R  358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R  358 -1400   144  217 5 cl_invvn  07d
SRL  0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2          R C3+  160  N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+  160  N/C    60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
```

```
--
3 dcd_succ_last_t1          F C3+R  2354 -1355  1874 1011 1 PO          0
dcd_succ_last_t1
RAT          999          0
----> BOX714/OUT          F C3+R  2354 -1355  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          F C3+R  2354 -1355  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y          F C3+R  2354 -1355  1874 1011 1 cs_invvv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a          R C3+R  1146 -1355    69  139 4 cs_invvv  01c NOT
1208 N675
---->{a} C2738/y          R C3+R  1146 -1355    69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b          F C3+R  1097 -1355    64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y          F C3+R  1097 -1355    64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a          R C3+R  1051 -1355   116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y          R C3+R  1051 -1355   116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b          F C3+R  983 -1355    36  113 2 cs_nnd3i  11b NAND
68 N892
---->{d} C2338/y          F C3+R  983 -1355    36  113 2 cs_nnd2x  14c NAND
0 N892
```

----> C2338/a	R C3+R	959	-1355	71	159	3	cs_nnd2x	14c	NAND	
24 N1119										
----> C2905/y	R C3+R	959	-1355	71	159	3	cs_invvv	12b	NOT	0
N1119										
----> C2905/a	F C3+R	915	-1355	59	76	1	cs_invvv	12b	NOT	45
N2010										
---->{e} C2906/y	F C3+R	915	-1355	59	76	1	cs_nor2g	12e	NOR	
0 N2010										
----> C2906/b	R C3+R	868	-1355	80	124	1	cs_nor2g	12e	NOR	
47 dcd_blk_dsucc&0										
----> BOX644/OUT	R C3+R	868	-1355	80	124	1	IOPAD		IOPAD	
0 dcd_blk_dsucc&0										
----> BOX644/IN	R C3+R	868	-1355	80	124	1	IOPAD		IOPAD	0
dcd_blk_dsucc										
----> dcd_blk_dsucc	R C3+R	868	-1355	80	124	1	PI			0
dcd_blk_dsucc										

```

> critical clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIO...
critical( clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS) );

```

```
-1669.49 Avg: -125.31
```

```
maximum area for proto box IDCDSUC is 4675
```

```
setting SCORE option to ALL.
```

```
setting ACTUAL option.
```

```
setting RE_POWER option.
```

```
setting FASTEST mode.
```

```
setting NO_VIOLATIONS option.
```

```
-1669.49 Avg: -125.31
```

```
ArrayNum: 6 ArrayMax: 906
```

```
[BD-500100]: 0 parallel copies of gates were made.
```

```
[clone]: Execution time was 0.1 seconds.
```

```
[BD-502000]: Called transforms 6 times and applied 0 of them.
```

```
> reset_critical_slack_limit
```

```
-1669.49 Avg: -125.31
```

```
resetting the current slack to -1669.4933
```

```
> critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
```

```
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
```

```
-1669.49 Avg: -125.31
```

```
maximum area for proto box IDCDSUC is 4675
```

```
setting SCORE option to ALL.
```

```
setting ESTIMATED option.
```

```
setting TWO_LEVEL option.
```

```
setting NO_VIOLATIONS option.
```

```
-1669.49 Avg: -125.31
```

```
ArrayNum: 6 ArrayMax: 906
```

```
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
```

```
[tswap]: Execution time was 0.0 seconds.
```

```
[BD-502000]: Called transforms 6 times and applied 0 of them.
```

```
> tc_parm REGALL
```

```
> repower_paths {FUZZY(0.02), SIMULTANEOUS_REPOWER}
```

```
initial slack is -1669
```

```
after repower paths slack is -1669
```

```
> repower_paths FUZZY(0.02)
```

```
initial slack is -1669
```

```
after repower paths slack is -1669
```

```

> critical {repower(SCORE(ALL ),INC ,NO_VIOLATIONS), re...
critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
-1669.49 Avg: -125.34
maximum area for proto box IDCDSUC is 4676
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1669.49 Avg: -125.34
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.

```

```

> compare_critical_slack_limit
-1669.49 Avg: -125.34
comparing new slack -1669.4933 to saved slack -1652.7983

```

```

> reset_critical_slack_limit
-1669.49 Avg: -125.34
resetting the current slack to -1669.4933
> write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:09:29 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 5

Cause of Slack Abbreviation Comparison/Description

Cause of Slack	Abbreviation	Comparison/Description
Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)

ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	-------------------------------------

1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT
1594 N675							
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND
0 N675							
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND
19 last_cycle							
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e NAND
0 last_cycle							
----> C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e NAND
21 N1587							
----> C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b NOT
N1587							0
----> C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b NOT
11 num_dcd_cyl&0(1)							
----> BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD
0 num_dcd_cyl&0(1)							
----> BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD
num_dcd_cyl(1)							0
----> num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI	0
num_dcd_cyl(1)							

2 iu_reset_op_c_t1	R C3+R	2399	-1400	3318	1011	1 PO	0
iu_reset_op_c_t1							
RAT	999					0	
----> BOX716/OUT	R C3+R	2399	-1400	3318	1011	1 IOPAD	IOPAD
0 iu_reset_op_c_t1							
----> BOX716/IN	R C3+R	2399	-1400	3318	1044	3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0							
---->{a} C2393/y	R C3+R	2399	-1400	3318	1044	3 cs_nnd2v	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	536	-1400	100	196	6 cs_nnd2v	02c NAND
1863 gbfonet_6							
----> gbfonet_6/y	F C3+R	536	-1400	100	196	6 cs_invvv	09c NOT
0 gbfonet_6							

```

----> gbfozell_6/a          R C3+R   472 -1400   184   44 1 cs_invvw  09c NOT
64 N2031
---->{b} C2162/y          R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a             F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n    F C3+R   358 -1400   144  217 5 cl_invvw  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2          R C3+    160   N/C    60  222 13 cl_invvw  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2           R C3+    160   N/C    60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
3 dcd_succ_last_t1          F C3+R  2352 -1353  1874 1011 1 PO              0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT          F C3+R  2352 -1353  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          F C3+R  2352 -1353  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y             F C3+R  2352 -1353  1874 1011 1 cs_invvw  01c NOT
0 dcd_succ_last_t1&0
----> C167/a             R C3+R   1144 -1353    69  139 4 cs_invvw  01c NOT
1208 N675
---->{a} C2738/y         R C3+R   1144 -1353    69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b           F C3+R   1095 -1353    64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y     F C3+R   1095 -1353    64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a       R C3+R   1049 -1353   116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y     R C3+R   1049 -1353   116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b       F C3+R    981 -1353    34  113 2 cs_nnd3i  11b NAND
67 N892
---->{d} C2338/y        F C3+R    981 -1353    34  113 2 cs_nnd2x  14c NAND
0 N892
----> C2338/a           R C3+R    958 -1353    62  159 3 cs_nnd2x  14c NAND
23 N1119
----> C2905/y           R C3+R    958 -1353    62  159 3 cs_invvw  13b NOT      0
N1119
----> C2905/a           F C3+R    918 -1353    63   92 1 cs_invvw  13b NOT      41
N2010
---->{e} C2906/y        F C3+R    918 -1353    63   92 1 cs_nor2g  12e NOR
0 N2010
----> C2906/b           R C3+R    868 -1353    80  124 1 cs_nor2g  12e NOR
50 dcd_blk_dsucc&0
----> BOX644/OUT        R C3+R    868 -1353    80  124 1 IOPAD      IOPAD
0 dcd_blk_dsucc&0
----> BOX644/IN        R C3+R    868 -1353    80  124 1 IOPAD      IOPAD      0
dcd_blk_dsucc
----> dcd_blk_dsucc     R C3+R    868 -1353    80  124 1 PI              0
dcd_blk_dsucc

```

```

-----
--
    4 local_milli_t2.reg_n.lat_0/a      F C3+R  2650 -1340  96  92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t2.reg_n.lat_0/c1    F C3-    160      60 238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                      F C3+R  2650 -1340  96  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R  2590 -1340  120  32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                      R C3+R  2590 -1340  120  32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R  2510 -1340  158  19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                      F C3+R  2510 -1340  158  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R  2399 -1340  3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                      R C3+R  2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                          F C3+R  536 -1400  100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfcoll_6/y                      F C3+R  536 -1400  100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfcoll_6/a                      R C3+R  472 -1400  184  44 1 cs_invvv  09c NOT
64 N2031
---->{e} C2162/y                      R C3+R  472 -1400  184  44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a                          F C3+R  358 -1400  144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R  358 -1400  144  217 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C   60 222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
-----

```

```

--
    5 local_milli_t1.reg_n.lat_0/a      F C3+R  2650 -1340  96  92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t1.reg_n.lat_0/c1    F C3-    160      60 238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                      F C3+R  2650 -1340  96  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R  2590 -1340  120  32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                      R C3+R  2590 -1340  120  32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R  2510 -1340  158  19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                      F C3+R  2510 -1340  158  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R  2399 -1340  3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                      R C3+R  2399 -1400  3318 1044 3 cs_nnd2v  02c NAND

```



```

0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R    536 -1400   100   196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfonet_6/y      F C3+R    536 -1400   100   196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfonet_6/a      R C3+R    472 -1400   184    44 1 cs_invvv  09c NOT
64 N2031
----> {e} C2162/y      R C3+R    472 -1400   184    44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a          F C3+R    358 -1400   144   217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R    358 -1400   144   217 5 cl_invvn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2        R C3+    160   N/C    60   222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160   N/C    60   222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

-----
> repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}

```

initial slack is -1669

total pct of low vt boxes initially is 5.475

box count 621, pct of low vt boxes added is 19.65

total pct of low vt boxes used is 5.636

after repower paths slack is -1669

```

> write_end_point_report -points 5

```

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:30 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time    RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup       ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold        ClkGHld     ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width   ClkTPW      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                    Setup        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                      Hold          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle               EndOfC      ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth          ClkPW       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

```

TRAILING EDGE)

ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST)

Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST)

Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	----------------------------------	-------

--								
1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO		0
dcd_succ_last_t1								
RAT	999					0		
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT	
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT	
1594 N675								
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND	
0 N675								
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND	
19 last_cycle								
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e NAND	
0 last_cycle								
----> C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e NAND	
21 N1587								
----> C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b NOT	0
N1587								
----> C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b NOT	
11 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD	
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD	0
num_dcd_cyl(1)								
----> num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI		0
num_dcd_cyl(1)								

--								
2 iu_reset_op_c_t1	R C3+R	2399	-1400	3318	1011	1 PO		0
iu_reset_op_c_t1								
RAT	999					0		
----> BOX716/OUT	R C3+R	2399	-1400	3318	1011	1 IOPAD	IOPAD	
0 iu_reset_op_c_t1								
----> BOX716/IN	R C3+R	2399	-1400	3318	1044	3 IOPAD	IOPAD	
0 iu_reset_op_c_t1&0								
---->{a} C2393/y	R C3+R	2399	-1400	3318	1044	3 cs_nnd2v	02c NAND	
0 iu_reset_op_c_t1&0								
----> C2393/a	F C3+R	536	-1400	100	196	6 cs_nnd2v	02c NAND	
1863 gbfont_6								
----> gbfont_6/y	F C3+R	536	-1400	100	196	6 cs_invvv	09c NOT	

```

0 gbfonet_6
----> gbfozell_6/a          R C3+R   472 -1400  184  44 1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y          R C3+R   472 -1400  184  44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a             F C3+R   358 -1400  144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R   358 -1400  144  217 5 cl_invvn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2            R C3+    160  N/C   60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+    160  N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
3 dcd_succ_last_t1          F C3+R  2352 -1353  1874  1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT          F C3+R  2352 -1353  1874  1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN          F C3+R  2352 -1353  1874  1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y             F C3+R  2352 -1353  1874  1011 1 cs_invvv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a             R C3+R   1144 -1353   69  139 4 cs_invvv  01c NOT
1208 N675
---->{a} C2738/y         R C3+R   1144 -1353   69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b           F C3+R   1095 -1353   64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y      F C3+R   1095 -1353   64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a        R C3+R   1049 -1353  116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y      R C3+R   1049 -1353  116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b        F C3+R   981 -1353   34  113 2 cs_nnd3i  11b NAND
67 N892
---->{d} C2338/y        F C3+R   981 -1353   34  113 2 cs_nnd2x  14c NAND
0 N892
----> C2338/a          R C3+R   958 -1353   62  159 3 cs_nnd2x  14c NAND
23 N1119
----> C2905/y          R C3+R   958 -1353   62  159 3 cs_invvv  13b NOT      0
N1119
----> C2905/a          F C3+R   918 -1353   63   92 1 cs_invvv  13b NOT      41
N2010
---->{e} C2906/y        F C3+R   918 -1353   63   92 1 cs_nor2g  12e NOR
0 N2010
----> C2906/b          R C3+R   868 -1353   80  124 1 cs_nor2g  12e NOR
50 dcd_blk_dsucc&0
----> BOX644/OUT        R C3+R   868 -1353   80  124 1 IOPAD      IOPAD
0 dcd_blk_dsucc&0
----> BOX644/IN        R C3+R   868 -1353   80  124 1 IOPAD      IOPAD      0
dcd_blk_dsucc
----> dcd_blk_dsucc     R C3+R   868 -1353   80  124 1 PI          0

```

dcd_blk_dsucc

```
--
4 local_milli_t2.reg_n.lat_0/a      F C3+R  2650 -1340  96  92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t2.reg_n.lat_0/c1  F C3-    160      60 238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                    F C3+R  2650 -1340  96  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                       R C3+R  2590 -1340 120  32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                    R C3+R  2590 -1340 120  32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                       F C3+R  2510 -1340 158  19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                    F C3+R  2510 -1340 158  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                        R C3+R  2399 -1340 3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                    R C3+R  2399 -1400 3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                        F C3+R   536 -1400 100 196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfcoll_6/y                   F C3+R   536 -1400 100 196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfcoll_6/a                   R C3+R   472 -1400 184  44 1 cs_invvv  09c NOT
64 N2031
---->{e} C2162/y                    R C3+R   472 -1400 184  44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a                       F C3+R   358 -1400 144 217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   358 -1400 144 217 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2     R C3+    160   N/C  60 222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2       R C3+    160   N/C  60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
-----
```

```
--
5 local_milli_t1.reg_n.lat_0/a      F C3+R  2650 -1340  96  92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t1.reg_n.lat_0/c1  F C3-    160      60 238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                    F C3+R  2650 -1340  96  92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                       R C3+R  2590 -1340 120  32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                    R C3+R  2590 -1340 120  32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                       F C3+R  2510 -1340 158  19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                    F C3+R  2510 -1340 158  19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                        R C3+R  2399 -1340 3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
```

```

---->{d} C2393/y          R C3+R   2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a             F C3+R   536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfonet_6/y         F C3+R   536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfonet_6/a         R C3+R   472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
---->{e} C2162/y          R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a             F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   358 -1400   144  217 5 cl_invvn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2       R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2         R C3+    160   N/C    60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1

```

```

--
      > compare_critical_slack_limit
-1669.49 Avg: -125.33
comparing new slack -1669.4933 to saved slack -1652.7983
      > traceset {repower_paths HOWMANY}
[traceset]: trace string = repower_paths HOWMANY
[tracing]: set trace variable repower_paths to 20
      > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
           for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:09:30 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont  Slack due to a point downstream on path
Required Arrival Time    RAT      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup       ClkGSet  ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold        ClkGHld  ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width   ClkTPW   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                    Setup    ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                      Hold     ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle               EndOfC  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )

```

ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	-------------------------------------

```

--
1 dcd_succ_last_t1          R C3+R   2668 -1669  3294 1011 1 PO          0
dcd_succ_last_t1
RAT                          999                      0
----> BOX714/OUT            R C3+R   2668 -1669  3294 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            R C3+R   2668 -1669  3294 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y               R C3+R   2668 -1669  3294 1011 1 cs_invvv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a               F C3+R   1075 -1669   27  139 4 cs_invvv  01c NOT
1594 N675
---->{a} C2738/y           F C3+R   1075 -1669   27  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/a              R C3+R   1056 -1669   33  114 1 cs_nnd2x  14b NAND
19 last_cycle
---->{b} C2487/y           R C3+R   1056 -1669   33  114 1 cs_nnd2x  14e NAND
0 last_cycle
----> C2487/a              F C3+R   1035 -1669   22  145 3 cs_nnd2x  14e NAND
21 N1587
----> C1952/y              F C3+R   1035 -1669   22  145 3 cs_invvv  19b NOT      0
N1587
----> C1952/a              R C3+R   1024 -1669   80  319 1 cs_invvv  19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT            R C3+R   1024 -1669   80  319 1 IOPAD      IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN            R C3+R   1024 -1669   80  319 1 IOPAD      IOPAD      0
num_dcd_cyl(1)
----> num_dcd_cyl(1)       R C3+R   1024 -1669   80  319 1 PI          0
num_dcd_cyl(1)

```

```

--
2 iu_reset_op_c_t1          R C3+R   2399 -1400  3318 1011 1 PO          0
iu_reset_op_c_t1
RAT                          999                      0
----> BOX716/OUT            R C3+R   2399 -1400  3318 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN            R C3+R   2399 -1400  3318 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y           R C3+R   2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a              F C3+R    536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfont_6

```

```

----> gbfcocell_6/y          F C3+R   536 -1400   100  196 6 cs_invvw  09c NOT
0 gbfcocell_6
----> gbfcocell_6/a          R C3+R   472 -1400   184   44 1 cs_invvw  09c NOT
64 N2031
---->{b} C2162/y            R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a                F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R   358 -1400   144  217 5 cl_invvw  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvw  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+    160   N/C    60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
3 dcd_succ_last_t1          F C3+R  2352 -1353  1874 1011 1 PO              0
dcd_succ_last_t1
RAT                          999              0
----> BOX714/OUT             F C3+R  2352 -1353  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN              F C3+R  2352 -1353  1874 1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y                 F C3+R  2352 -1353  1874 1011 1 cs_invvw  01c NOT
0 dcd_succ_last_t1&0
----> C167/a                 R C3+R   1144 -1353    69  139 4 cs_invvw  01c NOT
1208 N675
---->{a} C2738/y             R C3+R   1144 -1353    69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b                F C3+R   1095 -1353    64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y          F C3+R   1095 -1353    64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a             R C3+R   1049 -1353   116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y          R C3+R   1049 -1353   116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b             F C3+R    981 -1353    34  113 2 cs_nnd3i  11b NAND
67 N892
---->{d} C2338/y             F C3+R    981 -1353    34  113 2 cs_nnd2x  14c NAND
0 N892
----> C2338/a                R C3+R    958 -1353    62  159 3 cs_nnd2x  14c NAND
23 N1119
----> C2905/y                R C3+R    958 -1353    62  159 3 cs_invvw  13b NOT    0
N1119
----> C2905/a                F C3+R    918 -1353    63   92 1 cs_invvw  13b NOT    41
N2010
---->{e} C2906/y             F C3+R    918 -1353    63   92 1 cs_nor2g  12e NOR
0 N2010
----> C2906/b                R C3+R    868 -1353    80  124 1 cs_nor2g  12e NOR
50 dcd_blk_dsucc&0
----> BOX644/OUT             R C3+R    868 -1353    80  124 1 IOPAD      IOPAD
0 dcd_blk_dsucc&0
----> BOX644/IN              R C3+R    868 -1353    80  124 1 IOPAD      IOPAD    0
dcd_blk_dsucc

```

```

----> dcd_blk_dsucc          R C3+R   868  -1353   80  124 1 PI          0
dcd_blk_dsucc
-----

```

```

--
> chkbuff
[BD-500000]: chkbuff CMVC version 1.11 compiled on Apr 13 1999 at 18:21:07
[BD-501000]: Removed 0 buffers and merged 0 AND gates.
[chkbuff]: Execution time was 0.0 seconds.
> dualcnt REG
[dualcnt]: 0 REG boxes are followed by inverters
> dualcnt IOPAD
[dualcnt]: 32 or 7 IOPAD boxes are followed by inverters
> dual_rail_to_single_rail
[dual_rail_to_single_rail]: CMVC version 1.8 compiled on Apr 13 1999 at 18:01:34.
[dual_rail_to_single_rail]: created 0 single rail boxes
> nextbox chklegal
[
>>]: nextbox( chklegal );
[BD-41212]: (E) Gate 'slow_mode.clockblock' is bound to cell 'cb_clk_32_1' which is not a proper parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_1' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_2' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_3' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_4' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_5' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41200]: No illegal DOT gates found.
[BD-41202]: No illegal pin drops found.
> nextnet chklegal
[
>>]: nextnet( chklegal );
[BD-41206]: No illegal pin drops found.
[BD-41204]: No illegally dotted nets found.
> checksrc
[BD-40132]: Network IDCDSUC has no potential problems.
> nextbox dbuff()
[
>>]: nextbox( dbuff() );
[BD-500000]: dbuff CMVC version 1.6 compiled on Apr 13 1999 at 18:22:00
> reset_timing
> checkfan

```

Electrical Violations in Network 'IDCDSUC'

Fanout		Capacitance	Slew	Sink
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual	
Limit / AdjLim / Actual				
eu_iu_enter_slow_md	-> eu_iu_enter_slow_md	141.00 / 141.00 / 16.73	290.00	
12 / 290.00 / 352.00 *	12 / 12 / 1 1			
op_inq_stores	-> op_inq_stores	141.00 / 141.00 / 159.72 *	290.00 /	
290.00 / 112.00	12 / 12 / 3 1			

eu_iu_mmode	-> eu_iu_mmode	141.00 / 141.00 / 32.56	290.00 /
290.00 / 326.00 *	12 / 12 / 2 1		
du_iu_hold_aa_req	-> du_iu_hold_aa_req	141.00 / 141.00 / 141.99 *	290.00
/ 290.00 / 424.00 *	12 / 12 / 2 1		
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	141.00 / 141.00 / 30.80	290.00 /
290.00 / 339.00 *	12 / 12 / 1 1		
eu_iu_misc_hold	-> eu_iu_misc_hold	141.00 / 141.00 / 19.15	290.00 /
290.00 / 332.00 *	12 / 12 / 1 1		
op_mcend_raw	-> op_mcend_raw	141.00 / 141.00 / 144.35 *	290.00 /
290.00 / 91.00	12 / 12 / 3 1		
clkg	-> clkg	141.00 / 141.00 / 145.52 *	100.00 / 100.00 /
60.00	12 / 12 / 3 1		
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 20.50	290.00 /
290.00 / 338.00 *	12 / 12 / 1 1		
iq_empty	-> iq_empty	141.00 / 141.00 / 170.11 *	290.00 / 290.00
/ 116.00	12 / 12 / 4 1		
gptr_scan_in	-> gptr_scan_in	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /
0.00	12 / 12 / 1 1		
gptr_a_clk	-> gptr_a_clk	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /
0.00	12 / 12 / 1 1		
gptr_b_clk	-> gptr_b_clk	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /
0.00	12 / 12 / 1 1		
clkg2	-> clkg2	141.00 / 141.00 / 145.52 *	100.00 / 100.00 /
60.00	12 / 12 / 3 1		
eu_iu_fxu_exc_cond	-> eu_iu_fxu_exc_cond	141.00 / 141.00 / 15.67	290.00
/ 290.00 / 390.00 *	12 / 12 / 1 1		
du_iu_store_status(2)	-> du_iu_store_status(2)	141.00 / 141.00 / 16.89	290.00 /
290.00 / 500.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_actn(0)	-> eu_iu_srlz_op_actn(0)	141.00 / 141.00 / 47.57	290.00 /
290.00 / 374.00 *	12 / 12 / 2 1		
eu_iu_srlz_op_actn(1)	-> eu_iu_srlz_op_actn(1)	141.00 / 141.00 / 47.57	290.00 /
290.00 / 341.00 *	12 / 12 / 2 1		
num_dcd_cyl(1)	-> num_dcd_cyl(1)	141.00 / 141.00 / 318.91 *	290.00 /
290.00 / 80.00	12 / 12 / 1 1		
eu_iu_srlz_op_encode(0)	-> eu_iu_srlz_op_encode(0)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 401.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(1)	-> eu_iu_srlz_op_encode(1)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 400.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(2)	-> eu_iu_srlz_op_encode(2)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 420.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(3)	-> eu_iu_srlz_op_encode(3)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 302.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(4)	-> eu_iu_srlz_op_encode(4)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 406.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(5)	-> eu_iu_srlz_op_encode(5)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 373.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(6)	-> eu_iu_srlz_op_encode(6)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 354.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(7)	-> eu_iu_srlz_op_encode(7)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 398.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(8)	-> eu_iu_srlz_op_encode(8)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 367.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(9)	-> eu_iu_srlz_op_encode(9)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 323.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(11)	-> eu_iu_srlz_op_encode(11)	141.00 / 141.00 / 16.89	

290.00 / 290.00 / 500.00 * 12 / 12 / 1 1
 c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1 78.50 / 78.50 / 220.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1 78.50 / 78.50 / 222.27 *
 200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1 78.50 / 78.50 / 212.39 *
 200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2 78.50 / 78.50 / 239.36 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2 78.50 / 78.50 / 228.73 *
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3 78.50 / 78.50 / 239.37 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL

	Capacitance	Slew	Sink
Fanout			
Pin/Port -> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual	
Limit / AdjLim / Actual			
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4		78.50 / 78.50 / 239.36 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5		78.50 / 78.50 / 237.91 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1		78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2		78.50 / 78.50 / 239.37 *	

```

200.00 / 200.00 / 60.00    12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
cka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka          78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79    12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
y@C167:cs_invvn01c          -> dcd_succ_last_t1&0          70.00 / 70.00 / 1011.00 * 301.00
/ 301.00 / 3294.02 * 12 / 12 / 1 1 KEEP_BTR
y@C1994:cs_invvn01c          -> N1531          68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02    12 / 12 / 2 2
y@C2013:cs_invvn01c          -> N18&0          68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3608.92 * 12 / 12 / 1 1
y@C2082:cs_invvn01c          -> N146&0          68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 * 12 / 12 / 1 1
y@C2194:cs_invvn07c          -> N1681          261.00 / 261.00 / 271.46 * 290.00 /
290.00 / 261.53    12 / 12 / 7 7
y@C2393:cs_nnd2v02c          -> iu_reset_op_c_t1&0          71.00 / 71.00 / 1044.40 *
290.00 / 290.00 / 3371.12 * 12 / 12 / 3 3
y@C2425:cs_invvn01c          -> N1815          68.00 / 68.00 / 125.56 * 290.00 /
290.00 / 451.90 * 12 / 12 / 1 1
y@C2496:cs_nnd4n03c          -> N1435          85.00 / 85.00 / 97.67 * 290.00 /
290.00 / 353.82 * 12 / 12 / 5 5
y@C2646:cs_invvn04c          -> N1645          133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 275.60    12 / 12 / 6 6
y@C2726:cs_nnd2n11c          -> dsucc_or_agi&0          500.00 / 500.00 / 540.60 *
290.00 / 290.00 / 258.01    12 / 12 / 2 2
y@C2744:cs_invvn13c          -> N2086&0          996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 271.62    12 / 12 / 7 7
y@C2800:cs_invvn08c          -> N1290          326.00 / 326.00 / 234.15 * 290.00 /
290.00 / 193.42    12 / 12 / 14 * 14
y@C2728rwr:cs_invvn05c          -> N1097          167.00 / 167.00 / 183.47 * 290.00 /
290.00 / 266.58    12 / 12 / 4 4
y@C2918:cs_nor2n04c          -> N2016          110.00 / 110.00 / 132.34 * 290.00 /
290.00 / 428.15 * 12 / 12 / 1 1
y@gbfocell_0:cs_invvn12c          -> gbfonet_0          797.00 / 797.00 / 402.55 * 290.00 /
290.00 / 149.98    12 / 12 / 20 * 20
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q          247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45    12 / 12 / 8 8

```

[BD-500900]: (W) There were 64 electrical violations.
> measure

The model <IDCDSUC> has:

```

Primary Inputs    =      122
Primary Outputs   =       73
Primary BIDs      =        0
Signals           =     1129
Gate Count        =      906
Connections       =     1744
Master REG Bits   =       83
Slave REG Bits    =       83
Internal Area     =     4676
External Area     =        0
Gates/Connects   =     0.519495
Fanout Count      =     1744
Average Fanout    =     1.544730

```

Avg Tech Box Size = 5.161148
 Tech Box Size Stddev = 0.011242
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 754
 Real boxes = 531
 Real connections = 1369
 Real LSTs = 2123
 Real ICells/box = 8.806026
 Real LSTs/box = 3.998117
 Real nets/box = 1.419962

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
6		cs_ao22n03c	03c	>	AOI	6	0	0.000	36	0	0.000
2		cs_ao12n03c	03c	>	AOI	4	0	0.000	8	0	0.000
1		cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000
1		cs_ao22n04c	04c	>	AOI	6	0	0.000	6	0	0.000
1		cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000
1		cs_ao12n07c	07c	>	AOI	6	0	0.000	6	0	0.000
180		BRKPT	>	BRKPT	0	0	0.000	0	0	0.000	
195		IOPAD	>	IOPAD	0	0	0.000	0	0	0.000	
141		cs_nnd2n02c	02c	>	NAND	3	0	0.000	423	0	0.000
19		cs_nnd2n04c	04c	>	NAND	3	0	0.000	57	0	0.000
1		cs_nnd2v05c	05c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd2n12c	12c	>	NAND	12	0	0.000	12	0	0.000
18		cs_nnd3n02c	02c	>	NAND	4	0	0.000	72	0	0.000
1		cs_nnd3v02c	02c	>	NAND	4	0	0.000	4	0	0.000
3		cs_nnd2v13c	13c	>	NAND	15	0	0.000	45	0	0.000
3		cs_nnd2n03c	03c	>	NAND	3	0	0.000	9	0	0.000
5		cs_nnd4n03c	03c	>	NAND	5	0	0.000	25	0	0.000
2		cs_nnd3n03c	03c	>	NAND	4	0	0.000	8	0	0.000
2		cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	0.000
2		cs_nnd2x14c	14c	>	NAND	24	0	0.000	48	0	0.000
1		cs_nnd2v02c	02c	>	NAND	3	0	0.000	3	0	0.000
1		cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
4		cs_nnd2x14e	14e	>	NAND	20	0	0.000	80	0	0.000
2		cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1		cs_nnd2x14b	14b	>	NAND	28	0	0.000	28	0	0.000
1		cs_nnd3i11b	11b	>	NAND	30	0	0.000	30	0	0.000
1		cs_nnd4v10c	10c	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd2g14e	14e	>	NAND	23	0	0.000	23	0	0.000
1		cs_nnd4v10b	10b	>	NAND	20	0	0.000	20	0	0.000
1		cs_nnd2n08c	08c	>	NAND	7	0	0.000	7	0	0.000
1		cs_nnd2v14c	14c	>	NAND	19	0	0.000	19	0	0.000
2		cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1		cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd2v11c	11c	>	NAND	11	0	0.000	11	0	0.000
1		cs_nnd2g11b	11b	>	NAND	19	0	0.000	19	0	0.000
1		cs_nnd3z10c	10c	>	NAND	18	0	0.000	18	0	0.000
1		cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1		cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000

2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
7	cs_nor2n02c	02c	>	NOR	3	0	0.000	21	0	0.000
4	cs_nor2n04c	04c	>	NOR	3	0	0.000	12	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2g12e	12e	>	NOR	27	0	0.000	27	0	0.000
1	cs_nor3v10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2v11c	11c	>	NOR	11	0	0.000	11	0	0.000
1	cs_invvv01c	01c	>	NOT	2	0	0.000	2	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
5	cs_invvn09c	09c	>	NOT	4	0	0.000	20	0	0.000
48	cs_invvn07c	07c	>	NOT	2	0	0.000	96	0	0.000
49	cs_invvn01c	01c	>	NOT	2	0	0.000	98	0	0.000
6	cs_invvn15c	15c	>	NOT	10	0	0.000	60	0	0.000
3	cs_invvn11c	11c	>	NOT	6	0	0.000	18	0	0.000
4	cs_invvn13c	13c	>	NOT	8	0	0.000	32	0	0.000
1	cs_invvv19b	19b	>	NOT	28	0	0.000	28	0	0.000
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn08c	08c	>	NOT	4	0	0.000	12	0	0.000
3	cs_invvn02c	02c	>	NOT	2	0	0.000	6	0	0.000
2	cs_invvv14c	14c	>	NOT	8	0	0.000	16	0	0.000
12	cs_invvn04c	04c	>	NOT	2	0	0.000	24	0	0.000
8	cs_invvn05c	05c	>	NOT	2	0	0.000	16	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv13b	13b	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv13c	13c	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv10c	10c	>	NOT	4	0	0.000	4	0	0.000
1	cs_invvn16c	16c	>	NOT	14	0	0.000	14	0	0.000
1	cs_invvv09c	09c	>	NOT	4	0	0.000	4	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
1	cs_oa21n10c	10c	>	OAI	14	0	0.000	14	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
1	cs_oa21n10e	10e	>	OAI	14	0	0.000	14	0	0.000
22	cl_invvn07d	07d	>	REG	25	0	0.000	550	0	0.000
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

of
Levels Output

0	1	*
1	59	50* plus *****
2	1	*
3	4	****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
----------------	----------

0	7	*****
2	21	*****
3	1	*
4	5	****
5	6	*****
6	9	*****
9	1	*
10	6	*****
12	2	**
13	1	*
14	6	*****
15	7	*****
16	4	****
17	14	*****

The Histogram Of Fanin vs. Box

# of Fanin	Ops
---------------	-----

1	366	350* plus *****
2	202	200* plus **
3	35	*****
4	18	*****

The Histogram Of Fanout vs. Net

# of Fanout	Nets
----------------	------

0	2	**
1	931	900* plus *****
2	96	50* plus *****
3	37	*****
4	16	*****
5	8	*****
6	13	*****
7	3	***
8	3	***
13	3	***
14	16	*****

[End of measure]

[measure]: Execution time was 0.8 seconds.

> slackhist

[slackhist]: CMVC version 1.6 compiled on Mar 31 1999 at 11:27:25.

[slackhist]: worst = -1669.49, best = 1019.49, stddev=716.94 maxfanout 20

[slackhist]: avg = -125.33, delta = 0.50, intervals = 50

[slackhist]:

Distribution of Slacks for All Nets

[slackhist]: Worst -1669.49, Best 1019.49

[slackhist]: Avg -125.33, Std Dev 716.94

[slackhist]: Low to High: Number Percent Cum Percent

[slackhist]: -1669.50 to -1669.00: 7 0.62 0.62

[slackhist]:

[slackhist]: Above -1644.50: 817 72.36 72.98

[slackhist]: Other nets: 305 27.02 100.00

> prtdelay

[BD-500000]: prtdelay CMVC version 1.4 compiled on Apr 13 1999 at 18:31:38

[BD-501900]: Worst arrival time in the network is 2668.493164.

> write_end_point_report -points 10

[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:35 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 10

Cause of Slack Abbreviation Comparison/Description

Cause of Slack	Abbreviation	Comparison/Description
Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AssrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2

ARRIVAL TIME + ADJUST)

Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST)

Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	----------------------------------	-------

1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO		0
dcd_succ_last_t1								
RAT		999				0		
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1								
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD	
0 dcd_succ_last_t1&0								
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT	
0 dcd_succ_last_t1&0								
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT	
1594 N675								
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND	
0 N675								
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND	
19 last_cycle								
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e NAND	
0 last_cycle								
----> C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e NAND	
21 N1587								
----> C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b NOT	0
N1587								
----> C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b NOT	
11 num_dcd_cyl&0(1)								
----> BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD	
0 num_dcd_cyl&0(1)								
----> BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD	0
num_dcd_cyl(1)								
----> num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI		0
num_dcd_cyl(1)								

2 iu_reset_op_c_t1	R C3+R	2399	-1400	3318	1011	1 PO		0
iu_reset_op_c_t1								
RAT		999				0		
----> BOX716/OUT	R C3+R	2399	-1400	3318	1011	1 IOPAD	IOPAD	
0 iu_reset_op_c_t1								
----> BOX716/IN	R C3+R	2399	-1400	3318	1044	3 IOPAD	IOPAD	
0 iu_reset_op_c_t1&0								
---->{a} C2393/y	R C3+R	2399	-1400	3318	1044	3 cs_nnd2v	02c NAND	
0 iu_reset_op_c_t1&0								
----> C2393/a	F C3+R	536	-1400	100	196	6 cs_nnd2v	02c NAND	
1863 gbfonet_6								
----> gbfcocell_6/y	F C3+R	536	-1400	100	196	6 cs_invvv	09c NOT	
0 gbfonet_6								
----> gbfcocell_6/a	R C3+R	472	-1400	184	44	1 cs_invvv	09c NOT	


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64 N2031
---->{b} C2162/y          R C3+R    472 -1400  184  44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a             F C3+R    358 -1400  144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R    358 -1400  144  217 5 cl_inwn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2             R C3+    160  N/C   60  222 13 cl_inwn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2              R C3+    160  N/C   60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

-----
--
3 dcd_succ_last_t1          F C3+R    2352 -1353  1874  1011 1 PO          0
dcd_succ_last_t1
RAT                          999                                0
----> BOX714/OUT            F C3+R    2352 -1353  1874  1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1
----> BOX714/IN            F C3+R    2352 -1353  1874  1011 1 IOPAD      IOPAD
0 dcd_succ_last_t1&0
----> C167/y              F C3+R    2352 -1353  1874  1011 1 cs_invvv  01c NOT
0 dcd_succ_last_t1&0
----> C167/a              R C3+R    1144 -1353   69  139 4 cs_invvv  01c NOT
1208 N675
---->{a} C2738/y          R C3+R    1144 -1353   69  139 4 cs_nnd2x  14b NAND
0 N675
----> C2738/b            F C3+R    1095 -1353   64  178 3 cs_nnd2x  14b NAND
49 N1692
---->{b} C2725rwr/y      F C3+R    1095 -1353   64  178 3 cs_nnd2g  14e NAND
0 N1692
----> C2725rwr/a        R C3+R    1049 -1353  116  170 2 cs_nnd2g  14e NAND
46 N1479
---->{c} C2721rwr/y      R C3+R    1049 -1353  116  170 2 cs_nnd3i  11b NAND
0 N1479
----> C2721rwr/b        F C3+R    981 -1353   34  113 2 cs_nnd3i  11b NAND
67 N892
---->{d} C2338/y        F C3+R    981 -1353   34  113 2 cs_nnd2x  14c NAND
0 N892
----> C2338/a          R C3+R    958 -1353   62  159 3 cs_nnd2x  14c NAND
23 N1119
----> C2905/y          R C3+R    958 -1353   62  159 3 cs_invvv  13b NOT    0
N1119
----> C2905/a          F C3+R    918 -1353   63   92 1 cs_invvv  13b NOT    41
N2010
---->{e} C2906/y        F C3+R    918 -1353   63   92 1 cs_nor2g  12e NOR
0 N2010
----> C2906/b          R C3+R    868 -1353   80  124 1 cs_nor2g  12e NOR
50 dcd_blk_dsucc&0
----> BOX644/OUT        R C3+R    868 -1353   80  124 1 IOPAD      IOPAD
0 dcd_blk_dsucc&0
----> BOX644/IN        R C3+R    868 -1353   80  124 1 IOPAD      IOPAD    0
dcd_blk_dsucc
----> dcd_blk_dsucc      R C3+R    868 -1353   80  124 1 PI          0
dcd_blk_dsucc

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```

--
    4 local_milli_t2.reg_n.lat_0/a      F C3+R   2650 -1340   96   92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t2.reg_n.lat_0/c1    F C3-     160         60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                      F C3+R   2650 -1340   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R   2590 -1340  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                      R C3+R   2590 -1340  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R   2510 -1340  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                      F C3+R   2510 -1340  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R   2399 -1340 3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                      R C3+R   2399 -1400 3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a                          F C3+R   536  -1400  100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfcoll_6/y                      F C3+R   536  -1400  100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfcoll_6/a                      R C3+R   472  -1400  184   44 1 cs_invvv  09c NOT
64 N2031
---->{e} C2162/y                      R C3+R   472  -1400  184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a                          F C3+R   358  -1400  144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   358  -1400  144  217 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
    5 local_milli_t1.reg_n.lat_0/a      F C3+R   2650 -1340   96   92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli_t1.reg_n.lat_0/c1    F C3-     160         60  238 14 cl_invvn  07c
1200 slow_mode.c1_4
---->{a} BOX789/y                      F C3+R   2650 -1340   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a                          R C3+R   2590 -1340  120   32 1 cs_nnd3z  07c NAND
60 NET1054
---->{b} BOX785/y                      R C3+R   2590 -1340  120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a                          F C3+R   2510 -1340  158   19 1 cs_nnd2f  03c NAND
81 N1866
---->{c} C2555/y                      F C3+R   2510 -1340  158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b                          R C3+R   2399 -1340 3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/y                      R C3+R   2399 -1400 3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0

```

```

----> C2393/a          F C3+R   536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfozell_6/y      F C3+R   536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfozell_6/a      R C3+R   472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
----> {e} C2162/y       R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a          F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n F C3+R   358 -1400   144  217 5 cl_invvn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
6 local_milli.reg_n.lat_0/a      F C3+R   2650 -1340   96   92 3 cl_invvn  07c SRL
50 NET1056
Setup local_milli.reg_n.lat_0/c1 F C3-    160         60  238 14 cl_invvn  07c   1200
slow_mode.c1_2
----> {a} BOX789/y      F C3+R   2650 -1340   96   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/a          R C3+R   2590 -1340   120   32 1 cs_nnd3z  07c NAND
60 NET1054
----> {b} BOX785/y      R C3+R   2590 -1340   120   32 1 cs_nnd2f  03c NAND
0 NET1054
----> BOX785/a          F C3+R   2510 -1340   158   19 1 cs_nnd2f  03c NAND
81 N1866
----> {c} C2555/y       F C3+R   2510 -1340   158   19 1 cs_ao12n  03c AOI
0 N1866
----> C2555/b           R C3+R   2399 -1340  3318 1044 3 cs_ao12n  03c AOI
110 iu_reset_op_c_t1&0
----> {d} C2393/y       R C3+R   2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfozell_6/y      F C3+R   536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfozell_6/a      R C3+R   472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
----> {e} C2162/y       R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a          F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n F C3+R   358 -1400   144  217 5 cl_invvn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
7 local_milli_t2.reg_n.lat_0/a    R C3+R   2582 -1225   145   92 3 cl_invvn  07c SRL

```

```

3 NET1056
Setup local_milli_t2.reg_n.lat_0/c1      F C3-    160      60 238 14 cl_invvn 07c
1200 slow_mode.c1_4
---->{a} BOX789/y      R C3+R    2582 -1225 145 92 3 cs_nnd3z 07c NAND
0 NET1056
----> BOX789/b      F C3+R    2486 -1225 132 36 1 cs_nnd3z 07c NAND
96 N639
---->{b} C2466/y      F C3+R    2486 -1225 132 36 1 cs_nnd2n 02c NAND
0 N639
----> C2466/b      R C3+R    2399 -1225 3318 1044 3 cs_nnd2n 02c NAND
86 iu_reset_op_c_t1&0
---->{c} C2393/y      R C3+R    2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a      F C3+R    536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6
----> gbfozell_6/y    F C3+R    536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6
----> gbfozell_6/a    R C3+R    472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031
---->{d} C2162/y      R C3+R    472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031
----> C2162/a      F C3+R    358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n    F C3+R    358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C   60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2      R C3+    160   N/C   60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

8 local_milli_t1.reg_n.lat_0/a      R C3+R    2582 -1225 145 92 3 cl_invvn 07c SRL
3 NET1056
Setup local_milli_t1.reg_n.lat_0/c1      F C3-    160      60 238 14 cl_invvn 07c
1200 slow_mode.c1_4
---->{a} BOX789/y      R C3+R    2582 -1225 145 92 3 cs_nnd3z 07c NAND
0 NET1056
----> BOX789/b      F C3+R    2486 -1225 132 36 1 cs_nnd3z 07c NAND
96 N639
---->{b} C2466/y      F C3+R    2486 -1225 132 36 1 cs_nnd2n 02c NAND
0 N639
----> C2466/b      R C3+R    2399 -1225 3318 1044 3 cs_nnd2n 02c NAND
86 iu_reset_op_c_t1&0
---->{c} C2393/y      R C3+R    2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a      F C3+R    536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6
----> gbfozell_6/y    F C3+R    536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6
----> gbfozell_6/a    R C3+R    472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031
---->{d} C2162/y      R C3+R    472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031
----> C2162/a      F C3+R    358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q

```

```

----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R   358 -1400  144  217 5 cl_invrn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2              R C3+    160   N/C   60  222 13 cl_invrn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2                R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
    9 local_milli.reg_n.lat_0/a              R C3+R   2582 -1225  145   92 3 cl_invrn  07c SRL
3 NET1056
Setup local_milli.reg_n.lat_0/c1            F C3-    160         60  238 14 cl_invrn  07c    1200
slow_mode.c1_2
----> {a} BOX789/y                          R C3+R   2582 -1225  145   92 3 cs_nnd3z  07c NAND
0 NET1056
----> BOX789/b                              F C3+R   2486 -1225  132   36 1 cs_nnd3z  07c NAND
96 N639
----> {b} C2466/y                            F C3+R   2486 -1225  132   36 1 cs_nnd2n  02c NAND
0 N639
----> C2466/b                                R C3+R   2399 -1225  3318  1044 3 cs_nnd2n  02c NAND
86 iu_reset_op_c.t1&0
----> {c} C2393/y                            R C3+R   2399 -1400  3318  1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c.t1&0
----> C2393/a                                F C3+R    536 -1400  100  196 6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfozell_6/y                          F C3+R    536 -1400  100  196 6 cs_invrn  09c NOT
0 gbfonet_6
----> gbfozell_6/a                          R C3+R    472 -1400  184   44 1 cs_invrn  09c NOT
64 N2031
----> {d} C2162/y                            R C3+R    472 -1400  184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a                                F C3+R    358 -1400  144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n      F C3+R   358 -1400  144  217 5 cl_invrn  07d
SRL      0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2              R C3+    160   N/C   60  222 13 cl_invrn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2                R C3+    160   N/C   60  222 13 cb_clk_32_1  LCB
0 slow_mode.c2_1
-----
--
    10 idcdsuc_err                          R C3+R   2126 -1127  3605  1011 1 PO          0
N146
RAT                                          999          0
----> BOX750/OUT                              R C3+R   2126 -1127  3605  1011 1 IOPAD    IOPAD
0 N146
----> BOX750/IN                              R C3+R   2126 -1127  3605  1011 1 IOPAD    IOPAD
0 N146&0
----> C2082/y                                R C3+R   2126 -1127  3605  1011 1 cs_invrn  01c NOT
0 N146&0
----> C2082/a                                F C3+R    295 -1127   48   32 2 cs_invrn  01c NOT
1831 dcdsuc_err_q
----> dcdsuc_err.reg_n.lat_0/l2_out_n        F C3+R    295 -1127   48   32 2 cl_nnd2n  07c
SRL      0 dcdsuc_err_q
----> dcdsuc_err.reg_n.lat_0/c2              R C3+    160   N/C   60  222 13 cl_nnd2n  07c SRL
135 slow_mode.c2_1

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----> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
 0 slow_mode.c2_1

--
 > measure

The model <IDCDSUC> has:

Primary Inputs = 122
 Primary Outputs = 73
 Primary BIDs = 0
 Signals = 1129
 Gate Count = 906
 Connections = 1744
 Master REG Bits = 83
 Slave REG Bits = 83
 Internal Area = 4676
 External Area = 0
 Gates/Connects = 0.519495
 Fanout Count = 1744
 Average Fanout = 1.544730
 Avg Tech Box Size = 5.161148
 Tech Box Size Stddev = 0.011242
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 754
 Real boxes = 531
 Real connections = 1369
 Real LSTs = 2123
 Real ICells/box = 8.806026
 Real LSTs/box = 3.998117
 Real nets/box = 1.419962

Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
6	cs_ao22n03c	03c >	AOI	6	0	0.000	36	0	0.000		
2	cs_ao12n03c	03c >	AOI	4	0	0.000	8	0	0.000		
1	cs_ao12n10c	10c >	AOI	12	0	0.000	12	0	0.000		
1	cs_ao22n04c	04c >	AOI	6	0	0.000	6	0	0.000		
1	cs_ao22n10c	10c >	AOI	18	0	0.000	18	0	0.000		
1	cs_ao12n07c	07c >	AOI	6	0	0.000	6	0	0.000		
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
141	cs_nnd2n02c	02c >	NAND	3	0	0.000	423	0	0.000		
19	cs_nnd2n04c	04c >	NAND	3	0	0.000	57	0	0.000		
1	cs_nnd2v05c	05c >	NAND	4	0	0.000	4	0	0.000		
1	cs_nnd2n12c	12c >	NAND	12	0	0.000	12	0	0.000		
18	cs_nnd3n02c	02c >	NAND	4	0	0.000	72	0	0.000		
1	cs_nnd3v02c	02c >	NAND	4	0	0.000	4	0	0.000		
3	cs_nnd2v13c	13c >	NAND	15	0	0.000	45	0	0.000		
3	cs_nnd2n03c	03c >	NAND	3	0	0.000	9	0	0.000		
5	cs_nnd4n03c	03c >	NAND	5	0	0.000	25	0	0.000		
2	cs_nnd3n03c	03c >	NAND	4	0	0.000	8	0	0.000		
2	cs_nnd2n11c	11c >	NAND	11	0	0.000	22	0	0.000		

2	cs_nnd2x14c	14c	>	NAND	24	0	0.000	48	0	0.000
1	cs_nnd2v02c	02c	>	NAND	3	0	0.000	3	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
4	cs_nnd2x14e	14e	>	NAND	20	0	0.000	80	0	0.000
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	8	0	0.000
1	cs_nnd2x14b	14b	>	NAND	28	0	0.000	28	0	0.000
1	cs_nnd3i11b	11b	>	NAND	30	0	0.000	30	0	0.000
1	cs_nnd4v10c	10c	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd2g14e	14e	>	NAND	23	0	0.000	23	0	0.000
1	cs_nnd4v10b	10b	>	NAND	20	0	0.000	20	0	0.000
1	cs_nnd2n08c	08c	>	NAND	7	0	0.000	7	0	0.000
1	cs_nnd2v14c	14c	>	NAND	19	0	0.000	19	0	0.000
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd2v11c	11c	>	NAND	11	0	0.000	11	0	0.000
1	cs_nnd2g11b	11b	>	NAND	19	0	0.000	19	0	0.000
1	cs_nnd3z10c	10c	>	NAND	18	0	0.000	18	0	0.000
1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
7	cs_nor2n02c	02c	>	NOR	3	0	0.000	21	0	0.000
4	cs_nor2n04c	04c	>	NOR	3	0	0.000	12	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2g12e	12e	>	NOR	27	0	0.000	27	0	0.000
1	cs_nor3v10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2v11c	11c	>	NOR	11	0	0.000	11	0	0.000
1	cs_invvv01c	01c	>	NOT	2	0	0.000	2	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
5	cs_invvn09c	09c	>	NOT	4	0	0.000	20	0	0.000
48	cs_invvn07c	07c	>	NOT	2	0	0.000	96	0	0.000
49	cs_invvn01c	01c	>	NOT	2	0	0.000	98	0	0.000
6	cs_invvn15c	15c	>	NOT	10	0	0.000	60	0	0.000
3	cs_invvn11c	11c	>	NOT	6	0	0.000	18	0	0.000
4	cs_invvn13c	13c	>	NOT	8	0	0.000	32	0	0.000
1	cs_invvv19b	19b	>	NOT	28	0	0.000	28	0	0.000
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn08c	08c	>	NOT	4	0	0.000	12	0	0.000
3	cs_invvn02c	02c	>	NOT	2	0	0.000	6	0	0.000
2	cs_invvv14c	14c	>	NOT	8	0	0.000	16	0	0.000
12	cs_invvn04c	04c	>	NOT	2	0	0.000	24	0	0.000
8	cs_invvn05c	05c	>	NOT	2	0	0.000	16	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv13b	13b	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv13c	13c	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv10c	10c	>	NOT	4	0	0.000	4	0	0.000
1	cs_invvn16c	16c	>	NOT	14	0	0.000	14	0	0.000
1	cs_invvv09c	09c	>	NOT	4	0	0.000	4	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
1	cs_oa21n10c	10c	>	OAI	14	0	0.000	14	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
1	cs_oa21n10e	10e	>	OAI	14	0	0.000	14	0	0.000
22	cl_invvn07d	07d	>	REG	25	0	0.000	550	0	0.000
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000

1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels	Output
0	1 *
1	59 50* plus *****
2	1 *
3	4 ****
4	1 *
10	3 ***
11	1 *
12	3 ***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

# of Levels	Register
0	7 *****
2	21 *****
3	1 *
4	5 *****
5	6 *****
6	9 *****
9	1 *
10	6 *****
12	2 **
13	1 *
14	6 *****
15	7 *****
16	4 ****
17	14 *****

The Histogram Of Fanin vs. Box

# of Fanin	Ops
1	366 350* plus *****
2	202 200* plus **


```

3    35 *****
4    18 *****

```

The Histogram Of Fanout vs. Net

```

# of
Fanout Nets
-----
0    2  **
1   931 900* plus *****
2    96 50* plus *****
3    37 *****
4    16 *****
5     8 *****
6    13 *****
7     3 ***
8     3 ***
13    3 ***
14   16 *****
20    1  *

```

[End of measure]

[measure]: Execution time was 0.8 seconds.

```

> randsim q
[
>>]: randsim( q );
> randsim q
[
>>]: randsim( q );
> good_names

```

Good names for IDCDSUC

	Count	User	Like	New
For all nets	1129	80.96%	17.45%	1.59%
For register output nets	166	100.00%	0.00%	0.00%
For break point input nets	180	99.44%	0.56%	0.00%
For model input/output nets	195	99.49%	0.51%	0.00%

	Count	User	Like	New
For all boxes	906	58.17%	0.00%	41.83%
For register boxes	83	100.00%	0.00%	0.00%

> summary_report

The model <IDCDSUC> has:

```

Primary Inputs    =    122
Primary Outputs   =     73
Primary BIDs      =      0
Signals           =   1129
Gate Count        =    906
Connections       =   1744
Master REG Bits   =     83
Slave REG Bits    =     83
Internal Area     =   4676
External Area     =      0

```

Gates/Connects = 0.519495
 Fanout Count = 1744
 Average Fanout = 1.544730
 Avg Tech Box Size = 5.161148
 Tech Box Size Stddev = 0.011242
 Power = 0.000000

R-E-A-LS-T-A-T-I-S-T-I-C-S***

Real signals = 754
 Real boxes = 531
 Real connections = 1369
 Real LSTs = 2123
 Real ICells/box = 8.806026
 Real LSTs/box = 3.998117
 Real nets/box = 1.419962
 Cell Total
 Each Cell

Type	Cnt	Boxname	Power	Level	Function	Int	Ext	Power	Int	Ext	Power
6	cs_ao22n03c	03c >	AOI	6	0	0.000	36	0	0.000		
2	cs_ao12n03c	03c >	AOI	4	0	0.000	8	0	0.000		
1	cs_ao12n10c	10c >	AOI	12	0	0.000	12	0	0.000		
1	cs_ao22n04c	04c >	AOI	6	0	0.000	6	0	0.000		
1	cs_ao22n10c	10c >	AOI	18	0	0.000	18	0	0.000		
1	cs_ao12n07c	07c >	AOI	6	0	0.000	6	0	0.000		
180	BRKPT	>	BRKPT	0	0	0.000	0	0	0.000		
195	IOPAD	>	IOPAD	0	0	0.000	0	0	0.000		
141	cs_nnd2n02c	02c >	NAND	3	0	0.000	423	0	0.000		
19	cs_nnd2n04c	04c >	NAND	3	0	0.000	57	0	0.000		
1	cs_nnd2v05c	05c >	NAND	4	0	0.000	4	0	0.000		
1	cs_nnd2n12c	12c >	NAND	12	0	0.000	12	0	0.000		
18	cs_nnd3n02c	02c >	NAND	4	0	0.000	72	0	0.000		
1	cs_nnd3v02c	02c >	NAND	4	0	0.000	4	0	0.000		
3	cs_nnd2v13c	13c >	NAND	15	0	0.000	45	0	0.000		
3	cs_nnd2n03c	03c >	NAND	3	0	0.000	9	0	0.000		
5	cs_nnd4n03c	03c >	NAND	5	0	0.000	25	0	0.000		
2	cs_nnd3n03c	03c >	NAND	4	0	0.000	8	0	0.000		
2	cs_nnd2n11c	11c >	NAND	11	0	0.000	22	0	0.000		
2	cs_nnd2x14c	14c >	NAND	24	0	0.000	48	0	0.000		
1	cs_nnd2v02c	02c >	NAND	3	0	0.000	3	0	0.000		
1	cs_nnd3n07c	07c >	NAND	6	0	0.000	6	0	0.000		
4	cs_nnd2x14e	14e >	NAND	20	0	0.000	80	0	0.000		
2	cs_nnd2n07c	07c >	NAND	4	0	0.000	8	0	0.000		
1	cs_nnd2x14b	14b >	NAND	28	0	0.000	28	0	0.000		
1	cs_nnd3i11b	11b >	NAND	30	0	0.000	30	0	0.000		
1	cs_nnd4v10c	10c >	NAND	20	0	0.000	20	0	0.000		
1	cs_nnd2g14e	14e >	NAND	23	0	0.000	23	0	0.000		
1	cs_nnd4v10b	10b >	NAND	20	0	0.000	20	0	0.000		
1	cs_nnd2n08c	08c >	NAND	7	0	0.000	7	0	0.000		
1	cs_nnd2v14c	14c >	NAND	19	0	0.000	19	0	0.000		
2	cs_nnd3n05c	05c >	NAND	6	0	0.000	12	0	0.000		
1	cs_nnd2n05c	05c >	NAND	4	0	0.000	4	0	0.000		
1	cs_nnd2v11c	11c >	NAND	11	0	0.000	11	0	0.000		
1	cs_nnd2g11b	11b >	NAND	19	0	0.000	19	0	0.000		
1	cs_nnd3z10c	10c >	NAND	18	0	0.000	18	0	0.000		

1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000
7	cs_nor2n02c	02c	>	NOR	3	0	0.000	21	0	0.000
4	cs_nor2n04c	04c	>	NOR	3	0	0.000	12	0	0.000
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000
1	cs_nor2g12e	12e	>	NOR	27	0	0.000	27	0	0.000
1	cs_nor3v10e	10e	>	NOR	16	0	0.000	16	0	0.000
1	cs_nor2v11c	11c	>	NOR	11	0	0.000	11	0	0.000
1	cs_invvv01c	01c	>	NOT	2	0	0.000	2	0	0.000
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000
6	cs_invvn10c	10c	>	NOT	4	0	0.000	24	0	0.000
5	cs_invvn09c	09c	>	NOT	4	0	0.000	20	0	0.000
48	cs_invvn07c	07c	>	NOT	2	0	0.000	96	0	0.000
49	cs_invvn01c	01c	>	NOT	2	0	0.000	98	0	0.000
6	cs_invvn15c	15c	>	NOT	10	0	0.000	60	0	0.000
3	cs_invvn11c	11c	>	NOT	6	0	0.000	18	0	0.000
4	cs_invvn13c	13c	>	NOT	8	0	0.000	32	0	0.000
1	cs_invvv19b	19b	>	NOT	28	0	0.000	28	0	0.000
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12	0	0.000
3	cs_invvn08c	08c	>	NOT	4	0	0.000	12	0	0.000
3	cs_invvn02c	02c	>	NOT	2	0	0.000	6	0	0.000
2	cs_invvv14c	14c	>	NOT	8	0	0.000	16	0	0.000
12	cs_invvn04c	04c	>	NOT	2	0	0.000	24	0	0.000
8	cs_invvn05c	05c	>	NOT	2	0	0.000	16	0	0.000
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv13b	13b	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv13c	13c	>	NOT	8	0	0.000	8	0	0.000
1	cs_invvv10c	10c	>	NOT	4	0	0.000	4	0	0.000
1	cs_invvn16c	16c	>	NOT	14	0	0.000	14	0	0.000
1	cs_invvv09c	09c	>	NOT	4	0	0.000	4	0	0.000
1	cs_invvn01e	01e	>	NOT	2	0	0.000	2	0	0.000
1	cs_oa21n10c	10c	>	OAI	14	0	0.000	14	0	0.000
1	cs_oa22n10c	10c	>	OAI	18	0	0.000	18	0	0.000
1	cs_oa21n10e	10e	>	OAI	14	0	0.000	14	0	0.000
22	cl_invvn07d	07d	>	REG	25	0	0.000	550	0	0.000
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0	0.000
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000
1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000
1	cb_mode_block	A	>	SEQUENTIAL	70	0	0.000	70	0	0.000
6	cb_clk_32_1		>	SEQUENTIAL	80	0	0.000	480	0	0.000
1	cs_xbn2n01b	01b	>	XNOR	8	0	0.000	8	0	0.000
1	cs_xbo2n01d	01d	>	XOR	8	0	0.000	8	0	0.000

[End of measure]

[measure]: Execution time was 0.6 seconds.

> write_end_point_report -points 2
 [ET-0018]: >Begin...New EndPoint Report
 for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:38 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation

SlkCont

Slack due to a point downstream on path

Required Arrival Time

RAT

(ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT

(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)

Clock Gating Setup

ClkGSet

(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)

Clock Gating Hold

ClkGHld

(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)

Clock Tree Pulse Width

ClkTPW

(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)

Setup

Setup

(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)

Hold

Hold

(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)

EndOfCycle

EndOfC

(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)

ClockPulseWidth

ClkPW

(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)

ClockSeparation

ClkSep

(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)

Loop

ALTest

(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)

Arrival Time Limiting

ATLimit

Slack discontinuity due to failed test

Num/
Test PinName
NetName

LimitedAT/

E Phase

AT

Slack

Slew

CL

FO

Delay/

Failed Test/

P Func

T.Adj

1 dcd_succ_last_t1

R C3+R

2668

-1669

3294

1011

1 PO

0

dcd_succ_last_t1

RAT

999

0

----> BOX714/OUT

R C3+R

2668

-1669

3294

1011

1 IOPAD

IOPAD

0 dcd_succ_last_t1

----> BOX714/IN

R C3+R

2668

-1669

3294

1011

1 IOPAD

IOPAD

0 dcd_succ_last_t1&0

----> C167/y

R C3+R

2668

-1669

3294

1011

1 cs_invvv

01c NOT

0 dcd_succ_last_t1&0

----> C167/a

F C3+R

1075

-1669

27

139

4 cs_invvv

01c NOT

1594 N675

---->{a} C2738/y

F C3+R

1075

-1669

27

139

4 cs_nnd2x

14b NAND

```

0 N675
----> C2738/a          R C3+R   1056 -1669   33  114 1 cs_nnd2x  14b NAND
19 last_cycle
---->{b} C2487/y      R C3+R   1056 -1669   33  114 1 cs_nnd2x  14e NAND
0 last_cycle
----> C2487/a          F C3+R   1035 -1669   22  145 3 cs_nnd2x  14e NAND
21 N1587
----> C1952/y          F C3+R   1035 -1669   22  145 3 cs_invvv  19b NOT    0
N1587
----> C1952/a          R C3+R   1024 -1669   80  319 1 cs_invvv  19b NOT
11 num_dcd_cyl&0(1)
----> ' BOX679/OUT      R C3+R   1024 -1669   80  319 1 IOPAD      IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN        R C3+R   1024 -1669   80  319 1 IOPAD      IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)    R C3+R   1024 -1669   80  319 1 PI          0
num_dcd_cyl(1)

```

```

--
2 iu_reset_op_c_t1      R C3+R   2399 -1400  3318 1011 1 PO          0
iu_reset_op_c_t1
RAT                      999                      0
----> BOX716/OUT        R C3+R   2399 -1400  3318 1011 1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN        R C3+R   2399 -1400  3318 1044 3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y        R C3+R   2399 -1400  3318 1044 3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a          F C3+R   536 -1400   100  196 6 cs_nnd2v  02c NAND
1863 gbfont_6
----> gbfont_6/y        F C3+R   536 -1400   100  196 6 cs_invvv  09c NOT
0 gbfont_6
----> gbfont_6/a        R C3+R   472 -1400   184   44 1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y        R C3+R   472 -1400   184   44 1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a          F C3+R   358 -1400   144  217 5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n F C3+R   358 -1400   144  217 5 cl_invvn  07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
> msg::get_highest_level
> echo {Highest MsgLevel is error}
Highest MsgLevel is error
> total_area
> echo {Total Area is 4676}
Total Area is 4676
> critical_slack
> echo {Critical Slack is -1669.49328613}
Critical Slack is -1669.49328613

```

> slackhist DELTA(50),INTERVALS(10)

[slackhist]: CMVC version 1.6 compiled on Mar 31 1999 at 11:27:25.

[slackhist]: Slack delta 50.000000

[slackhist]: Max Intervals 10

[slackhist]: worst = -1669.49, best = 1019.49, stddev=716.94 maxfanout 20

[slackhist]: avg = -125.33, delta = 50.00, intervals = 10

[slackhist]:

Distribution of Slacks for All Nets

[slackhist]: Worst -1669.49, Best 1019.49

[slackhist]: Avg -125.33, Std Dev 716.94

[slackhist]: Low to High: Number Percent Cum Percent

[slackhist]: -1700.00 to -1650.00: 7 0.62 0.62

[slackhist]: -1650.00 to -1600.00: 10 0.89 1.51

[slackhist]: -1600.00 to -1550.00: 26 2.30 3.81

[slackhist]: -1550.00 to -1500.00: 17 1.51 5.31

[slackhist]: -1500.00 to -1450.00: 15 1.33 6.64

[slackhist]: -1450.00 to -1400.00: 28 2.48 9.12

[slackhist]: -1400.00 to -1350.00: 13 1.15 10.27

[slackhist]: -1350.00 to -1300.00: 10 0.89 11.16

[slackhist]: -1300.00 to -1250.00: 8 0.71 11.87

[slackhist]: -1250.00 to -1200.00: 10 0.89 12.75

[slackhist]: Above -1200.00: 680 60.23 72.98

[slackhist]: Other nets: 305 27.02 100.00

> write_end_point_report -points 2 -audit

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:38 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation

SlkCont

Slack due to a point downstream on path

Required Arrival Time

RAT

(ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT

(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

TIME)

Clock Gating Setup

ClkGSet

(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

ARRIVAL TIME + ADJUST)

Clock Gating Hold

ClkGHld

(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK

ARRIVAL TIME + ADJUST)

Clock Tree Pulse Width

ClkTPW

(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE)

Setup

Setup

(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +

ADJUST)

Hold

Hold

(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +

ADJUST)

EndOfCycle

EndOfC

(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +

ADJUST)

ClockPulseWidth

ClkPW

(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE)

ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST)

Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST)

Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	----------------------------------------

--							
1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO	0
dcd_succ_last_t1							
RAT	999					0	
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT
1594 N675							
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND
0 N675							
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND
19 last_cycle							
---->{b} C2487/y	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14e NAND
0 last_cycle							
----> C2487/a	F C3+R	1035	-1669	22	145	3 cs_nnd2x	14e NAND
21 N1587							
----> C1952/y	F C3+R	1035	-1669	22	145	3 cs_invvv	19b NOT 0
N1587							
----> C1952/a	R C3+R	1024	-1669	80	319	1 cs_invvv	19b NOT
11 num_dcd_cyl&0(1)							
----> BOX679/OUT	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD
0 num_dcd_cyl&0(1)							
----> BOX679/IN	R C3+R	1024	-1669	80	319	1 IOPAD	IOPAD 0
num_dcd_cyl(1)							
----> num_dcd_cyl(1)	R C3+R	1024	-1669	80	319	1 PI	0
num_dcd_cyl(1)							

--							
2 iu_reset_op_c_t1	R C3+R	2399	-1400	3318	1011	1 PO	0
iu_reset_op_c_t1							
RAT	999					0	
----> BOX716/OUT	R C3+R	2399	-1400	3318	1011	1 IOPAD	IOPAD
0 iu_reset_op_c_t1							
----> BOX716/IN	R C3+R	2399	-1400	3318	1044	3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0							
---->{a} C2393/y	R C3+R	2399	-1400	3318	1044	3 cs_nnd2v	02c NAND
0 iu_reset_op_c_t1&0							
----> C2393/a	F C3+R	536	-1400	100	196	6 cs_nnd2v	02c NAND
1863 gbfontet_6							
----> gbfontet_6/y	F C3+R	536	-1400	100	196	6 cs_invvv	09c NOT

```

0 gbfonet_6
----> gbfcocell_6/a      R C3+R   472  -1400   184   44  1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y        R C3+R   472  -1400   184   44  1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a           F C3+R   358  -1400   144  217  5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n  F C3+R   358  -1400   144  217  5 cl_invvv  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2        R C3+    160   N/C    60  222 13 cl_invvv  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2          R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

--

***** Audit Section *****

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Part: IDCDSUC

Analysis: Late and Early / Nominal

EDA EinsTimer Design Information

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

*** Wire model Information ***

Block	WireModelType	CellCount	ModelName
-------	---------------	-----------	-----------

IDCDSUC	Enclosed	4676	2kCells
---------	----------	------	---------

Pin	ModelName
-----	-----------

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Part: IDCDSUC

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*** General Information ***

DTA Adjust Mode is Edge Based

Clock Limiting is ON

PinToPinNetModel is FALSE

Analysis mode is default

TimeUnitToSeconds= 1.00e-12

LoadUnitToFarads= 1.00e-15

InductanceUnitToHenries= 1.00e+00

ResistanceUnitToOhms= 1.00e+03

ClockGatingPulseWidth= 0.00ns

ClockGatingSetup= 0.00ns

ClockGatingHold= 0.00ns

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Part: IDCDSUC

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Release Level: 03.01

*** Technology Information ***

Block Tech Name

IDCDSUC GENERIC

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Part: IDCDSUC

Analysis: Late and Early / Nominal EDA EinsTimer Design Information

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01 *** Vt, Vdd, Temp ***

Delay Factor WorstCase BestCase Nominal

Technology Type WorstCase BestCase Nominal

GENERIC	Current Temp	10	-10	10
	Current VCM	2	2	2
	Current VDD	1	2	1
	Current VDD150	1	2	2
	Current VDD180	2	2	2
	Current VDD2	3	4	3
	Current VDD250	2	3	2
	Current VDD330	3	4	3
	Current VDDQ	1	2	2
	Current VREF	2	2	2
	Current VTT	1	2	2
	Base Temp	10	-10	10
	Base VCM	2	2	2
	Base VDD	2	3	2
	Base VDD150	1	2	2
	Base VDD180	2	2	2
	Base VDD2	3	4	3
	Base VDD250	2	3	2
	Base VDD330	3	4	3
	Base VDDQ	1	2	2
	Base VREF	2	2	2
	Base VTT	1	2	2

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Part: IDCDSUC

Analysis: Late and Early / Nominal EDA EinsTimer Design Information

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01 *** Voltage Island Information ***

Island Technology Rail WorstCase BestCase Nominal

Cell Island

Block Island

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Part: IDCDSUC

Analysis: Late and Early / Nominal

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

EDA EinsTimer Design Information

*** Phases Definitions ***

*Phase Tleading Ttrailing Cycle

*-----
C3 0 600 1200
C3L 0 600 1200
*-----

CLK_OVERRIDE

*Clock ATr(L) ATf(L) SLwr(L) SLwf(L) ATr(E) ATf(E) SLwr(E) SLwf(E)

*-----
C3 160 750 60 60 160 750 60 60
C3L 160 750 60 60 160 750 60 60
*-----

CLK_TREE_OVERRIDE

*Clock ATr(L) ATf(L) SLwr(L) SLwf(L) ATr(E) ATf(E) SLwr(E) SLwf(E)

*-----
*-----

CLK_PAIR_EXCLUSION

*Clock1 Clock2

*-----
*-----

USER_DELTA_ADJUST

*Clock1 Clock2 Edge1 Edge2 Test

Adjust

*-----
*-----

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Part: IDCDSUC

Analysis: Late and Early / Nominal

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

EDA EinsTimer Design Information

*** Pls and Asserted Arrival Times ***

Pin Phase ATr(L) ATf(L) SLwr(L) SLwf(L) ATr(E) ATf(E) SLwr(E) SLwf(E)
Signal/Net

op_dsbl_after C3+R 1022 1101 80 80 391 387 83 80
op_dsbl_after C3+R 465 430 204 195 215 196 80 80
eu_iu_spare1 C3+R 465 437 135 80 263 251 80 80
second_op_lat
second_op_lat

mcr41_trap	C3+R	700	674	125	105	287	283	80	80	mcr41_trap
ifet_xcptn	C3+R	931	939	141	117	351	358	102	87	ifet_xcptn
iu_eu_xcptPend	C3+R	491	468	117	98	272	258	80	80	
iu_eu_xcptPend										
iq_blk_d1	C3+R	580	570	108	110	278	274	80	80	iq_blk_d1
clk1_mode7	C3+R	401	401	151	151	101	101	151	151	clk1_mode7
dcd_op_44	C3+R	854	807	86	80	379	373	80	80	dcd_op_44
ru_write_in_iq	C3+R	672	715	147	159	227	218	80	80	
ru_write_in_iq										
a_clk	C3+R	401	401	151	151	101	101	151	151	a_clk
b_clk	C3+R	401	401	151	151	101	101	151	151	b_clk
ru_iu_rcvy_rst	C3+R	700	700	151	151	999000	999000	151	151	
ru_iu_rcvy_rst										
eu_iu_enter_slow_md	C3+R	837	816	352	346	270	258	80	80	
eu_iu_enter_slow_md										
id_instr_stores	C3+R	1149	1163	176	100	430	406	129	80	
id_instr_stores										
op_inq_stores	C3+R	386	384	112	108	210	212	80	80	
op_inq_stores										
test_c1	C3+R	401	401	151	151	101	101	151	151	test_c1
iq_blk_aa	C3+R	518	532	105	91	279	276	80	80	iq_blk_aa
aa_ofc_available	C3+R	403	400	119	119	210	207	80	80	
aa_ofc_available										
eu_iu_mmode	C3+R	693	667	326	326	327	304	80	80	
eu_iu_mmode										
eu_iu_mcset_e1	C3+R	843	778	248	248	313	298	80	80	
eu_iu_mcset_e1										
aa_ofc_hold	C3+R	415	371	149	91	218	199	80	80	aa_ofc_hold
ru_98_43	C3+R	428	421	80	80	243	240	80	80	ru_98_43
srlz_op_match	C3+R	1281	1274	80	80	367	355	80	80	
srlz_op_match										
first_op_lat	C3+R	452	452	115	84	247	254	80	80	first_op_lat
zero_branches	C3+R	556	537	80	80	314	304	80	80	
ZERO_BRANCHES										
dcd_mcr41_blk	C3+R	850	835	80	80	314	311	80	80	
dcd_mcr41_blk										
xu_iu_xlat_busy	C3+R	817	863	193	193	368	360	80	80	
xu_iu_xlat_busy										
du_iu_hold_aa_req	C3+R	558	557	424	424	243	246	80	80	
du_iu_hold_aa_req										
eu_iu_fpu_end_op	C3+R	669	615	339	338	283	274	80	80	
eu_iu_fpu_end_op										
eu_iu_misc_hold	C3+R	499	460	332	310	210	201	80	80	
eu_iu_misc_hold										
op_cmp_raw	C3+R	858	818	80	80	354	362	80	80	
op_cmp_raw										
op_dsbl_before	C3+R	755	728	80	80	407	394	80	80	
op_dsbl_before										
op_drain	C3+R	852	809	82	80	379	332	134	102	op_drain
eu_iu_fxu_end_op	C3+R	672	651	286	281	276	280	80	80	
eu_iu_fxu_end_op										
op_mcend_raw	C3+R	850	810	91	85	369	372	80	80	
op_mcend_raw										
eu_iu_br_wrong	C3+R	911	903	264	264	340	320	80	80	
eu_iu_br_wrong										

need_opnd_req	C3+R	384	368	80	80	219	209	80	80
need_opnd_req	C3+R	1358	1386	84	84	376	380	80	80 legal_bht_br
legal_bht_br	C3-	600	0	160	160	600	0	160	160 clkg
clkg	C3+R	401	401	151	151	101	101	151	151
bht_branch_req	C3+R	1291	1371	123	92	450	475	80	80
bht_branch_req	C3+R	537	521	338	338	244	227	80	80
id_ex_in_mm	C3+R	835	809	80	80	350	366	80	80
id_ex_in_mm	C3+R	829	802	80	80	345	362	80	80
du_iu_quiesced	C3+R	814	787	80	80	336	357	80	80
du_iu_quiesced	C3+R	808	780	80	80	335	355	80	80
iu_op_cmp_hit_a	C3+R	1157	1158	80	80	370	395	80	80 dcd_frc_milli
iu_op_cmp_hit_a	C3+R	637	608	116	108	307	296	80	80 iq_empty
iu_op_cmp_hit_b	C3+R	802	756	80	80	372	363	80	80 op_serialize
iu_op_cmp_hit_b	C3+R	401	401	151	151	101	101	151	151
iu_op_cmp_hit_c	C3+R	404	401	121	115	223	225	80	80 aa_agi_lat
iu_op_cmp_hit_c	C3+R	386	385	118	113	210	211	80	80
iu_op_cmp_hit_d	C3+R	366	358	80	80	204	199	80	80 ru_9a_52
dcd_frc_milli	C3+R	664	644	236	236	280	261	80	80
iq_empty	C3+R	868	829	80	80	381	359	80	80
op_serialize	C3+R	1202	1217	82	80	331	366	80	80
gptr_scan_in	C3+R	714	687	80	80	293	295	80	80
gptr_scan_in	C3+R	401	401	151	151	101	101	151	151
aa_agi_lat	C3+R	757	727	271	262	301	272	80	80
branch_request	C3+R	405	402	129	129	211	210	80	80
branch_request	C3+R	537	512	183	183	269	251	80	80
ru_9a_52	C3+R	506	520	114	114	280	292	80	80
bu_iu_quiesced	C3+R	780	740	184	184	348	339	80	80 ru_iu_rq_blk
bu_iu_quiesced	C3+R	800	773	80	80	366	351	80	80
dcd_blk_dsucc	C3+R	779	799	105	117	275	278	80	80 ireg_valid
dcd_blk_dsucc	C3+R	371	363	81	81	204	199	80	80 ru_9a_36
op_eim_dcd	C3+R	583	598	110	81	302	284	86	80
op_eim_dcd	C3+R	401	401	151	151	101	101	151	151
iqmcode_mod_390gr	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
iqmcode_mod_390gr	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
scan_in	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
scan_invec(0)	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
eu_iu_e1_exc_cond	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
eu_iu_e1_exc_cond	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
aa_ofc_block_req	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
aa_ofc_block_req	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
eu_iu_fpu_excprn	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
eu_iu_fpu_excprn	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
block_aa_branch	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
block_aa_branch	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
ru_iu_rq_blk	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
op_chkpt_synch	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
op_chkpt_synch	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
ireg_valid	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
ru_9a_36	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
three_branches	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
three_branches	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
bht_block_dcd	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
bht_block_dcd	C3+R	369	362	80	80	204	199	80	80 ru_9a_20
ru_9a_20	C3+R	369	362	80	80	204	199	80	80 ru_9a_20

iu_eu_data_blocked	C3+R	410	406	125	123	223	224	80	80
iu_eu_data_blocked									
gptra_a_clk	C3+R	401	401	151	151	101	101	151	151 gptra_a_clk
gptra_b_clk	C3+R	401	401	151	151	101	101	151	151 gptra_b_clk
op_is_44	C3+R	989	939	105	80	507	475	98	80 op_is_44
inst_fetches	C3+R	1207	1306	80	80	406	423	80	80 inst_fetches
clk2	C3-	600	0	160	160	600	0	160	160 clk2
eu_iu_fxu_exc_cond	C3+R	988	953	390	390	371	354	80	80
eu_iu_fxu_exc_cond									
ru_9a_04	C3+R	379	372	82	82	204	198	80	80 ru_9a_04
br_wrong_targ	C3+R	1171	1099	175	82	362	349	100	80
br_wrong_targ									
scan_enable	C3+R	1045	1039	86	81	999172	999172	80	80
scan_enable									
du_iu_store_status(0)	C3+R	541	508	289	289	252	231	80	80
du_iu_store_status(0)									
du_iu_store_status(1)	C3+R	527	507	276	276	246	233	80	80
du_iu_store_status(1)									
du_iu_store_status(2)	C3+R	691	649	500	500	256	236	500	500
du_iu_store_status(2)									
eu_iu_srlz_op_actn(0)	C3+R	544	557	366	374	225	218	80	80
eu_iu_srlz_op_actn(0)									
eu_iu_srlz_op_actn(1)	C3+R	1344	1348	341	341	267	249	80	80
eu_iu_srlz_op_actn(1)									
ru_9a_0001(0)	C3+R	387	381	86	86	207	203	80	80
ru_9a_0001(0)									
ru_9a_0001(1)	C3+R	387	381	86	86	207	202	80	80
ru_9a_0001(1)									
ireg_0_1(0)	C3+R	440	428	172	172	236	229	80	80 ireg_0_1(0)
ireg_0_1(1)	C3+R	440	428	177	177	236	230	80	80 ireg_0_1(1)
num_dcd_cyl(0)	C3+R	1040	1088	80	80	414	453	80	84
num_dcd_cyl(0)									
num_dcd_cyl(1)	C3+R	1024	1016	80	80	399	387	80	80
num_dcd_cyl(1)									
ru_9a_3233(32)	C3+R	373	365	81	81	207	203	80	80
ru_9a_3233(32)									
ru_9a_3233(33)	C3+R	375	366	81	81	208	203	80	80
ru_9a_3233(33)									
eu_iu_interrupt_info(0)	C3+R	1260	1237	142	142	404	366	80	80
eu_iu_interrupt_info(0)									
eu_iu_interrupt_info(1)	C3+R	1256	1212	146	146	411	359	80	80
eu_iu_interrupt_info(1)									
eu_iu_interrupt_info(2)	C3+R	1226	1257	152	152	426	423	80	80
eu_iu_interrupt_info(2)									
eu_iu_interrupt_info(3)	C3+R	1210	1153	177	177	357	333	80	80
eu_iu_interrupt_info(3)									
ru_9a_1617(16)	C3+R	382	376	83	83	207	202	80	80
ru_9a_1617(16)									
ru_9a_1617(17)	C3+R	378	372	81	81	208	203	80	80
ru_9a_1617(17)									
eu_iu_srlz_op_encode(0)	C3+R	1086	1042	401	401	287	272	80	80
eu_iu_srlz_op_encode(0)									
eu_iu_srlz_op_encode(1)	C3+R	1091	1045	400	399	287	272	80	80
eu_iu_srlz_op_encode(1)									
eu_iu_srlz_op_encode(2)	C3+R	1094	1049	420	420	287	273	80	80

eu_iu_srlz_op_encode(2)									
eu_iu_srlz_op_encode(3)	C3+R	1066	1020	302	295	287	271	80	80
eu_iu_srlz_op_encode(3)									
eu_iu_srlz_op_encode(4)	C3+R	1051	1048	406	405	270	261	80	80
eu_iu_srlz_op_encode(4)									
eu_iu_srlz_op_encode(5)	C3+R	906	933	373	373	270	271	80	80
eu_iu_srlz_op_encode(5)									
eu_iu_srlz_op_encode(6)	C3+R	923	930	354	336	267	269	80	80
eu_iu_srlz_op_encode(6)									
eu_iu_srlz_op_encode(7)	C3+R	919	940	398	395	267	269	80	80
eu_iu_srlz_op_encode(7)									
eu_iu_srlz_op_encode(8)	C3+R	1051	1018	367	367	277	266	80	80
eu_iu_srlz_op_encode(8)									
eu_iu_srlz_op_encode(9)	C3+R	919	847	323	319	287	272	80	80
eu_iu_srlz_op_encode(9)									
eu_iu_srlz_op_encode(10)	C3+R	891	894	246	223	267	269	80	80
eu_iu_srlz_op_encode(10)									
eu_iu_srlz_op_encode(11)	C3+R	1102	1082	500	500	278	258	500	500
eu_iu_srlz_op_encode(11)									
ru_9a_4849(48)	C3+R	370	362	80	80	208	203	80	80
ru_9a_4849(48)									
ru_9a_4849(49)	C3+R	370	363	80	80	208	203	80	80
ru_9a_4849(49)									
ireg_1631(22)	C3+R	423	412	129	129	229	222	80	80
ireg_1631(22)									
ireg_1631(23)	C3+R	410	400	101	101	224	218	80	80
ireg_1631(23)									
ireg_1631(24)	C3+R	422	411	127	127	228	222	80	80
ireg_1631(24)									
ireg_1631(25)	C3+R	422	411	126	126	224	217	80	80
ireg_1631(25)									
ireg_1631(26)	C3+R	427	416	133	133	230	223	80	80
ireg_1631(26)									
ireg_1631(27)	C3+R	420	410	118	118	230	224	80	80
ireg_1631(27)									
ireg_1631(28)	C3+R	436	421	140	134	244	237	90	80
ireg_1631(28)									
ireg_1631(29)	C3+R	436	422	141	138	243	236	88	80
ireg_1631(29)									
ireg_1631(30)	C3+R	439	423	144	134	245	239	93	80
ireg_1631(30)									

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Part: IDCDSUC

Analysis: Late and Early / Nominal

EDA EinsTimer Design Information

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Release Level: 03.01

*** POs and Asserted Required Arrival Times and CAP data ***

Pin	Phase	RATr(L)	RATf(L)	RATr(E)	RATf(E)	Cap	Signal/Net
<hr/>							
iu_eu_opcode_cmp	C3+R	1060	1143	238	235	1170	N36
iu_rcvry_reset	C3+R	1060	1085	218	199	1099	N158
iu_reset_op_c	C3+R	587	559	197	183	1209	iu_reset_op_c

dcd_succ_last_t1	C3+R	999	999	-999	-999	1001	dcd_succ_last_t1
iu_milli_mode	C3+R	400	400	126	125	633	N12
iu_reset_op_c_t1	C3+R	999	999	-999	-999	1001	iu_reset_op_c_t1
dcd_succ_last	C3+R	929	879	224	229	964	N2086
iu_eu_op_nomatch	C3+R	835	835	84	69	1208	N26
ds_1st_maybe	C3+R	866	897	205	198	411	ds_1st_maybe
id_xcute_targ	C3+R	470	400	243	246	434	N34
xc_frc_ia_to_if_t1	C3+R	400	400	101	142	365	N14
dcd_success_tr	C3+R	1060	1060	-999160	-999129	531	N2097
dsucc_or_agi_n	C3+R	1060	1081	230	237	786	dsucc_or_agi_n
dsucc_or_agi	C3+R	1006	976	197	192	441	dsucc_or_agi
iu_slow_mode	C3+R	468	443	182	175	538	N0
slwmd_blk_n	C3+R	1060	1038	131	139	258	slwmd_blk_n
xc_frc_milli	C3+R	569	516	114	102	192	N16
dcd_succ_first_t1	C3+R	1060	1067	198	207	344	dcd_succ_first_t1
iu_reset_all	C3+R	980	924	202	188	746	iu_reset_all
iu_milli_mode_t1	C3+R	400	400	33	63	314	N2089
iu_milli_mode_t2	C3+R	1060	1142	181	169	288	N72
iu_milli_mode_t3	C3+R	708	644	235	228	632	N2090
xc_frc_milli_t1	C3+R	400	400	104	96	300	N42
iu_exc_cond	C3+R	1060	1223	221	203	208	N2096
slow_mode_tr	C3+R	1060	1060	-999089	-999055	570	N80
iu_eu_slow_mode	C3+R	1060	1117	238	235	1195	N22
dcd_success	C3+R	1016	1030	234	228	1112	dcd_success
iu_milli_mode_tr	C3+R	596	548	83	94	537	N70
iu_reset_if	C3+R	557	628	124	121	206	N140
exc_cond_tr	C3+R	1060	1060	-999070	-999051	570	N78
dcd_succ_first	C3+R	816	805	184	187	406	N2088
execute_recovery	C3+R	630	594	207	184	278	N136
execute_xcptn	C3+R	1060	1225	185	195	89	execute_xcptn
xc_frc_ia_to_if	C3+R	763	732	174	149	437	N8
iu_slow_mode_t1	C3+R	999	999	-999	-999	1001	N18
gptr_scan_out	C3+R	999	999	-999	-999	1000	gptr_scan_out&1
iu_reset_fst	C3+R	400	400	187	180	218	N4
scan_out	C3+R	999	999	-999	-999	106	scan_out
iu_eu_dcd_succ_tr	C3+R	843	769	80	52	1160	N134
idcdsuc_err	C3+R	999	999	-999	-999	1001	N146
frc_milli	C3+R	400	400	134	108	643	N10
iu_intrupt_info(0)	C3+R	1060	1020	135	131	105	N2092
iu_intrupt_info(1)	C3+R	942	888	68	49	94	N2093
iu_intrupt_info(2)	C3+R	1060	1024	134	133	105	N2094
iu_intrupt_info(3)	C3+R	1060	1016	131	132	105	N2095
blk_dcd_info_tr(0)	C3+R	1060	1060	-999153	-999134	543	N126
blk_dcd_info_tr(1)	C3+R	1060	1060	-999153	-999134	543	N128
blk_dcd_info_tr(2)	C3+R	1060	1060	-999150	-999135	543	N130
blk_dcd_info_tr(3)	C3+R	1060	1060	-999153	-999133	544	N132
iu_srlz_op_encode(0)	C3+R	734	746	14	-4	132	N44
iu_srlz_op_encode(1)	C3+R	688	652	-11	-17	132	N46
iu_srlz_op_encode(2)	C3+R	677	679	-19	-14	141	N48
iu_srlz_op_encode(3)	C3+R	765	759	7	1	98	N50
iu_srlz_op_encode(4)	C3+R	812	806	28	19	141	N52
iu_srlz_op_encode(5)	C3+R	646	645	15	6	145	N54
iu_srlz_op_encode(6)	C3+R	789	760	28	9	101	N56
iu_srlz_op_encode(7)	C3+R	789	784	31	16	141	N58
iu_srlz_op_encode(8)	C3+R	799	786	19	12	98	N60

iu_srlz_op_encode(9)	C3+R	736	681	50	22	153 N62
iu_srlz_op_encode(10)	C3+R	789	783	18	11	98 N64
iu_srlz_op_encode(11)	C3+R	795	785	12	11	98 N66
decode_iloc(0)	C3+R	476	504	38	29	356 N90
decode_iloc(1)	C3+R	458	489	52	39	404 N92
srlz_actn_tr(0)	C3+R	1060	1060	-999075	-999050	570 N30
srlz_actn_tr(1)	C3+R	1060	1060	-999075	-999050	542 N32
intrpt_info_tr(0)	C3+R	1060	1060	-999062	-999062	540 N104
intrpt_info_tr(1)	C3+R	1060	1060	-999066	-999058	568 N106
intrpt_info_tr(2)	C3+R	1060	1060	-999071	-999055	570 N108
intrpt_info_tr(3)	C3+R	1060	1060	-999071	-999055	568 N110
op_44_info_tr(0)	C3+R	626	481	98	71	552 N154
op_44_info_tr(1)	C3+R	624	548	96	93	539 N156
dcd_c_cnt(0)	C3+R	400	400	129	125	571 N148
dcd_c_cnt(1)	C3+R	400	400	140	126	601 N150

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Part: IDCDSUC

Analysis: Late and Early / Nominal

EDA EinsTimer Design Information

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

*** Don't Care, Data Adjust, Clock Adjust, Renamed Phase Tags ***

Pin Name Signal/Net	DC AdjR	DC AdjF Phs	NewPhs	DC AdjR	DC AdjF Phs	NewPhs
slow_mode.clockblock/c1	-	*	C3-	-	*	C3-
slow_mode.clockblock/c2	-	*	C3+	-	*	C3+
slow_mode.clockblock_1/c1	-	*	C3-	-	*	C3-
slow_mode.c1_2	-	*	C3+	-	*	C3+
slow_mode.clockblock_1/c2	-	*	C3+	-	*	C3+
slow_mode.c2_2	-	*	C3-	-	*	C3-
slow_mode.clockblock_2/c1	-	*	C3-	-	*	C3-
slow_mode.c1_3	-	*	C3+	-	*	C3+
slow_mode.clockblock_2/c2	-	*	C3+	-	*	C3+
slow_mode.c2_3	-	*	C3-	-	*	C3-
slow_mode.clockblock_3/c1	-	*	C3-	-	*	C3-
slow_mode.c1_4	-	*	C3+	-	*	C3+
slow_mode.clockblock_3/c2	-	*	C3+	-	*	C3+
slow_mode.c2_4	-	*	C3-	-	*	C3-
slow_mode.clockblock_4/c1	-	*	C3-	-	*	C3-
slow_mode.c1_5	-	*	C3+	-	*	C3+
slow_mode.clockblock_4/c2	-	*	C3+	-	*	C3+
slow_mode.c2_5	-	*	C3-	-	*	C3-
slow_mode.clockblock_5/c1	-	*	C3-	-	*	C3-
slow_mode.clockblock_5/c2	-	*	C3+	-	*	C3+
						slow_mode.c1
						slow_mode.c2

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Part: IDCDSUC

Analysis: Late and Early / Nominal

EDA EinsTimer Design Information

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Release Level: 03.01

*** User Selected Modes ***

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Part: IDCDSUC

Analysis: Late and Early / Nominal

EDA EinsTimer Design Information

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Release Level: 03.01

*** User Defined Tests ***

Mode	Pin1	Edge1	Pin2	Edge2	BC	Norm
WC						

***** EinsTimer Parameters *****

calculator.detail-calculator:	CDC
calculator.failure-calc:	NOPATH
calculator.tib-k1-term:	1E-09
calculator.tib-k2-term:	1E-10
calculator.tib-k3-term:	0
cdc-flags.include-output-caps:	FALSE
defaults.at-default:	0
defaults.clock-gating-hold-time:	0
defaults.clock-gating-mode:	input-to-input
defaults.clock-gating-pulse-width-time:	0
defaults.clock-gating-setup-time:	0
defaults.rat-default:	4E-09
defaults.rat-default-early:	2E-06
defaults.rat-default-late:	2E-06
defaults.slew-fall-default:	1.51E-07
defaults.slew-rise-default:	1.51E-07
delaymode.delay-mode:	Nominal
delaymode.lcd-best-early-value:	0
delaymode.lcd-best-late-value:	0
delaymode.lcd-nominal-early-value:	0
delaymode.lcd-nominal-late-value:	0
delaymode.lcd-pw-correction:	0
delaymode.lcd-worst-early-value:	1
delaymode.lcd-worst-late-value:	1
limits.global-cap-limit:	0
limits.global-slew-limit:	4.55E-07
limits.use-global-cap-limit:	FALSE
limits.use-global-slew-limit:	TRUE
misc.bus-delimiter:	()
misc.cache-limit:	10000
misc.debug-level:	0
misc.default-delimiter:	/
misc.em_data_mult:	1
misc.frequency:	0
misc.message-suppress:	610
misc.no-loop-message:	FALSE
netcalc.cap-mode-external:	TRUE
netcalc.net-delay-mode:	no-rcest

```

netcalc.pin-to-pin-net-model:    FALSE
pd.incremental-pi-model:         FALSE
process.best-case-temp:         -10
process.best-case-vdd:          1.7
process.best-case-vtt:          0
process.nominal-case-temp:       10
process.nominal-case-vdd:       1.45
process.nominal-case-vtt:       0
process.use-default-temp:        FALSE
process.use-default-vdd:         FALSE
process.use-default-vtt:        TRUE
process.worst-case-temp:         10
process.worst-case-vdd:         1.45
process.worst-case-vtt:         0
report.decimal-places:          0
rice.c-mult-bc:                 1
rice.c-mult-nom:                 1
rice.c-mult-wc:                 1
rice.r-mult-bc:                 1
rice.r-mult-nom:                 1
rice.r-mult-wc:                 1
rice.rice-order:                3
timer.clock-limiting:            TRUE
timer.domino-phase-creation:     FALSE
timer.dta-adjust-mode:           EdgeBased
timer.flush-propagate-on-dc-clock: TRUE
timer.perform-hold-tests:        TRUE
timer.slew-dependency:           path-slew
> checkfan

```

Electrical Violations in Network 'IDCDSUC'

Fanout		Capacitance	Slew	Sink
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual	
eu_iu_enter_slow_md	-> eu_iu_enter_slow_md	141.00 / 141.00 / 16.73	290.00	
12 / 290.00 / 352.00 *	12 / 12 / 1 1			
op_inq_stores	-> op_inq_stores	141.00 / 141.00 / 159.72 *	290.00 /	
12 / 290.00 / 112.00	12 / 12 / 3 1			
eu_iu_mmode	-> eu_iu_mmode	141.00 / 141.00 / 32.56	290.00 /	
12 / 290.00 / 326.00 *	12 / 12 / 2 1			
du_iu_hold_aa_req	-> du_iu_hold_aa_req	141.00 / 141.00 / 141.99 *	290.00	
12 / 290.00 / 424.00 *	12 / 12 / 2 1			
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	141.00 / 141.00 / 30.80	290.00 /	
12 / 290.00 / 339.00 *	12 / 12 / 1 1			
eu_iu_misc_hold	-> eu_iu_misc_hold	141.00 / 141.00 / 19.15	290.00 /	
12 / 290.00 / 332.00 *	12 / 12 / 1 1			
op_mcend_raw	-> op_mcend_raw	141.00 / 141.00 / 144.35 *	290.00 /	
12 / 290.00 / 91.00	12 / 12 / 3 1			
clkg	-> clkg	141.00 / 141.00 / 145.52 *	100.00 / 100.00 /	
12 / 60.00	12 / 12 / 3 1			
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 20.50	290.00 /	
12 / 290.00 / 338.00 *	12 / 12 / 1 1			
iq_empty	-> iq_empty	141.00 / 141.00 / 170.11 *	290.00 / 290.00	

```

/116.00    12/ 12/ 4 1
gptr_scan_in      -> gptr_scan_in      141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00    12/ 12/ 1 1
gptr_a_clk        -> gptr_a_clk        141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00    12/ 12/ 1 1
gptr_b_clk        -> gptr_b_clk        141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00    12/ 12/ 1 1
clk2             -> clk2             141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00    12/ 12/ 3 1
eu_iu_fxu_exc_cond      -> eu_iu_fxu_exc_cond      141.00 / 141.00 / 15.67 290.00
/ 290.00 / 390.00 * 12/ 12/ 1 1
du_iu_store_status(2)    -> du_iu_store_status(2)    141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 * 12/ 12/ 1 1
eu_iu_srlz_op_actn(0)    -> eu_iu_srlz_op_actn(0)    141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 * 12/ 12/ 2 1
eu_iu_srlz_op_actn(1)    -> eu_iu_srlz_op_actn(1)    141.00 / 141.00 / 47.57 290.00 /
290.00 / 341.00 * 12/ 12/ 2 1
num_dcd_cyl(1)         -> num_dcd_cyl(1)         141.00 / 141.00 / 318.91 * 290.00 /
290.00 / 80.00    12/ 12/ 1 1
eu_iu_srlz_op_encode(0)  -> eu_iu_srlz_op_encode(0)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(1)  -> eu_iu_srlz_op_encode(1)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(2)  -> eu_iu_srlz_op_encode(2)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(3)  -> eu_iu_srlz_op_encode(3)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(4)  -> eu_iu_srlz_op_encode(4)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 406.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(5)  -> eu_iu_srlz_op_encode(5)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(6)  -> eu_iu_srlz_op_encode(6)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(7)  -> eu_iu_srlz_op_encode(7)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(8)  -> eu_iu_srlz_op_encode(8)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 * 12/ 12/ 1 1

eu_iu_srlz_op_encode(9)  -> eu_iu_srlz_op_encode(9)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(11) -> eu_iu_srlz_op_encode(11)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 * 12/ 12/ 1 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1      78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00    12/ 12/ 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1      78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00    12/ 12/ 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1    78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59    12/ 12/ 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00    12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2      78.50 / 78.50 / 239.36 *

```

200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2 78.50 / 78.50 / 228.73 *
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_2:cb_clk_32 -> slow_mode.c1_3 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock_2:cb_clk_32 -> slow_mode.c2_3 78.50 / 78.50 / 239.37 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_3:cb_clk_32 -> slow_mode.c1_4 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL

Fanout	Capacitance	Slew	Sink
Pin/Port	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual
-> Net			
c2@slow_mode.clockblock_3:cb_clk_32 -> slow_mode.c2_4	78.50 / 78.50 / 239.36 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4	78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_4:cb_clk_32 -> slow_mode.c1_5	78.50 / 78.50 / 237.91 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_4:cb_clk_32 -> slow_mode.c2_5	78.50 / 78.50 / 239.37 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5	78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32 -> slow_mode.c1	78.50 / 78.50 / 237.92 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32 -> slow_mode.c2	78.50 / 78.50 / 239.37 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka	78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
y@C167:cs_invv01c -> dcd_succ_last_t1&0	70.00 / 70.00 / 1011.00 *	301.00	
/ 301.00 / 3294.02 * 12 / 12 / 1 1 KEEP_BTR			
y@C1994:cs_invvn01c -> N1531	68.00 / 68.00 / 77.40 *	290.00 /	
290.00 / 286.02 12 / 12 / 2 2			
y@C2013:cs_invvn01c -> N18&0	68.00 / 68.00 / 1011.00 *	301.00 /	
301.00 / 3608.92 * 12 / 12 / 1 1			
y@C2082:cs_invvn01c -> N146&0	68.00 / 68.00 / 1011.00 *	301.00 /	
301.00 / 3604.78 * 12 / 12 / 1 1			
y@C2194:cs_invvn07c -> N1681	261.00 / 261.00 / 271.46 *	290.00 /	

```

290.00 / 261.53      12 / 12 / 7 7
y@C2393:cs_nnd2v02c      -> iu_reset_op_c_t1&0      71.00 / 71.00 / 1044.40 *
290.00 / 290.00 / 3371.12 * 12 / 12 / 3 3
y@C2425:cs_invvn01c      -> N1815      68.00 / 68.00 / 125.56 * 290.00 /
290.00 / 451.90 * 12 / 12 / 1 1
y@C2496:cs_nnd4n03c      -> N1435      85.00 / 85.00 / 97.67 * 290.00 /
290.00 / 353.82 * 12 / 12 / 5 5
y@C2646:cs_invvn04c      -> N1645      133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 275.60      12 / 12 / 6 6
y@C2726:cs_nnd2n11c      -> dsucc_or_agi&0      500.00 / 500.00 / 540.60 *
290.00 / 290.00 / 258.01      12 / 12 / 2 2
y@C2744:cs_invvn13c      -> N2086&0      996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 271.62      12 / 12 / 7 7
y@C2800:cs_invvn08c      -> N1290      326.00 / 326.00 / 234.15      290.00 /
290.00 / 193.42      12 / 12 / 14 * 14
y@C2728rwr:cs_invvn05c      -> N1097      167.00 / 167.00 / 183.47 * 290.00 /
290.00 / 266.58      12 / 12 / 4 4
y@C2918:cs_nor2n04c      -> N2016      110.00 / 110.00 / 132.34 * 290.00 /
290.00 / 428.15 * 12 / 12 / 1 1
y@gbfocell_0:cs_invvn12c      -> gbfonet_0      797.00 / 797.00 / 402.55      290.00 /
290.00 / 149.98      12 / 12 / 20 * 20
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q      247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45      12 / 12 / 8 8

```

[BD-500900]: (W) There were 64 electrical violations.

> write_info_report

[ET-0018]: >Begin...Info Report
for file /tmp/info_report..92476.

[ET-0019]: <End.....Info Report.

Sun Apr 18 22:09:40 1999

Part : IDCDSUC

Mode : Late and Early Mode / Nominal EDA EinsTimer Info Report

Release Level : 03.01 and Compile Date : Wed Mar 24 22:00:23 1999

***** CAPACITANCE VIOLATIONS *****

Pin	Cell	Power	Over (+%)/ Cap Limit		Signal/ Under(-%) Source	Net
C2744/y	cs_invvn	13c	1081	996	9 N2086&0	
C2393/y	cs_nnd2v	02c	1044	71	1371 iu_reset_op_c_t1&0	
gp_tr_b_clk			1011	141	617 gp_tr_b_clk	
gp_tr_a_clk			1011	141	617 gp_tr_a_clk	
gp_tr_scan_in			1011	141	617 gp_tr_scan_in	
BOX750/OUT	IOPAD		1011	68	1387 N146	
BOX745/OUT	IOPAD		1011	68	1387 N18	
BOX716/OUT	IOPAD		1011	25	4025 iu_reset_op_c_t1	
BOX714/OUT	IOPAD		1011	70	1344 dcd_succ_last_t1	
BOX661/OUT	IOPAD		1011	141	617 gp_tr_b_clk&0	
BOX660/OUT	IOPAD		1011	141	617 gp_tr_a_clk&0	
BOX639/OUT	IOPAD		1011	141	617 gp_tr_scan_in&0	
C2082/y	cs_invvn	01c	1011	68	1387 N146&0	
C2013/y	cs_invvn	01c	1011	68	1387 N18&0	
C167/y	cs_invvn	01c	1011	70	1344 dcd_succ_last_t1&0	
BOX746/OUT	IOPAD		1010	0	0 gp_tr_scan_out&1	

gptr_latch/gptr_scan_out	XMODEBLOCK A	1010	0	0	gptr_scan_out&0
BOX717/OUT	IOPAD	974	848	15	N2086
C2726/y	cs_nnd2n 11c	541	500	8	dsucc_or_agi&0
BOX724/OUT	IOPAD	451	396	14	dsucc_or_agi
num_dcd_cyl(1)		319	141	126	num_dcd_cyl(1)
BOX679/OUT	IOPAD	319	141	126	num_dcd_cyl&0(1)
frc_blk_1cyc.reg_n.lat_0/12_out_n	cl_nnd2n 07c	302	247	22	frc_blk_1cyc_q
C2194/y	cs_invvn 07c	271	261	4	N1681
slow_mode.clockblock_4/c2	cb_clk_32_1	239	78	205	slow_mode.c2_5
slow_mode.clockblock_2/c2	cb_clk_32_1	239	78	205	slow_mode.c2_3
slow_mode.clockblock_5/c2	cb_clk_32_1	239	78	205	slow_mode.c2
slow_mode.clockblock_1/c2	cb_clk_32_1	239	78	205	slow_mode.c2_2
slow_mode.clockblock_3/c2	cb_clk_32_1	239	78	205	slow_mode.c2_4
slow_mode.clockblock_3/c1	cb_clk_32_1	238	78	203	slow_mode.c1_4
slow_mode.clockblock_5/c1	cb_clk_32_1	238	78	203	slow_mode.c1
slow_mode.clockblock_1/c1	cb_clk_32_1	238	78	203	slow_mode.c1_2
slow_mode.clockblock_2/c1	cb_clk_32_1	238	78	203	slow_mode.c1_3
slow_mode.clockblock_4/c1	cb_clk_32_1	238	78	203	slow_mode.c1_5
slow_mode.clockblock_4/clka	cb_clk_32_1	229	78	191	slow_mode.clka_5
slow_mode.clockblock_3/clka	cb_clk_32_1	229	78	191	slow_mode.clka_4
slow_mode.clockblock_1/clka	cb_clk_32_1	229	78	191	slow_mode.clka_2
slow_mode.clockblock_5/clka	cb_clk_32_1	229	78	191	slow_mode.clka
slow_mode.clockblock_2/clka	cb_clk_32_1	229	78	191	slow_mode.clka_3
slow_mode.clockblock/c2	cb_clk_32_1	222	78	183	slow_mode.c2_1
slow_mode.clockblock/c1	cb_clk_32_1	221	78	181	slow_mode.c1_1
slow_mode.clockblock/clka	cb_clk_32_1	212	78	171	slow_mode.clka_1
C2728rwr/y	cs_invvn 05c	183	167	10	N1097
iq_empty		170	141	21	iq_empty
BOX637/OUT	IOPAD	170	141	21	iq_empty&0
op_inq_stores		160	141	13	op_inq_stores
BOX604/OUT	IOPAD	160	141	13	op_inq_stores&0
C2646/y	cs_invvn 04c	151	133	13	N1645
clk2		146	141	3	clk2
clk		146	141	3	clk
BOX664/OUT	IOPAD	146	141	3	clk2&0
BOX628/OUT	IOPAD	146	141	3	clk&0
op_mcend_raw		144	141	2	op_mcend_raw
BOX624/OUT	IOPAD	144	141	2	op_mcend_raw&0
du_iu_hold_aa_req		142	141	1	du_iu_hold_aa_req
BOX617/OUT	IOPAD	142	141	1	du_iu_hold_aa_req&0
C2918/y	cs_nor2n 04c	132	110	20	N2016
gptr_latch/clkl_mode8	XMODEBLOCK A	128	0	0	clkl_mode8
C2425/y	cs_invvn 01c	126	68	85	N1815
gptr_latch/clkl_mode5	XMODEBLOCK A	103	0	0	clkl_mode5_0
gptr_latch/clkl_mode4	XMODEBLOCK A	99	0	0	clkl_mode4_0
C2496/y	cs_nnd4n 03c	98	85	15	N1435
gptr_latch/clkl_mode6	XMODEBLOCK A	96	0	0	clkl_mode6_0
C1994/y	cs_invvn 01c	77	68	14	N1531
iu_dsbl_ovrlp.reg_n.lat_0/12_out_n	cl_nor2n 06c	16	16	-2	iu_dsbl_ovrlp_q
dsbl_ovrlp_blk.reg_n.lat_0/12_out_n	cl_nnd2n 07c	16	16	-2	dsbl_ovrlp_blk_q
bht_block.reg_n.lat_0/12_out_n	cl_invvn 07d	16	16	-2	bht_block_q
slow_mode.t1.reg_n.lat_0/12_out_n	cl_invvn 07c	16	16	-2	slow_mode.t1_q
eu_iu_spare.reg_n.lat_0/12_out_n	cl_invvn 07d	15	16	-6	eu_iu_spare_q

***** SLEW TIMES VIOLATIONS *****

Signal/ Pin Net	Cell	Power	Early/ Late	Edge	Over (+%)/ Slew Limit	- Driver - Under(-%)	Cell	Power Source
iu_slow_mode_t1			L	R	3609	301	1099 IOPAD	N18
iu_slow_mode_t1			E	R	3609	301	1099 IOPAD	N18
BOX745/IN	IOPAD		L	R	3609	455	693 cs_invvn	01c N18&0
BOX745/IN	IOPAD		E	R	3609	455	693 cs_invvn	01c N18&0
idcdsuc_err			L	R	3605	301	1098 IOPAD	N146
idcdsuc_err			E	R	3605	301	1098 IOPAD	N146
BOX750/IN	IOPAD		L	R	3605	455	692 cs_invvn	01c N146&0
BOX750/IN	IOPAD		E	R	3605	455	692 cs_invvn	01c N146&0
iu_reset_op_c_t1			E	R	3371	301	1020 IOPAD	
iu_reset_op_c_t1								
BOX716/IN	IOPAD		E	R	3371	455	641 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2555/b	cs_ao12n	03c	E	R	3371	290	1062 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2466/b	cs_nnd2n	02c	E	R	3371	290	1062 cs_nnd2v	02c
iu_reset_op_c_t1&0								
iu_reset_op_c_t1			L	R	3318	301	1002 IOPAD	
iu_reset_op_c_t1								
BOX716/IN	IOPAD		L	R	3318	455	629 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2555/b	cs_ao12n	03c	L	R	3318	290	1044 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2466/b	cs_nnd2n	02c	L	R	3318	290	1044 cs_nnd2v	02c
iu_reset_op_c_t1&0								
dcd_succ_last_t1			L	R	3294	301	994 IOPAD	
dcd_succ_last_t1								
dcd_succ_last_t1			E	R	3294	301	994 IOPAD	
dcd_succ_last_t1								
BOX714/IN	IOPAD		L	R	3294	455	624 cs_invvv	01c
dcd_succ_last_t1&0								
BOX714/IN	IOPAD		E	R	3294	455	624 cs_invvv	01c
dcd_succ_last_t1&0								
iu_reset_op_c_t1			L	F	2484	301	725 IOPAD	
iu_reset_op_c_t1								
BOX716/IN	IOPAD		L	F	2484	455	446 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2555/b	cs_ao12n	03c	L	F	2484	290	757 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2466/b	cs_nnd2n	02c	L	F	2484	290	757 cs_nnd2v	02c
iu_reset_op_c_t1&0								
iu_reset_op_c_t1			E	F	2177	301	623 IOPAD	
iu_reset_op_c_t1								
BOX716/IN	IOPAD		E	F	2177	455	378 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2555/b	cs_ao12n	03c	E	F	2177	290	651 cs_nnd2v	02c
iu_reset_op_c_t1&0								
C2466/b	cs_nnd2n	02c	E	F	2177	290	651 cs_nnd2v	02c

iu_reset_op_c_t1&0									
iu_slow_mode_t1			L	F	1973	301	555 IOPAD	N18	
iu_slow_mode_t1			E	F	1973	301	555 IOPAD	N18	
BOX745/IN	IOPAD		L	F	1973	455	334 cs_invv	01c	N18&0
BOX745/IN	IOPAD		E	F	1973	455	334 cs_invv	01c	N18&0
idcdsuc_err		L	F	1961	301	552 IOPAD		N146	
idcdsuc_err		E	F	1961	301	552 IOPAD		N146	
BOX750/IN	IOPAD		L	F	1961	455	331 cs_invv	01c	N146&0
BOX750/IN	IOPAD		E	F	1961	455	331 cs_invv	01c	N146&0
dcd_succ_last_t1		L	F	1874	301	523 IOPAD			
dcd_succ_last_t1									
BOX714/IN	IOPAD		L	F	1874	455	312 cs_invv	01c	
dcd_succ_last_t1&0									
BOX714/IN	IOPAD		E	F	1829	455	302 cs_invv	01c	
dcd_succ_last_t1&0									
dcd_succ_last_t1		E	F	1829	301	508 IOPAD			
dcd_succ_last_t1									
BOX699/IN	IOPAD		L	F	500	290	72		
eu_iu_srlz_op_encode(11)									
BOX699/IN	IOPAD		L	R	500	290	72		
eu_iu_srlz_op_encode(11)									
BOX699/IN	IOPAD		E	F	500	290	72		
eu_iu_srlz_op_encode(11)									
BOX699/IN	IOPAD		E	R	500	290	72		
eu_iu_srlz_op_encode(11)									
BOX671/IN	IOPAD		L	F	500	290	72		
du_iu_store_status(2)									
BOX671/IN	IOPAD		L	R	500	290	72		
du_iu_store_status(2)									
BOX671/IN	IOPAD		E	F	500	290	72		
du_iu_store_status(2)									
BOX671/IN	IOPAD		E	R	500	290	72		
du_iu_store_status(2)									
C2763/a	cs_nnd2n	02c	L	F	500	290	72 IOPAD		
du_iu_store_status&0(2)									
C2763/a	cs_nnd2n	02c	L	R	500	290	72 IOPAD		
du_iu_store_status&0(2)									
C2763/a	cs_nnd2n	02c	E	F	500	290	72 IOPAD		
du_iu_store_status&0(2)									
C2763/a	cs_nnd2n	02c	E	R	500	290	72 IOPAD		
du_iu_store_status&0(2)									
C2650/a	cs_nnd2n	02c	L	F	500	290	72 IOPAD		
eu_iu_srlz_op_encode&0(11)									
C2650/a	cs_nnd2n	02c	L	R	500	290	72 IOPAD		
eu_iu_srlz_op_encode&0(11)									
C2650/a	cs_nnd2n	02c	E	F	500	290	72 IOPAD		
eu_iu_srlz_op_encode&0(11)									
C2650/a	cs_nnd2n	02c	E	R	500	290	72 IOPAD		
eu_iu_srlz_op_encode&0(11)									
C2487/b	cs_nnd2x	14e	L	R	452	290	56 cs_invv	01c	N1815
C2487/b	cs_nnd2x	14e	E	R	448	290	55 cs_invv	01c	N1815
C2917/b	cs_nnd2x	14c	L	R	428	290	48 cs_nor2n	04c	N2016
BOX617/IN	IOPAD		L	F	424	290	46		
du_iu_hold_aa_req									
BOX617/IN	IOPAD		L	R	424	290	46		

du_iu_hold_aa_req									
bce_hold_aa.reg_n.lat_0/a	cl_invv	07d	L	F	424	290	46	IOPAD	
du_iu_hold_aa_req&0									
bce_hold_aa.reg_n.lat_0/a	cl_invv	07d	L	R	424	290	46	IOPAD	
du_iu_hold_aa_req&0									
C2020/a	cs_invv	14c	L	F	424	290	46	IOPAD	
du_iu_hold_aa_req&0									
C2020/a	cs_invv	14c	L	R	424	290	46	IOPAD	
du_iu_hold_aa_req&0									
C2917/b	cs_nnd2x	14c	E	R	423	290	46	cs_nor2n	04c N2016
BOX690/IN	IOPAD		L	F	420	290	45		
eu_iu_srlz_op_encode(2)									
BOX690/IN	IOPAD		L	R	420	290	45		
eu_iu_srlz_op_encode(2)									
C2665/a	cs_nnd2n	02c	L	F	420	290	45	IOPAD	
eu_iu_srlz_op_encode&0(2)									
C2665/a	cs_nnd2n	02c	L	R	420	290	45	IOPAD	
eu_iu_srlz_op_encode&0(2)									
BOX692/IN	IOPAD		L	R	406	290	40		
eu_iu_srlz_op_encode(4)									
C2657/a	cs_nnd2n	02c	L	R	406	290	40	IOPAD	
eu_iu_srlz_op_encode&0(4)									
BOX692/IN	IOPAD		L	F	405	290	40		
eu_iu_srlz_op_encode(4)									
C2657/a	cs_nnd2n	02c	L	F	405	290	40	IOPAD	
eu_iu_srlz_op_encode&0(4)									
BOX688/IN	IOPAD		L	F	401	290	38		
eu_iu_srlz_op_encode(0)									
BOX688/IN	IOPAD		L	R	401	290	38		
eu_iu_srlz_op_encode(0)									
C2667/a	cs_nnd2n	02c	L	F	401	290	38	IOPAD	
eu_iu_srlz_op_encode&0(0)									
C2667/a	cs_nnd2n	02c	L	R	401	290	38	IOPAD	
eu_iu_srlz_op_encode&0(0)									
BOX689/IN	IOPAD		L	R	400	290	38		
eu_iu_srlz_op_encode(1)									
C2666/a	cs_nnd2n	02c	L	R	400	290	38	IOPAD	
eu_iu_srlz_op_encode&0(1)									
BOX689/IN	IOPAD		L	F	399	290	38		
eu_iu_srlz_op_encode(1)									
C2666/a	cs_nnd2n	02c	L	F	399	290	38	IOPAD	
eu_iu_srlz_op_encode&0(1)									
BOX695/IN	IOPAD		L	R	398	290	37		
eu_iu_srlz_op_encode(7)									
C2659/a	cs_nnd2n	02c	L	R	398	290	37	IOPAD	
eu_iu_srlz_op_encode&0(7)									
BOX695/IN	IOPAD		L	F	395	290	36		
eu_iu_srlz_op_encode(7)									
C2659/a	cs_nnd2n	02c	L	F	395	290	36	IOPAD	
eu_iu_srlz_op_encode&0(7)									
BOX665/IN	IOPAD		L	F	390	290	34		
eu_iu_fxu_exc_cond									
BOX665/IN	IOPAD		L	R	390	290	34		
eu_iu_fxu_exc_cond									
C1928/a	cs_invv	01c	L	F	390	290	34	IOPAD	

eu_iu_fxu_exc_cond&0 C1928/a	cs_invvn	01c	L	R	390	290	34	IOPAD
eu_iu_fxu_exc_cond&0 BOX672/IN	IOPAD		L	F	374	290	29	
eu_iu_srlz_op_actn(0) srlz_actn.reg_n.lat_0/a eu_iu_srlz_op_actn&0(0)	cl_invvn	07d	L	F	374	290	29	IOPAD
C2651/a	cs_nnd2n	02c	L	F	374	290	29	IOPAD
eu_iu_srlz_op_actn&0(0) BOX693/IN	IOPAD		L	F	373	290	29	
eu_iu_srlz_op_encode(5) BOX693/IN	IOPAD		L	R	373	290	29	
eu_iu_srlz_op_encode(5) C2656/a	cs_nnd2n	02c	L	F	373	290	29	IOPAD
eu_iu_srlz_op_encode&0(5) C2656/a	cs_nnd2n	02c	L	R	373	290	29	IOPAD
eu_iu_srlz_op_encode&0(5) BOX696/IN	IOPAD		L	F	367	290	27	
eu_iu_srlz_op_encode(8) BOX696/IN	IOPAD		L	R	367	290	27	
eu_iu_srlz_op_encode(8) C2660/a	cs_nnd2n	02c	L	F	367	290	27	IOPAD
eu_iu_srlz_op_encode&0(8) C2660/a	cs_nnd2n	02c	L	R	367	290	27	IOPAD
eu_iu_srlz_op_encode&0(8) BOX672/IN	IOPAD		L	R	366	290	26	
eu_iu_srlz_op_actn(0) srlz_actn.reg_n.lat_0/a eu_iu_srlz_op_actn&0(0)	cl_invvn	07d	L	R	366	290	26	IOPAD
C2651/a	cs_nnd2n	02c	L	R	366	290	26	IOPAD
eu_iu_srlz_op_actn&0(0) BOX694/IN	IOPAD		L	R	354	290	22	
eu_iu_srlz_op_encode(6) C2658/a	cs_nnd2n	02c	L	R	354	290	22	IOPAD
eu_iu_srlz_op_encode&0(6) iu_dsbl_ovrlp.reg_n.lat_0/b N1435	cl_nor2n	06c	L	R	354	290	22	cs_nnd4n 03c
C2622/b	cs_nor2n	02c	L	R	354	290	22	cs_nnd4n 03c N1435
C2544/a	cs_invvn	01c	L	R	354	290	22	cs_nnd4n 03c N1435
C2543/b	cs_nnd2n	02c	L	R	354	290	22	cs_nnd4n 03c N1435
C2513/b	cs_nnd2n	02c	L	R	354	290	22	cs_nnd4n 03c N1435
BOX602/IN	IOPAD		L	R	352	290	21	
eu_iu_enter_slow_md C2107/b	cs_nnd2n	02c	L	R	352	290	21	IOPAD
eu_iu_enter_slow_md&0 BOX602/IN	IOPAD		L	F	346	290	19	
eu_iu_enter_slow_md C2107/b	cs_nnd2n	02c	L	F	346	290	19	IOPAD
eu_iu_enter_slow_md&0 BOX673/IN	IOPAD		L	F	341	290	18	
eu_iu_srlz_op_actn(1) BOX673/IN	IOPAD		L	R	341	290	18	
eu_iu_srlz_op_actn(1) srlz_actn.reg_n.lat_1/a eu_iu_srlz_op_actn&0(1)	cl_invvn	07d	L	F	341	290	18	IOPAD

BOX691/IN	IOPAD	L	R	302	290	4	
eu_iu_srlz_op_encode(3)							
C2664/a	cs_nnd2n	02c	L	R	302	290	4 IOPAD
eu_iu_srlz_op_encode&0(3)							
BOX691/IN	IOPAD	L	F	295	290	2	
eu_iu_srlz_op_encode(3)							
C2664/a	cs_nnd2n	02c	L	F	295	290	2 IOPAD
eu_iu_srlz_op_encode&0(3)							
BOX661/IN	IOPAD	L	F	151	0	0	gptr_b_clk
BOX661/IN	IOPAD	L	R	151	0	0	gptr_b_clk
BOX661/IN	IOPAD	E	F	151	0	0	gptr_b_clk
BOX661/IN	IOPAD	E	R	151	0	0	gptr_b_clk
BOX660/IN	IOPAD	L	F	151	0	0	gptr_a_clk
BOX660/IN	IOPAD	L	R	151	0	0	gptr_a_clk
BOX660/IN	IOPAD	E	F	151	0	0	gptr_a_clk
BOX660/IN	IOPAD	E	R	151	0	0	gptr_a_clk
BOX639/IN	IOPAD	L	F	151	0	0	gptr_scan_in
BOX639/IN	IOPAD	L	R	151	0	0	gptr_scan_in
BOX639/IN	IOPAD	E	F	151	0	0	gptr_scan_in
BOX639/IN	IOPAD	E	R	151	0	0	gptr_scan_in
gptr_latch/gptr_scan_in	XMODEBLOCK	A	L	F	151	0	0 IOPAD
gptr_scan_in&0							
gptr_latch/gptr_scan_in	XMODEBLOCK	A	L	R	151	0	0 IOPAD
gptr_scan_in&0							
gptr_latch/gptr_scan_in	XMODEBLOCK	A	E	F	151	0	0 IOPAD
gptr_scan_in&0							
gptr_latch/gptr_scan_in	XMODEBLOCK	A	E	R	151	0	0 IOPAD
gptr_scan_in&0							
gptr_latch/gptr_b_clk	XMODEBLOCK	A	L	F	151	0	0 IOPAD
gptr_b_clk&0							
gptr_latch/gptr_b_clk	XMODEBLOCK	A	L	R	151	0	0 IOPAD
gptr_b_clk&0							
gptr_latch/gptr_b_clk	XMODEBLOCK	A	E	F	151	0	0 IOPAD
gptr_b_clk&0							
gptr_latch/gptr_b_clk	XMODEBLOCK	A	E	R	151	0	0 IOPAD
gptr_b_clk&0							
gptr_latch/gptr_a_clk	XMODEBLOCK	A	L	F	151	0	0 IOPAD
gptr_a_clk&0							
gptr_latch/gptr_a_clk	XMODEBLOCK	A	L	R	151	0	0 IOPAD
gptr_a_clk&0							
gptr_latch/gptr_a_clk	XMODEBLOCK	A	E	F	151	0	0 IOPAD
gptr_a_clk&0							
gptr_latch/gptr_a_clk	XMODEBLOCK	A	E	R	151	0	0 IOPAD
gptr_a_clk&0							
C2890rwr/a	cs_invvv	10c	L	F	30	30	-1 cs_nnd2v 13c N2005
C2339/a	cs_nnd2v	13c	E	F	30	30	-1 cs_nnd2v 13c NET690
dcd_succ_disable_scan.reg_n.lat_1/a	cl_invvn	07d	L	F	30	30	-1 cs_invvn 07c
N2060							
dcd_succ_disable_scan.reg_n.lat_1/a	cl_invvn	07d	E	F	30	30	-1 cs_invvn 07c
N2060							
C2909/b	cs_nnd2x	14e	L	F	29	30	-2 cs_invvv 13c N2012
C2101/a	cs_nnd2n	04c	L	F	29	30	-2 cs_invvn 07c N1643
C2113/a	cs_nnd2n	04c	L	F	29	30	-3 cs_invvn 07c N1644
C2113/a	cs_nnd2n	04c	E	F	29	30	-3 cs_invvn 07c N1644
C2101/a	cs_nnd2n	04c	E	F	29	30	-3 cs_invvn 07c N1643

C2409/b	cs_nnd2n	04c	E	F	29	30	-3 cs_invvv	07c	N1707
C2212/b	cs_nnd2n	04c	E	F	29	30	-3 cs_invvv	07c	N139
blk_dcd.reg_n.lat_3/a1	cl_ao21n	07c	L	F	29	30	-4 cs_invvv	13b	N1119
blk_dcd.reg_n.lat_3/a1	cl_ao21n	07c	E	F	29	30	-4 cs_invvv	13b	N1119
C2509/b	cs_nor2n	02c	L	F	29	30	-4 cs_invvv	13b	N1119
C2509/b	cs_nor2n	02c	E	F	29	30	-4 cs_invvv	13b	N1119
C2338/a	cs_nnd2x	14c	L	F	29	30	-4 cs_invvv	13b	N1119
C2338/a	cs_nnd2x	14c	E	F	29	30	-4 cs_invvv	13b	N1119
C2889/b	cs_ao21n	10e	L	R	29	30	-4 cs_invvv	10c	N2000
C2890rwr/a	cs_invvv	10c	E	F	29	30	-5 cs_nnd2v	13c	N2005
C2889/b	cs_ao21n	10e	E	R	28	30	-5 cs_invvv	10c	N2000
C2284/b	cs_nnd3n	02c	L	F	28	30	-6 cs_invvv	07c	N1693
C2909/b	cs_nnd2x	14e	E	F	28	30	-6 cs_invvv	13c	N2012
C2187/b	cs_nnd2v	13c	E	F	28	30	-6 cs_invvv	14c	N29
C2744/a	cs_invvv	13c	L	F	27	30	-9 cs_nnd2x	14b	N675
C2744/a	cs_invvv	13c	E	F	27	30	-9 cs_nnd2x	14b	N675
C2743/b	cs_nnd2n	02c	L	F	27	30	-9 cs_nnd2x	14b	N675
C2743/b	cs_nnd2n	02c	E	F	27	30	-9 cs_nnd2x	14b	N675
C2742/b	cs_nnd2n	02c	L	F	27	30	-9 cs_nnd2x	14b	N675
C2742/b	cs_nnd2n	02c	E	F	27	30	-9 cs_nnd2x	14b	N675
C167/a	cs_invvv	01c	L	F	27	30	-9 cs_nnd2x	14b	N675
C167/a	cs_invvv	01c	E	F	27	30	-9 cs_nnd2x	14b	N675
C2269/b	cs_nnd3n	02c	L	F	27	30	-9 cs_invvv	07c	N1688
C2257/b	cs_nnd3n	02c	L	F	27	30	-9 cs_invvv	07c	N1686
C2321/b	cs_nnd3n	02c	L	E	27	30	-9 cs_invvv	07c	N1702
C2321/b	cs_nnd3n	02c	E	F	27	30	-9 cs_invvv	07c	N1702
C2284/b	cs_nnd3n	02c	E	F	27	30	-9 cs_invvv	07c	N1693
C2269/b	cs_nnd3n	02c	E	F	27	30	-9 cs_invvv	07c	N1688
C2257/b	cs_nnd3n	02c	E	F	27	30	-9 cs_invvv	07c	N1686
spare.reg_n.lat_0/a	cl_invvv	07d	L	F	27	30	-11 cs_invvv	07c	N2064
spare.reg_n.lat_0/a	cl_invvv	07d	E	F	27	30	-11 cs_invvv	07c	N2064
C2897/b	cs_ao12n	07c	L	F	26	30	-12 cs_invvv	07c	N2007
C2897/b	cs_ao12n	07c	E	F	26	30	-12 cs_invvv	07c	N2007
dcd_succ_disable_scan.reg_n.lat_2/a	cl_invvv	05d	L	F	26	30	-13 cs_invvv	07c	N2062
dcd_succ_disable_scan.reg_n.lat_2/a	cl_invvv	05d	E	F	26	30	-13 cs_invvv	07c	N2062
C2709rwr/a	cs_nor3v	10e	L	F	26	30	-15 cs_nnd2g	11b	N1986
C2709rwr/a	cs_nor3v	10e	E	F	26	30	-15 cs_nnd2g	11b	N1986
C2297/b	cs_nnd2n	02c	L	F	25	30	-17 cs_invvv	07c	N1683
C2297/b	cs_nnd2n	02c	E	F	25	30	-17 cs_invvv	07c	N1683
C2723rwr/a	cs_nnd3n	05c	L	F	24	30	-20 cs_invvv	09c	N1857
C2723rwr/a	cs_nnd3n	05c	E	F	24	30	-20 cs_invvv	09c	N1857
FANINV/a	cs_invvv	01e	L	F	22	30	-28 cs_invvv	19b	N1587
FANINV/a	cs_invvv	01e	E	F	22	30	-28 cs_invvv	19b	N1587
C2487/a	cs_nnd2x	14e	L	F	22	30	-28 cs_invvv	19b	N1587
C2487/a	cs_nnd2x	14e	E	F	22	30	-28 cs_invvv	19b	N1587
C2406/b2	cs_ao22n	03c	L	F	22	30	-28 cs_invvv	19b	N1587
C2406/b2	cs_ao22n	03c	E	F	22	30	-28 cs_invvv	19b	N1587
C2217/a	cs_nnd2n	02c	L	F	22	30	-28 cs_invvv	06c	N1615
C2217/a	cs_nnd2n	02c	E	F	22	30	-28 cs_invvv	06c	N1615
C2889/b	cs_ao21n	10e	L	F	19	30	-37 cs_invvv	10c	N2000
C2889/b	cs_ao21n	10e	E	F	19	30	-38 cs_invvv	10c	N2000

***** Worst Slew per Phase *****

Early
Phase Worst Slew Pin

```
-----
C3+      60 slow_mode.clockblock/c2
C3-      60 slow_mode.clockblock/clkg
C3+R     3609 C2013/y
```

Late
Phase Worst Slew Pin

```
-----
C3+      60 slow_mode.clockblock/c2
C3-      60 slow_mode.clockblock/clkg
C3+R     3609 C2013/y
```

***** SINKLESS - Output pin not feeding into any other pins *****
Pin Cell+Power

<<<< No SINKLESS Pins >>>>

***** SOURCELESS - Input pin not fed by any other pins *****
Pin Cell+Power

<<<< No SOURCELESS Pins >>>>

***** PATHLESS - Input pin without sink and Output pin without source *****
Pin Cell+Power

```
-----
gp_tr_latch/gp_tr_a_clk      cb_mode_block
gp_tr_latch/gp_tr_b_clk      cb_mode_block
gp_tr_latch/gp_tr_scan_in    cb_mode_block
slow_mode.clockblock/scan_enable  cb_clk_32_1
slow_mode.clockblock/clkl_mode7   cb_clk_32_1
slow_mode.clockblock_1/scan_enable cb_clk_32_1
slow_mode.clockblock_1/clkl_mode7  cb_clk_32_1
slow_mode.clockblock_2/scan_enable cb_clk_32_1
slow_mode.clockblock_2/clkl_mode7  cb_clk_32_1
slow_mode.clockblock_3/scan_enable cb_clk_32_1
slow_mode.clockblock_3/clkl_mode7  cb_clk_32_1
slow_mode.clockblock_4/scan_enable cb_clk_32_1
slow_mode.clockblock_4/clkl_mode7  cb_clk_32_1
slow_mode.clockblock_5/scan_enable cb_clk_32_1
slow_mode.clockblock_5/clkl_mode7  cb_clk_32_1
slow_mode.reg_n.lat_0/clka      cl_invvn07d
slow_mode.reg_n.lat_0/scan_in   cl_invvn07d
ru_rq_blk.reg_n.lat_0/clka      cl_invvn07d
ru_rq_blk.reg_n.lat_0/scan_in   cl_invvn07d
iu_rst_fst.reg_n.lat_0/clka     cl_invvn07c
iu_rst_fst.reg_n.lat_0/scan_in  cl_invvn07c
iu_restart.reg_n.lat_0/clka     cl_nnd2n07c
iu_restart.reg_n.lat_0/scan_in  cl_nnd2n07c
ia_to_if.reg_n.lat_0/clka       cl_invvn07c
ia_to_if.reg_n.lat_0/scan_in    cl_invvn07c
frc_mmode.reg_n.lat_0/clka      cl_nnd2n07c
frc_mmode.reg_n.lat_0/scan_in   cl_nnd2n07c
local_milli.reg_n.lat_0/clka    cl_invvn07c
```

local_milli.reg_n.lat_0/scan_in	cl_invvn07c
ia_to_if_t1.reg_n.lat_0/clka	cl_invvn07c
ia_to_if_t1.reg_n.lat_0/scan_in	cl_invvn07c
mia_to_if.reg_n.lat_0/clka	cl_invvn07c
mia_to_if.reg_n.lat_0/scan_in	cl_invvn07c
slow_mode_t1.reg_n.lat_0/clka	cl_invvn07c
slow_mode_t1.reg_n.lat_0/scan_in	cl_invvn07c
iq_empty_dly.reg_n.lat_0/clka	cl_invvn05c
iq_empty_dly.reg_n.lat_0/scan_in	cl_invvn05c
slow_mode_t2.reg_n.lat_0/clka	cl_invvn07d
slow_mode_t2.reg_n.lat_0/scan_in	cl_invvn07d
s390_updt_blk.reg_n.lat_0/clka	cl_nnd2n07c
s390_updt_blk.reg_n.lat_0/scan_in	cl_nnd2n07c
sriz_nomatch.reg_n.lat_0/clka	cl_nnd2n07c
sriz_nomatch.reg_n.lat_0/scan_in	cl_nnd2n07c
bce_hold_aa.reg_n.lat_0/clka	cl_invvn07d
bce_hold_aa.reg_n.lat_0/scan_in	cl_invvn07d
sriz_actn.reg_n.lat_0/clka	cl_invvn07d
sriz_actn.reg_n.lat_0/scan_in	cl_invvn07d
sriz_actn.reg_n.lat_1/clka	cl_invvn07d
sriz_actn.reg_n.lat_1/scan_in	cl_invvn07d
op_44_dcd.reg_n.lat_0/clka	cl_ao22n07c
op_44_dcd.reg_n.lat_0/scan_in	cl_ao22n07c
op_cmp_tr.reg_n.lat_0/clka	cl_nnd2n07c
op_cmp_tr.reg_n.lat_0/scan_in	cl_nnd2n07c
num_dcd.reg_n.lat_0/clka	cl_ao22n07c
num_dcd.reg_n.lat_0/scan_in	cl_ao22n07c
num_dcd.reg_n.lat_1/clka	cl_ao22n07c
num_dcd.reg_n.lat_1/scan_in	cl_ao22n07c
mia_to_if_t1.reg_n.lat_0/clka	cl_invvn07c
mia_to_if_t1.reg_n.lat_0/scan_in	cl_invvn07c
eu_op_encode.reg_n.lat_0/clka	cl_invvn06d
eu_op_encode.reg_n.lat_0/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_1/clka	cl_invvn06d
eu_op_encode.reg_n.lat_1/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_2/clka	cl_invvn06d
eu_op_encode.reg_n.lat_2/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_3/clka	cl_invvn06d
eu_op_encode.reg_n.lat_3/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_4/clka	cl_invvn06d
eu_op_encode.reg_n.lat_4/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_5/clka	cl_invvn06d
eu_op_encode.reg_n.lat_5/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_6/clka	cl_invvn06d
eu_op_encode.reg_n.lat_6/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_7/clka	cl_invvn06d
eu_op_encode.reg_n.lat_7/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_8/clka	cl_invvn06d
eu_op_encode.reg_n.lat_8/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_9/clka	cl_invvn07d
eu_op_encode.reg_n.lat_9/scan_in	cl_invvn07d
eu_op_encode.reg_n.lat_10/clka	cl_invvn06d
eu_op_encode.reg_n.lat_10/scan_in	cl_invvn06d
eu_op_encode.reg_n.lat_11/clka	cl_invvn06d
eu_op_encode.reg_n.lat_11/scan_in	cl_invvn06d

frc_blk_1cyc.reg_n.lat_0/clka	cl_nnd2n07c
frc_blk_1cyc.reg_n.lat_0/scan_in	cl_nnd2n07c
local_milli_t1.reg_n.lat_0/clka	cl_invvn07c
local_milli_t1.reg_n.lat_0/scan_in	cl_invvn07c
local_milli_t2.reg_n.lat_0/clka	cl_invvn07c
local_milli_t2.reg_n.lat_0/scan_in	cl_invvn07c
bht_block.reg_n.lat_0/clka	cl_invvn07d
bht_block.reg_n.lat_0/scan_in	cl_invvn07d
srlz_blk.reg_n.lat_0/clka	cl_nnd2n07c
srlz_blk.reg_n.lat_0/scan_in	cl_nnd2n07c
exc_cond.reg_n.lat_0/clka	cl_invvn07d
exc_cond.reg_n.lat_0/scan_in	cl_invvn07d
slow_mode_dly.reg_n.lat_0/clka	cl_invvn07d
slow_mode_dly.reg_n.lat_0/scan_in	cl_invvn07d
dcd_succ_disable_scan.reg_n.lat_0/clka	cl_invvn07d
dcd_succ_disable_scan.reg_n.lat_0/scan_in	cl_invvn07d
dcd_succ_disable_scan.reg_n.lat_1/clka	cl_invvn07d
dcd_succ_disable_scan.reg_n.lat_1/scan_in	cl_invvn07d
dcd_succ_disable_scan.reg_n.lat_2/clka	cl_invvn05d
dcd_succ_disable_scan.reg_n.lat_2/scan_in	cl_invvn05d
drain_blk.reg_n.lat_0/clka	cl_nnd2n07c
drain_blk.reg_n.lat_0/scan_in	cl_nnd2n07c
dcd_ilc.reg_n.lat_0/clka	cl_nnd2n07c
dcd_ilc.reg_n.lat_0/scan_in	cl_nnd2n07c
dcd_ilc.reg_n.lat_1/clka	cl_nnd3n07c
dcd_ilc.reg_n.lat_1/scan_in	cl_nnd3n07c
slow_mode_blk.reg_n.lat_0/clka	cl_nnd2n07c
slow_mode_blk.reg_n.lat_0/scan_in	cl_nnd2n07c
op_cmp_44.reg_n.lat_0/clka	cl_invvn07d
op_cmp_44.reg_n.lat_0/scan_in	cl_invvn07d
op_cmp_dsbl.reg_n.lat_0/clka	cl_nnd2n07c
op_cmp_dsbl.reg_n.lat_0/scan_in	cl_nnd2n07c
eu_frc_milli.reg_n.lat_0/clka	cl_invvn07d
eu_frc_milli.reg_n.lat_0/scan_in	cl_invvn07d
bcr_store_stat.reg_n.lat_0/clka	cl_ao22n07c
bcr_store_stat.reg_n.lat_0/scan_in	cl_ao22n07c
exc_info.reg_n.lat_0/clka	cl_ao22n07c
exc_info.reg_n.lat_0/scan_in	cl_ao22n07c
exc_info.reg_n.lat_1/clka	cl_ao22n07c
exc_info.reg_n.lat_1/scan_in	cl_ao22n07c
exc_info.reg_n.lat_2/clka	cl_ao22n07c
exc_info.reg_n.lat_2/scan_in	cl_ao22n07c
exc_info.reg_n.lat_3/clka	cl_ao22n07c
exc_info.reg_n.lat_3/scan_in	cl_ao22n07c
spare.reg_n.lat_0/clka	cl_invvn07d
spare.reg_n.lat_0/scan_in	cl_invvn07d
mcset_e1.reg_n.lat_0/clka	cl_invvn07c
mcset_e1.reg_n.lat_0/scan_in	cl_invvn07c
eu_iu_spare.reg_n.lat_0/clka	cl_invvn07d
eu_iu_spare.reg_n.lat_0/scan_in	cl_invvn07d
dsbl_ovrlp_blk.reg_n.lat_0/clka	cl_nnd2n07c
dsbl_ovrlp_blk.reg_n.lat_0/scan_in	cl_nnd2n07c
inst_fetch.reg_n.lat_0/clka	cl_invvn07d
inst_fetch.reg_n.lat_0/scan_in	cl_invvn07d
iu_dsbl_ovrlp.reg_n.lat_0/clka	cl_nor2n06c

iu_dsbl_ovrlp.reg_n.lat_0/scan_in	cl_nor2n06c
ex_in_prog.reg_n.lat_0/clka	cl_nnd2n07c
ex_in_prog.reg_n.lat_0/scan_in	cl_nnd2n07c
blk_dcd.reg_n.lat_0/clka	cl_invvn06d
blk_dcd.reg_n.lat_0/scan_in	cl_invvn06d
blk_dcd.reg_n.lat_1/clka	cl_invvn06d
blk_dcd.reg_n.lat_1/scan_in	cl_invvn06d
blk_dcd.reg_n.lat_2/clka	cl_invvn06d
blk_dcd.reg_n.lat_2/scan_in	cl_invvn06d
blk_dcd.reg_n.lat_3/clka	cl_ao21n07c
blk_dcd.reg_n.lat_3/scan_in	cl_ao21n07c
dcd_succ_dly.reg_n.lat_0/clka	cl_invvn07c
dcd_succ_dly.reg_n.lat_0/scan_in	cl_invvn07c
exec_recov.reg_n.lat_0/clka	cl_nnd2n07c
exec_recov.reg_n.lat_0/scan_in	cl_nnd2n07c
ru_updt_dly.reg_n.lat_0/clka	cl_invvn07d
ru_updt_dly.reg_n.lat_0/scan_in	cl_invvn07d
iu_rst_fst_t1.reg_n.lat_0/clka	cl_invvn07c
iu_rst_fst_t1.reg_n.lat_0/scan_in	cl_invvn07c
inst_store.reg_n.lat_0/clka	cl_invvn07d
inst_store.reg_n.lat_0/scan_in	cl_invvn07d
eu_dsbl_aftr.reg_n.lat_0/clka	cl_invvn07d
eu_dsbl_aftr.reg_n.lat_0/scan_in	cl_invvn07d
dcdsuc_err.reg_n.lat_0/clka	cl_nnd2n07c
dcdsuc_err.reg_n.lat_0/scan_in	cl_nnd2n07c
dcd_cyl_cnt.reg_n.lat_0/clka	cl_nnd2n07c
dcd_cyl_cnt.reg_n.lat_0/scan_in	cl_nnd2n07c
dcd_cyl_cnt.reg_n.lat_1/clka	cl_nnd3n07c
dcd_cyl_cnt.reg_n.lat_1/scan_in	cl_nnd3n07c
blk_mcend.reg_n.lat_0/clka	cl_nnd2n07c
blk_mcend.reg_n.lat_0/scan_in	cl_nnd2n07c
op_44_info.reg_n.lat_0/clka	cl_invvn06c
op_44_info.reg_n.lat_0/scan_in	cl_invvn06c
op_44_info.reg_n.lat_1/clka	cl_invvn06c
op_44_info.reg_n.lat_1/scan_in	cl_invvn06c
rcvry_reset.reg_n.lat_0/clka	cl_invvn07d
rcvry_reset.reg_n.lat_0/scan_in	cl_invvn07d
br_wrongs.reg_n.lat_0/clka	cl_ao21n07c
br_wrongs.reg_n.lat_0/scan_in	cl_ao21n07c
rstrt_reset.reg_n.lat_0/clka	cl_invvn07d
rstrt_reset.reg_n.lat_0/scan_in	cl_invvn07d
br_dcd_pend.reg_n.lat_0/clka	cl_nnd2n07c
br_dcd_pend.reg_n.lat_0/scan_in	cl_nnd2n07c

***** Timing Checks Not Performed *****

<<< none >>>

***** SUMMARY *****

Total Number of CAP violations	:: 69
Total Number of Early SLEW violations	:: 79
Total Number of Late SLEW violations	:: 159
Total Number of Sourceless Pins	:: 0
Total Number of Sinkless Pins	:: 0
Total Number of Pathless Pins	:: 181
Total Number of Timing checks not performed	:: 0

> accTime_display

Timing Correction Accounting Results

Transform - repower

Tested: 4048, Applied: 123, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0822, Max: 140.6079, Avg: 14.9094

% -> Min: 0.0247, Max: 1204.4907, Avg: 26.2961

(Crit) % -> Min: 0.0044, Max: 6.1281, Avg: 0.7524

Area Cost -> Min: -4.0000, Max: 11.0000, Avg: 0.6098

% -> Min: -0.0859, Max: 0.2388, Avg: 0.0133

Total Averages

Run Time: 0.0000

Slack Gain: 1833.8529

Area Cost: 75.0000

Transform - clone

Tested: 57, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - fantom

Tested: 39, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - faninv

Tested: 39, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 12.0017, Max: 12.0017, Avg: 12.0017

% -> Min: 0.6101, Max: 0.6101, Avg: 0.6101

(Crit) % -> Min: 0.6101, Max: 0.6101, Avg: 0.6101

Area Cost -> Min: 2.0000, Max: 2.0000, Avg: 2.0000

% -> Min: 0.0434, Max: 0.0434, Avg: 0.0434

Total Averages

Run Time: 0.0000

Slack Gain: 12.0017

Area Cost: 2.0000

Transform - onebuff

Tested: 2467, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - dinv

Tested: 2454, Applied: 22, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0500, Max: 2042.1168, Avg: 164.9743

% -> Min: 0.0074, Max: 95.4595, Avg: 26.1605

(Crit) % -> Min: 0.0026, Max: 91.0505, Avg: 7.5052

Area Cost -> Min: -17.0000, Max: 0.0000, Avg: -3.8182

% -> Min: -0.3668, Max: 0.0000, Avg: -0.0836

Total Averages

Run Time: 0.0000

Slack Gain: 3629.4342

Area Cost: -84.0000

Transform - tpushb

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tpushl

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tpushr

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tbmove

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tswap

Tested: 836, Applied: 59, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0001, Max: 20.6266, Avg: 4.2551

% -> Min: 0.0000, Max: 2.9882, Avg: 0.7086

(Crit) % -> Min: 0.0000, Max: 1.2355, Avg: 0.2272

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Slack Gain: 251.0519

Area Cost: 0.0000

Transform - tsteal

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tcfe

Tested: 364, Applied: 4, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 13.5331, Max: 39.8060, Avg: 30.0562

% -> Min: 3.4911, Max: 33.9806, Avg: 14.4824

(Crit) % -> Min: 0.6789, Max: 1.9969, Avg: 1.5078

Area Cost -> Min: -2.0000, Max: -2.0000, Avg: -2.0000
% -> Min: -0.0442, Max: -0.0441, Avg: -0.0442

Total Averages

Run Time: 0.0000

Slack Gain: 120.2248

Area Cost: -8.0000

Transform - texpand

Tested: 1428, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 1.0000, Max: 1.0000, Avg: 1.0000

% -> Min: 0.0667, Max: 0.0667, Avg: 0.0667

(Crit) % -> Min: 0.0506, Max: 0.0506, Avg: 0.0506

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Slack Gain: 1.0000

Area Cost: 0.0000

Transform - trecover

Tested: 683, Applied: 3, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 5.3128, Max: 20.5709, Avg: 12.3908

% -> Min: 0.6576, Max: 1.9107, Avg: 1.3506

(Crit) % -> Min: 0.2701, Max: 1.0457, Avg: 0.6299

Area Cost -> Min: -1.0000, Max: 4.0000, Avg: 1.3333

% -> Min: -0.0217, Max: 0.0870, Avg: 0.0290

Total Averages

Run Time: 0.0000

Slack Gain: 37.1723

Area Cost: 4.0000

Transform - texpao

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tmerge

Tested: 353, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tncube

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tdual_correct

Tested: 702, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - speedreg

Tested: 598, Applied: 28, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0005, Max: 4.8468, Avg: 0.8625

% -> Min: 0.0001, Max: 1.9721, Avg: 0.2321

(Crit) % -> Min: 0.0000, Max: 0.2479, Avg: 0.0441

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Slack Gain: 24.1497

Area Cost: 0.0000

Transform - absrbreg

Tested: 598, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages.

Run Time: 0.0000

Information By Driver

=====

Transform - repower

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 494, Applied: 31, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.5562, Max: 140.6079, Avg: 12.6121

% -> Min: 0.0247, Max: 6.1281, Avg: 0.5969

(Crit) % -> Min: 0.0247, Max: 6.1281, Avg: 0.5919

Area Cost -> Min: -4.0000, Max: 11.0000, Avg: 2.5484

% -> Min: -0.0859, Max: 0.2388, Avg: 0.0554

NonCritical

Tested: 3554, Applied: 92, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0822, Max: 66.5485, Avg: 15.6834

% -> Min: 0.0265, Max: 1204.4907, Avg: 34.9557

(Crit) % -> Min: 0.0044, Max: 3.4038, Avg: -0.8065

Area Cost -> Min: -4.0000, Max: 0.0000, Avg: -0.0435

% -> Min: -0.0859, Max: 0.0000, Avg: -0.0009

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - clone

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 57, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - fantom

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 39, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - faninv

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 39, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 12.0017, Max: 12.0017, Avg: 12.0017

% -> Min: 0.6101, Max: 0.6101, Avg: 0.6101

(Crit) % -> Min: 0.6101, Max: 0.6101, Avg: 0.6101

Area Cost -> Min: 2.0000, Max: 2.0000, Avg: 2.0000

% -> Min: 0.0434, Max: 0.0434, Avg: 0.0434

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - onebuff

Quick

Tested: 1266, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 1189, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - dinv

Quick

Tested: 1256, Applied: 15, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 50.2148, Max: 2042.1168, Avg: 241.9390

% -> Min: 2.3647, Max: 95.4595, Avg: 38.3639

(Crit) % -> Min: 2.2389, Max: 91.0505, Avg: 11.0064

Area Cost -> Min: -17.0000, Max: 0.0000, Avg: -4.2667

% -> Min: -0.3668, Max: 0.0000, Avg: -0.0939

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 1186, Applied: 7, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0500, Max: 0.0500, Avg: 0.0500

% -> Min: 0.0074, Max: 0.0156, Avg: 0.0103

(Crit) % -> Min: 0.0026, Max: 0.0026, Avg: 0.0026

Area Cost -> Min: -4.0000, Max: -2.0000, Avg: -2.8571

% -> Min: -0.0862, Max: -0.0430, Avg: -0.0615

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tpushb

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tpushl

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tpushr

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tbmove

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tswap

Quick

Tested: 737, Applied: 52, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0001, Max: 20.6266, Avg: 3.9889

% -> Min: 0.0000, Max: 2.9882, Avg: 0.7845

(Crit) % -> Min: 0.0000, Max: 1.2355, Avg: 0.2213

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000
% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 99, Applied: 7, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.3071, Max: 14.5166, Avg: 6.2324
% -> Min: 0.0000, Max: 0.6232, Avg: 0.1450
(Crit) % -> Min: 0.0134, Max: 0.6232, Avg: 0.2706

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000
% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tsteal

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tcte

Quick

Tested: 358, Applied: 4, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 13.5331, Max: 39.8060, Avg: 30.0562
% -> Min: 3.4911, Max: 33.9806, Avg: 14.4824
(Crit) % -> Min: 0.6789, Max: 1.9969, Avg: 1.5078

Area Cost -> Min: -2.0000, Max: -2.0000, Avg: -2.0000
% -> Min: -0.0442, Max: -0.0441, Avg: -0.0442

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - texpand

Quick

Tested: 1410, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 1.0000, Max: 1.0000, Avg: 1.0000

% -> Min: 0.0667, Max: 0.0667, Avg: 0.0667

(Crit) % -> Min: 0.0506, Max: 0.0506, Avg: 0.0506

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 18, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - trecover

Quick

Tested: 683, Applied: 3, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 5.3128, Max: 20.5709, Avg: 12.3908

% -> Min: 0.6576, Max: 1.9107, Avg: 1.3506

(Crit) % -> Min: 0.2701, Max: 1.0457, Avg: 0.6299

Area Cost -> Min: -1.0000, Max: 4.0000, Avg: 1.3333

% -> Min: -0.0217, Max: 0.0870, Avg: 0.0290

Critical

Tested: 0, Applied: 0, Corrected: 0

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - texpao

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tmerge

Quick

Tested: 353, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 0, Applied: 0, Corrected: 0

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tncube

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tdual_correct

Quick

Tested: 702, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 0, Applied: 0, Corrected: 0

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - speedreg

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 592, Applied: 28, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0005, Max: 4.8468, Avg: 0.8625

% -> Min: 0.0001, Max: 1.9721, Avg: 0.2321

(Crit) % -> Min: 0.0000, Max: 0.2479, Avg: 0.0441

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

% -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - absrbreg

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 592, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Correct

Tested: 0, Applied: 0, Corrected: 0

> write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:41 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack

Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time   RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT  ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup      ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold       ClkGHld      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width  ClkTPW       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup                   Setup        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
Hold                     Hold          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
EndOfCycle              EndOfC       ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
ClockPulseWidth         ClkPW        ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
ClockSeparation         ClkSep       ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
Loop                     ALTest      ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
Arrival Time Limiting   ATLimit      Slack discontinuity due to failed test
  
```

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func T.Adj
1 dcd_succ_last_t1	R C3+R	2668	-1669	3294	1011	1 PO	0
dcd_succ_last_t1		999				0	
----> BOX714/OUT	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1							
----> BOX714/IN	R C3+R	2668	-1669	3294	1011	1 IOPAD	IOPAD
0 dcd_succ_last_t1&0							
----> C167/y	R C3+R	2668	-1669	3294	1011	1 cs_invvv	01c NOT
0 dcd_succ_last_t1&0							
----> C167/a	F C3+R	1075	-1669	27	139	4 cs_invvv	01c NOT
1594 N675							
---->{a} C2738/y	F C3+R	1075	-1669	27	139	4 cs_nnd2x	14b NAND
0 N675							
----> C2738/a	R C3+R	1056	-1669	33	114	1 cs_nnd2x	14b NAND
19 last_cycle							

```

---->{b} C2487/y          R C3+R   1056 -1669   33  114  1 cs_nnd2x  14e NAND
0 last_cycle
----> C2487/a             F C3+R   1035 -1669   22  145  3 cs_nnd2x  14e NAND
21 N1587
----> C1952/y            F C3+R   1035 -1669   22  145  3 cs_invvv  19b NOT    0
N1587
----> C1952/a            R C3+R   1024 -1669   80  319  1 cs_invvv  19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT          R C3+R   1024 -1669   80  319  1 IOPAD      IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN          R C3+R   1024 -1669   80  319  1 IOPAD      IOPAD    0
num_dcd_cyl(1)
----> num_dcd_cyl(1)      R C3+R   1024 -1669   80  319  1 PI          0
num_dcd_cyl(1)

```

```

--
  2 iu_reset_op_c_t1      R C3+R   2399 -1400  3318 1011  1 PO          0
iu_reset_op_c_t1
RAT                        999                                0
----> BOX716/OUT          R C3+R   2399 -1400  3318 1011  1 IOPAD      IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN          R C3+R   2399 -1400  3318 1044  3 IOPAD      IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y          R C3+R   2399 -1400  3318 1044  3 cs_nnd2v  02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a             F C3+R   536 -1400   100  196  6 cs_nnd2v  02c NAND
1863 gbfonet_6
----> gbfozell_6/y        F C3+R   536 -1400   100  196  6 cs_invvv  09c NOT
0 gbfonet_6
----> gbfozell_6/a        R C3+R   472 -1400   184   44  1 cs_invvv  09c NOT
64 N2031
---->{b} C2162/y          R C3+R   472 -1400   184   44  1 cs_nnd3v  02c NAND
0 N2031
----> C2162/a             F C3+R   358 -1400   144  217  5 cs_nnd3v  02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R   358 -1400   144  217  5 cl_invvn  07d
SRL    0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2      R C3+    160   N/C    60  222 13 cl_invvn  07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2        R C3+    160   N/C    60  222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
> tiegen FOLIM(1)
> padnet

```

[padnet]: Added 0 IOPADs.

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_utils.tcl

```

> idm::get_active_network
> idm::foreach_proto_pin po -proto_box __CiType_16_30a98de8...
> idm::object_name __CiType_17_30aac34c
> idm::get_net_from_proto_pin __CiType_17_30aac34c
> idm::object_name __CiType_20_3057fc90

```

[CTE::fixup_po_nets]: (I) PO net 'N36' doesn't match PO 'iu_eu_opcode_cmp' -> attempting to rename

```

> idm::locate_net -name iu_eu_opcode_cmp -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057fc90 -name iu_eu_...

```



```

> idm::object_name __CiType_17_30aac328
> idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
[CTE::fixup_po_nets]: (I) PO net 'N158' doesn't match PO 'iu_rcvry_reset' -> attempting to rename
> idm::locate_net -name iu_rcvry_reset -proto_box __CiType...
> idm::set_net_name -net __CiType_20_30590568 -name iu_rcv...
> idm::object_name __CiType_17_30aac304
> idm::get_net_from_proto_pin __CiType_17_30aac304
> idm::object_name __CiType_20_3058f6e0
> idm::object_name __CiType_17_30aac2e0
> idm::get_net_from_proto_pin __CiType_17_30aac2e0
> idm::object_name __CiType_20_3057f6c8
> idm::object_name __CiType_17_30aac2bc
> idm::get_net_from_proto_pin __CiType_17_30aac2bc
> idm::object_name __CiType_20_3057fe48
[CTE::fixup_po_nets]: (I) PO net 'N12' doesn't match PO 'iu_milli_mode' -> attempting to rename
> idm::locate_net -name iu_milli_mode -proto_box __CiType...
> idm::set_net_name -net __CiType_20_3057fe48 -name iu_mil...
> idm::object_name __CiType_17_30aac298
> idm::get_net_from_proto_pin __CiType_17_30aac298
> idm::object_name __CiType_20_3059af68
> idm::object_name __CiType_17_30a4bda8
> idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
[CTE::fixup_po_nets]: (I) PO net 'N2086' doesn't match PO 'dcd_succ_last' -> attempting to rename
> idm::locate_net -name dcd_succ_last -proto_box __CiType...
> idm::set_net_name -net __CiType_20_3059ae78 -name dcd_su...
> idm::object_name __CiType_17_30a4bd84
> idm::get_net_from_proto_pin __CiType_17_30a4bd84
> idm::object_name __CiType_20_3057fd58
[CTE::fixup_po_nets]: (I) PO net 'N26' doesn't match PO 'iu_eu_op_nomatch' -> attempting to rename
> idm::locate_net -name iu_eu_op_nomatch -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057fd58 -name iu_eu...
> idm::object_name __CiType_17_30a4bd60
> idm::get_net_from_proto_pin __CiType_17_30a4bd60
> idm::object_name __CiType_20_30568e50
> idm::object_name __CiType_17_30a4bd3c
> idm::get_net_from_proto_pin __CiType_17_30a4bd3c
> idm::object_name __CiType_20_3057fcb8
[CTE::fixup_po_nets]: (I) PO net 'N34' doesn't match PO 'id_xcute_targ' -> attempting to rename
> idm::locate_net -name id_xcute_targ -proto_box __CiType...
> idm::set_net_name -net __CiType_20_3057fcb8 -name id_xcu...
> idm::object_name __CiType_17_30a4bd18
> idm::get_net_from_proto_pin __CiType_17_30a4bd18
> idm::object_name __CiType_20_3057fdf8
[CTE::fixup_po_nets]: (I) PO net 'N14' doesn't match PO 'xc_frc_ia_to_if_t1' -> attempting to rename
> idm::locate_net -name xc_frc_ia_to_if_t1 -proto_box __Ci...
> idm::set_net_name -net __CiType_20_3057fdf8 -name xc_frc...
> idm::object_name __CiType_17_30a4bcf4
> idm::get_net_from_proto_pin __CiType_17_30a4bcf4
> idm::object_name __CiType_20_3057f6a0
[CTE::fixup_po_nets]: (I) PO net 'N2097' doesn't match PO 'dcd_success_tr' -> attempting to rename
> idm::locate_net -name dcd_success_tr -proto_box __CiType...
> idm::set_net_name -net __CiType_20_3057f6a0 -name dcd_su...
> idm::object_name __CiType_17_30a4bcd0

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> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
> idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
> idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
> idm::object_name __CiType_20_3057ff60
[CTE::fixup_po_nets]: (I) PO net 'N0' doesn't match PO 'iu_slow_mode' -> attempting to rename
> idm::locate_net -name iu_slow_mode -proto_box __CiType_1...
> idm::set_net_name -net __CiType_20_3057ff60 -name iu_slo...
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
> idm::object_name __CiType_20_3057fdd0
[CTE::fixup_po_nets]: (I) PO net 'N16' doesn't match PO 'xc_frc_milli' -> attempting to rename
> idm::locate_net -name xc_frc_milli -proto_box __CiType_1...
> idm::set_net_name -net __CiType_20_3057fdd0 -name xc_frc...
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
> idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
> idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
> idm::object_name __CiType_20_3057fa60
[CTE::fixup_po_nets]: (I) PO net 'N2089' doesn't match PO 'iu_milli_mode_t1' -> attempting to rename
> idm::locate_net -name iu_milli_mode_t1 -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057fa60 -name iu_mil...
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
> idm::object_name __CiType_20_3057f628
[CTE::fixup_po_nets]: (I) PO net 'N72' doesn't match PO 'iu_milli_mode_t2' -> attempting to rename
> idm::locate_net -name iu_milli_mode_t2 -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057f628 -name iu_mil...
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
> idm::object_name __CiType_20_3057fa38
[CTE::fixup_po_nets]: (I) PO net 'N2090' doesn't match PO 'iu_milli_mode_t3' -> attempting to rename
> idm::locate_net -name iu_milli_mode_t3 -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057fa38 -name iu_mil...
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
> idm::object_name __CiType_20_3057fc68
[CTE::fixup_po_nets]: (I) PO net 'N42' doesn't match PO 'xc_frc_milli_t1' -> attempting to rename
> idm::locate_net -name xc_frc_milli_t1 -proto_box __CiTyp...
> idm::set_net_name -net __CiType_20_3057fc68 -name xc_frc...
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
> idm::object_name __CiType_20_3057f600
[CTE::fixup_po_nets]: (I) PO net 'N2096' doesn't match PO 'iu_exc_cond' -> attempting to rename
> idm::locate_net -name iu_exc_cond -proto_box __CiType_16...

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> idm::set_net_name -net __CiType_20_3057f600 -name iu_exc...
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
> idm::object_name __CiType_20_3057fa10
[CTE::fixup_po_nets]: (I) PO net 'N80' doesn't match PO 'slow_mode_tr' -> attempting to rename
> idm::locate_net -name slow_mode_tr -proto_box __CiType_1...
> idm::set_net_name -net __CiType_20_3057fa10 -name slow_m...
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
> idm::object_name __CiType_20_3057fd80
[CTE::fixup_po_nets]: (I) PO net 'N22' doesn't match PO 'iu_eu_slow_mode' -> attempting to rename
> idm::locate_net -name iu_eu_slow_mode -proto_box __CiTyp...
> idm::set_net_name -net __CiType_20_3057fd80 -name iu_eu_...
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
> idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
> idm::object_name __CiType_20_3057f650
[CTE::fixup_po_nets]: (I) PO net 'N70' doesn't match PO 'iu_milli_mode_tr' -> attempting to rename
> idm::locate_net -name iu_milli_mode_tr -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057f650 -name iu_mil...
> idm::object_name __CiType_17_30a4ba24
> idm::get_net_from_proto_pin __CiType_17_30a4ba24
> idm::object_name __CiType_20_3057f7b8
[CTE::fixup_po_nets]: (I) PO net 'N140' doesn't match PO 'iu_reset_if' -> attempting to rename
> idm::locate_net -name iu_reset_if -proto_box __CiType_16...
> idm::set_net_name -net __CiType_20_3057f7b8 -name iu_res...
> idm::object_name __CiType_17_30a4ba00
> idm::get_net_from_proto_pin __CiType_17_30a4ba00
> idm::object_name __CiType_20_3058fbb8
[CTE::fixup_po_nets]: (I) PO net 'N78' doesn't match PO 'exc_cond_tr' -> attempting to rename
> idm::locate_net -name exc_cond_tr -proto_box __CiType_16...
> idm::set_net_name -net __CiType_20_3058fbb8 -name exc_co...
> idm::object_name __CiType_17_30a4b9dc
> idm::get_net_from_proto_pin __CiType_17_30a4b9dc
> idm::object_name __CiType_20_3059b1c0
[CTE::fixup_po_nets]: (I) PO net 'N2088' doesn't match PO 'dcd_succ_first' -> attempting to rename
> idm::locate_net -name dcd_succ_first -proto_box __CiType...
> idm::set_net_name -net __CiType_20_3059b1c0 -name dcd_su...
> idm::object_name __CiType_17_30a4b9b8
> idm::get_net_from_proto_pin __CiType_17_30a4b9b8
> idm::object_name __CiType_20_3057f808
[CTE::fixup_po_nets]: (I) PO net 'N136' doesn't match PO 'execute_recovery' -> attempting to rename
> idm::locate_net -name execute_recovery -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057f808 -name execut...
> idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin __CiType_17_30a4b994
> idm::object_name __CiType_20_3059b648
> idm::object_name __CiType_17_30a4b970
> idm::get_net_from_proto_pin __CiType_17_30a4b970
> idm::object_name __CiType_20_3057fec0
[CTE::fixup_po_nets]: (I) PO net 'N8' doesn't match PO 'xc_frc_ia_to_if' -> attempting to rename
> idm::locate_net -name xc_frc_ia_to_if -proto_box __CiTyp...
> idm::set_net_name -net __CiType_20_3057fec0 -name xc_frc...

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> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
> idm::object_name __CiType_20_3057fda8
[CTE::fixup_po_nets]: (I) PO net 'N18' doesn't match PO 'iu_slow_mode_t1' -> attempting to rename
> idm::locate_net -name iu_slow_mode_t1 -proto_box __CiType...
> idm::set_net_name -net __CiType_20_3057fda8 -name iu_slo...
> idm::object_name __CiType_17_30a4b928
> idm::get_net_from_proto_pin __CiType_17_30a4b928
> idm::object_name __CiType_20_3059b7d8
[CTE::fixup_po_nets]: (I) PO net 'gpnr_scan_out&1' doesn't match PO 'gpnr_scan_out' -> attempting to
rename
> idm::locate_net -name gpnr_scan_out -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3059b7d8 -name gpnr_s...
> idm::object_name __CiType_17_30a4b904
> idm::get_net_from_proto_pin __CiType_17_30a4b904
> idm::object_name __CiType_20_3057ff10
[CTE::fixup_po_nets]: (I) PO net 'N4' doesn't match PO 'iu_reset_fst' -> attempting to rename
> idm::locate_net -name iu_reset_fst -proto_box __CiType_1...
> idm::set_net_name -net __CiType_20_3057ff10 -name iu_res...
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto_pin __CiType_17_30a4b8bc
> idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::get_net_from_proto_pin __CiType_17_30a4b898
> idm::object_name __CiType_20_30590540
[CTE::fixup_po_nets]: (I) PO net 'N134' doesn't match PO 'iu_eu_dcd_succ_tr' -> attempting to rename
> idm::locate_net -name iu_eu_dcd_succ_tr -proto_box __CiT...
> idm::set_net_name -net __CiType_20_30590540 -name iu_eu_...
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
[CTE::fixup_po_nets]: (I) PO net 'N146' doesn't match PO 'idcdsuc_err' -> attempting to rename
> idm::locate_net -name idcdsuc_err -proto_box __CiType_16...
> idm::set_net_name -net __CiType_20_3057f790 -name idcdsu...
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
> idm::object_name __CiType_20_3057fe70
[CTE::fixup_po_nets]: (I) PO net 'N10' doesn't match PO 'frc_milli' -> attempting to rename
> idm::locate_net -name frc_milli -proto_box __CiType_16_3...
> idm::set_net_name -net __CiType_20_3057fe70 -name frc_milli
> idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17_30a4b82c
> idm::object_name __CiType_20_3057f998
[CTE::fixup_po_nets]: (I) PO net 'N2092' doesn't match PO 'iu_intrupt_info(0)' -> attempting to rename
> idm::locate_net -name iu_intrupt_info(0) -proto_box __Ci...
> idm::set_net_name -net __CiType_20_3057f998 -name iu_int...
> idm::object_name __CiType_17_30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
> idm::object_name __CiType_20_3057f970
[CTE::fixup_po_nets]: (I) PO net 'N2093' doesn't match PO 'iu_intrupt_info(1)' -> attempting to rename
> idm::locate_net -name iu_intrupt_info(1) -proto_box __Ci...
> idm::set_net_name -net __CiType_20_3057f970 -name iu_int...
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17_30a4b7e4
> idm::object_name __CiType_20_3057f948

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[CTE::fixup_po_nets]: (I) PO net 'N2094' doesn't match PO 'iu_intrupt_info(2)' -> attempting to rename
  > idm::locate_net -name iu_intrupt_info(2) -proto_box __Ci...
  > idm::set_net_name -net __CiType_20_3057f948 -name iu_int...
  > idm::object_name __CiType_17_30a4b7c0
  > idm::get_net_from_proto_pin __CiType_17_30a4b7c0
  > idm::object_name __CiType_20_3057f920
[CTE::fixup_po_nets]: (I) PO net 'N2095' doesn't match PO 'iu_intrupt_info(3)' -> attempting to rename
  > idm::locate_net -name iu_intrupt_info(3) -proto_box __Ci...
  > idm::set_net_name -net __CiType_20_3057f920 -name iu_int...
  > idm::object_name __CiType_17_30a4b79c
  > idm::get_net_from_proto_pin __CiType_17_30a4b79c
  > idm::object_name __CiType_20_3057f8d0
[CTE::fixup_po_nets]: (I) PO net 'N126' doesn't match PO 'blk_dcd_info_tr(0)' -> attempting to rename
  > idm::locate_net -name blk_dcd_info_tr(0) -proto_box __Ci...
  > idm::set_net_name -net __CiType_20_3057f8d0 -name blk_dc...
  > idm::object_name __CiType_17_30a4b778
  > idm::get_net_from_proto_pin __CiType_17_30a4b778
  > idm::object_name __CiType_20_3057f880
[CTE::fixup_po_nets]: (I) PO net 'N128' doesn't match PO 'blk_dcd_info_tr(1)' -> attempting to rename
  > idm::locate_net -name blk_dcd_info_tr(1) -proto_box __Ci...
  > idm::set_net_name -net __CiType_20_3057f880 -name blk_dc...
  > idm::object_name __CiType_17_30a4b754
  > idm::get_net_from_proto_pin __CiType_17_30a4b754
  > idm::object_name __CiType_20_3057f858
[CTE::fixup_po_nets]: (I) PO net 'N130' doesn't match PO 'blk_dcd_info_tr(2)' -> attempting to rename
  > idm::locate_net -name blk_dcd_info_tr(2) -proto_box __Ci...
  > idm::set_net_name -net __CiType_20_3057f858 -name blk_dc...
  > idm::object_name __CiType_17_30a4b730
  > idm::get_net_from_proto_pin __CiType_17_30a4b730
  > idm::object_name __CiType_20_3057f830
[CTE::fixup_po_nets]: (I) PO net 'N132' doesn't match PO 'blk_dcd_info_tr(3)' -> attempting to rename
  > idm::locate_net -name blk_dcd_info_tr(3) -proto_box __Ci...
  > idm::set_net_name -net __CiType_20_3057f830 -name blk_dc...
  > idm::object_name __CiType_17_30a4b70c
  > idm::get_net_from_proto_pin __CiType_17_30a4b70c
  > idm::object_name __CiType_20_3057fc40
[CTE::fixup_po_nets]: (I) PO net 'N44' doesn't match PO 'iu_srlz_op_encode(0)' -> attempting to rename
  > idm::locate_net -name iu_srlz_op_encode(0) -proto_box __...
  > idm::set_net_name -net __CiType_20_3057fc40 -name iu_srl...
  > idm::object_name __CiType_17_30a4b6e8
  > idm::get_net_from_proto_pin __CiType_17_30a4b6e8
  > idm::object_name __CiType_20_3057fc18
[CTE::fixup_po_nets]: (I) PO net 'N46' doesn't match PO 'iu_srlz_op_encode(1)' -> attempting to rename
  > idm::locate_net -name iu_srlz_op_encode(1) -proto_box __...
  > idm::set_net_name -net __CiType_20_3057fc18 -name iu_srl...
  > idm::object_name __CiType_17_30a4b6c4
  > idm::get_net_from_proto_pin __CiType_17_30a4b6c4
  > idm::object_name __CiType_20_3057fbf0
[CTE::fixup_po_nets]: (I) PO net 'N48' doesn't match PO 'iu_srlz_op_encode(2)' -> attempting to rename
  > idm::locate_net -name iu_srlz_op_encode(2) -proto_box __...
  > idm::set_net_name -net __CiType_20_3057fbf0 -name iu_srl...
  > idm::object_name __CiType_17_30a4b6a0
  > idm::get_net_from_proto_pin __CiType_17_30a4b6a0
  > idm::object_name __CiType_20_3057fbc8
[CTE::fixup_po_nets]: (I) PO net 'N50' doesn't match PO 'iu_srlz_op_encode(3)' -> attempting to rename

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> idm::locate_net -name iu_srlz_op_encode(3) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fbc8 -name iu_srl...
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
[CTE::fixup_po_nets]: (I) PO net 'N52' doesn't match PO 'iu_srlz_op_encode(4)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(4) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fba0 -name iu_srl...
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
[CTE::fixup_po_nets]: (I) PO net 'N54' doesn't match PO 'iu_srlz_op_encode(5)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(5) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fb78 -name iu_srl...
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
[CTE::fixup_po_nets]: (I) PO net 'N56' doesn't match PO 'iu_srlz_op_encode(6)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(6) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fb50 -name iu_srl...
> idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_20_3057fb28
[CTE::fixup_po_nets]: (I) PO net 'N58' doesn't match PO 'iu_srlz_op_encode(7)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(7) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fb28 -name iu_srl...
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
[CTE::fixup_po_nets]: (I) PO net 'N60' doesn't match PO 'iu_srlz_op_encode(8)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(8) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fb00 -name iu_srl...
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
[CTE::fixup_po_nets]: (I) PO net 'N62' doesn't match PO 'iu_srlz_op_encode(9)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(9) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fad8 -name iu_srl...
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
> idm::object_name __CiType_20_3057fab0
[CTE::fixup_po_nets]: (I) PO net 'N64' doesn't match PO 'iu_srlz_op_encode(10)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(10) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fab0 -name iu_srl...
> idm::object_name __CiType_17_30a4b514
> idm::get_net_from_proto_pin __CiType_17_30a4b514
> idm::object_name __CiType_20_3057fa88
[CTE::fixup_po_nets]: (I) PO net 'N66' doesn't match PO 'iu_srlz_op_encode(11)' -> attempting to rename
> idm::locate_net -name iu_srlz_op_encode(11) -proto_box ___...
> idm::set_net_name -net __CiType_20_3057fa88 -name iu_srl...
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin __CiType_17_30a4b4f0
> idm::object_name __CiType_20_3057f9e8
[CTE::fixup_po_nets]: (I) PO net 'N90' doesn't match PO 'decode_ilc(0)' -> attempting to rename
> idm::locate_net -name decode_ilc(0) -proto_box __CiType_...

```

```

> idm::set_net_name -net __CiType_20_3057f9e8 -name decode...
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
> idm::object_name __CiType_20_3057f9c0
[CTE::fixup_po_nets]: (I) PO net 'N92' doesn't match PO 'decode_ilc(1)' -> attempting to rename
> idm::locate_net -name decode_ilc(1) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f9c0 -name decode...
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin __CiType_17_30a4b4a8
> idm::object_name __CiType_20_3057fd08
[CTE::fixup_po_nets]: (I) PO net 'N30' doesn't match PO 'srlz_actn_tr(0)' -> attempting to rename
> idm::locate_net -name srlz_actn_tr(0) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057fd08 -name srlz_a...
> idm::object_name __CiType_17_30a4b484
> idm::get_net_from_proto_pin __CiType_17_30a4b484
> idm::object_name __CiType_20_3057fce0
[CTE::fixup_po_nets]: (I) PO net 'N32' doesn't match PO 'srlz_actn_tr(1)' -> attempting to rename
> idm::locate_net -name srlz_actn_tr(1) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057fce0 -name srlz_a...
> idm::object_name __CiType_17_30a4b460
> idm::get_net_from_proto_pin __CiType_17_30a4b460
> idm::object_name __CiType_20_3057f5d8
[CTE::fixup_po_nets]: (I) PO net 'N104' doesn't match PO 'intrpt_info_tr(0)' -> attempting to rename
> idm::locate_net -name intrpt_info_tr(0) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f5d8 -name intrpt...
> idm::object_name __CiType_17_30a4b43c
> idm::get_net_from_proto_pin __CiType_17_30a4b43c
> idm::object_name __CiType_20_3057f5b0
[CTE::fixup_po_nets]: (I) PO net 'N106' doesn't match PO 'intrpt_info_tr(1)' -> attempting to rename
> idm::locate_net -name intrpt_info_tr(1) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f5b0 -name intrpt...
> idm::object_name __CiType_17_30a4b418
> idm::get_net_from_proto_pin __CiType_17_30a4b418
> idm::object_name __CiType_20_3057f588
[CTE::fixup_po_nets]: (I) PO net 'N108' doesn't match PO 'intrpt_info_tr(2)' -> attempting to rename
> idm::locate_net -name intrpt_info_tr(2) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f588 -name intrpt...
> idm::object_name __CiType_17_30a4b3f4
> idm::get_net_from_proto_pin __CiType_17_30a4b3f4
> idm::object_name __CiType_20_3057f560
[CTE::fixup_po_nets]: (I) PO net 'N110' doesn't match PO 'intrpt_info_tr(3)' -> attempting to rename
> idm::locate_net -name intrpt_info_tr(3) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f560 -name intrpt...
> idm::object_name __CiType_17_30a4b3d0
> idm::get_net_from_proto_pin __CiType_17_30a4b3d0
> idm::object_name __CiType_20_3057f718
[CTE::fixup_po_nets]: (I) PO net 'N154' doesn't match PO 'op_44_info_tr(0)' -> attempting to rename
> idm::locate_net -name op_44_info_tr(0) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f718 -name op_44_...
> idm::object_name __CiType_17_30a4b3ac
> idm::get_net_from_proto_pin __CiType_17_30a4b3ac
> idm::object_name __CiType_20_3057f6f0
[CTE::fixup_po_nets]: (I) PO net 'N156' doesn't match PO 'op_44_info_tr(1)' -> attempting to rename
> idm::locate_net -name op_44_info_tr(1) -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3057f6f0 -name op_44_...

```

```

> idm::object_name __CiType_17_30a4b364
> idm::get_net_from_proto_pin __CiType_17_30a4b364
> idm::object_name __CiType_20_3057f768
[CTE::fixup_po_nets]: (I) PO net 'N148' doesn't match PO 'dcd_c_cnt(0)' -> attempting to rename
> idm::locate_net -name dcd_c_cnt(0) -proto_box __CiType_1...
> idm::set_net_name -net __CiType_20_3057f768 -name dcd_c_...
> idm::object_name __CiType_17_30a4b340
> idm::get_net_from_proto_pin __CiType_17_30a4b340
> idm::object_name __CiType_20_3057f740
[CTE::fixup_po_nets]: (I) PO net 'N150' doesn't match PO 'dcd_c_cnt(1)' -> attempting to rename
> idm::locate_net -name dcd_c_cnt(1) -proto_box __CiType_1...
> idm::set_net_name -net __CiType_20_3057f740 -name dcd_c_...
> write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report
           for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:09:42 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack Abbreviation Comparison/Description

Slack Continuation	SlkCont	Slack due to a point downstream on path
Required Arrival Time	RAT	(ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time	AsrtRAT	(ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup	ClkGSet	(DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold	ClkGHld	(DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width	ClkTPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup	Setup	(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold	Hold	(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle	EndOfC	(DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth	ClkPW	(CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation	ClkSep	(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop	ALTest	(DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ Failed Test/ P Func	T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	----------------------------------	-------

1 dcd_succ_last_t1

R C3+R 2668 -1669 3294 1011 1 PO

0


```

dcd_succ_last_t1
RAT
999 0
----> BOX714/OUT R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1
----> BOX714/IN R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&0
----> C167/y R C3+R 2668 -1669 3294 1011 1 cs_invvv 01c NOT
0 dcd_succ_last_t1&0
----> C167/a F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT
1594 N675
----> {a} C2738/y F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND
0 N675
----> C2738/a R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND
19 last_cycle
----> {b} C2487/y R C3+R 1056 -1669 33 114 1 cs_nnd2x 14e NAND
0 last_cycle
----> C2487/a F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
21 N1587
----> C1952/y F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
N1587
----> C1952/a R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT R C3+R 1024 -1669 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1)
----> num_dcd_cyl(1) R C3+R 1024 -1669 80 319 1 PI 0
num_dcd_cyl(1)

```

```

2 iu_reset_op_c_t1 R C3+R 2399 -1400 3318 1011 1 PO 0
iu_reset_op_c_t1
RAT
999 0
----> BOX716/OUT R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1
----> BOX716/IN R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0
----> {a} C2393/y R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6
----> gbfonet_6/y F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6
----> gbfonet_6/a R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031
----> {b} C2162/y R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031
----> C2162/a F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/2_out_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1

```

```

--
> load_xrule -file /afs/apd/func/vlsi/alliance00/bssc8/pro...
[BD-450042]: Reading XRULE file '/afs/apd/func/vlsi/alliance00/bssc8/prod/xrule/bssc8.xrule'
[BD-450041]: File '/afs/apd/func/vlsi/alliance00/bssc8/prod/xrule/bssc8.xrule' is being read under VIEW
'XPANDVIEW'
[BD-450037]: (E) (Line 3) Macro proto (M record) of name 'cs_buffe01a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 6) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 9) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 13) Macro proto (M record) of name 'cs_buffe02a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 16) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 19) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 23) Macro proto (M record) of name 'cs_buffe03a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 26) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 29) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 33) Macro proto (M record) of name 'cs_buffe04a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 36) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 39) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 43) Macro proto (M record) of name 'cs_buffe05a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 46) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 49) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 53) Macro proto (M record) of name 'cs_buffe06a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 56) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 59) No currently active macro box (M Record). X Record ignored.
> nextbox synexpand(XPANDVIEW)

```

```

[
>>]: nextbox( synexpand(XPANDVIEW) );
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
> checkfan

```

Electrical Violations in Network 'IDCDSUC'

Fanout		Capacitance	Slew	Sink
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual	
Limit / AdjLim / Actual				
eu_iu_enter_slow_md	-> eu_iu_enter_slow_md		141.00 / 141.00 / 16.73	290.00

/ 290.00 / 352.00 *	12 / 12 / 1 1	
op_inq_stores	-> op_inq_stores	141.00 / 141.00 / 159.72 * 290.00 /
290.00 / 112.00	12 / 12 / 3 1	
eu_iu_mmode	-> eu_iu_mmode	141.00 / 141.00 / 32.56 290.00 /
290.00 / 326.00 *	12 / 12 / 2 1	
du_iu_hold_aa_req	-> du_iu_hold_aa_req	141.00 / 141.00 / 141.99 * 290.00
/ 290.00 / 424.00 *	12 / 12 / 2 1	
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	141.00 / 141.00 / 30.80 290.00 /
290.00 / 339.00 *	12 / 12 / 1 1	
eu_iu_misc_hold	-> eu_iu_misc_hold	141.00 / 141.00 / 19.15 290.00 /
290.00 / 332.00 *	12 / 12 / 1 1	
op_mccend_raw	-> op_mccend_raw	141.00 / 141.00 / 144.35 * 290.00 /
290.00 / 91.00	12 / 12 / 3 1	
clk	-> clk	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00	12 / 12 / 3 1	
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 20.50 290.00 /
290.00 / 338.00 *	12 / 12 / 1 1	
iq_empty	-> iq_empty	141.00 / 141.00 / 170.11 * 290.00 / 290.00
/ 116.00	12 / 12 / 4 1	
gp_tr_scan_in	-> gp_tr_scan_in	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00	12 / 12 / 1 1	
gp_tr_a_clk	-> gp_tr_a_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00	12 / 12 / 1 1	
gp_tr_b_clk	-> gp_tr_b_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00	12 / 12 / 1 1	
clk2	-> clk2	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00	12 / 12 / 3 1	
eu_iu_fxu_exc_cond	-> eu_iu_fxu_exc_cond	141.00 / 141.00 / 15.67 290.00
/ 290.00 / 390.00 *	12 / 12 / 1 1	
du_iu_store_status(2)	-> du_iu_store_status(2)	141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_actn(0)	-> eu_iu_srlz_op_actn(0)	141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 *	12 / 12 / 2 1	
eu_iu_srlz_op_actn(1)	-> eu_iu_srlz_op_actn(1)	141.00 / 141.00 / 47.57 290.00 /
290.00 / 341.00 *	12 / 12 / 2 1	
num_dcd_cyl(1)	-> num_dcd_cyl(1)	141.00 / 141.00 / 318.91 * 290.00 /
290.00 / 80.00	12 / 12 / 1 1	
eu_iu_srlz_op_encode(0)	-> eu_iu_srlz_op_encode(0)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(1)	-> eu_iu_srlz_op_encode(1)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(2)	-> eu_iu_srlz_op_encode(2)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(3)	-> eu_iu_srlz_op_encode(3)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(4)	-> eu_iu_srlz_op_encode(4)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 406.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(5)	-> eu_iu_srlz_op_encode(5)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(6)	-> eu_iu_srlz_op_encode(6)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(7)	-> eu_iu_srlz_op_encode(7)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(8)	-> eu_iu_srlz_op_encode(8)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 *	12 / 12 / 1 1	

```

eu_iu_srlz_op_encode(9)      -> eu_iu_srlz_op_encode(9)      141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 12 / 12 / 1 1
eu_iu_srlz_op_encode(11)    -> eu_iu_srlz_op_encode(11)    141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 * 12 / 12 / 1 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1      78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00      12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1      78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00      12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1      78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59      12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2      78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2      78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3      78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3      78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00      12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL

```

Fanout	Capacitance	Slew	Sink
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual
Limit / AdjLim / Actual			
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4		78.50 / 78.50 / 239.36 *	
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL		
NO_SERIAL			
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL		
NO_SERIAL			
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5		78.50 / 78.50 / 237.91 *	
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL		
NO_SERIAL			
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL		
NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL		
NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1		78.50 / 78.50 / 237.92 *	

```

200.00 / 200.00 / 60.00    12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2          78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00    12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka        78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79    12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
y@C167:cs_invv01c          -> dcd_succ_last_t1&0            70.00 / 70.00 / 1011.00 * 301.00
/ 301.00 / 3294.02 * 12/ 12/ 1 1 KEEP_BTR
y@C1994:cs_invvn01c         -> N1531                        68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02    12/ 12/ 2 2
y@C2013:cs_invvn01c         -> N18&0                       68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3608.92 * 12/ 12/ 1 1
y@C2082:cs_invvn01c         -> N146&0                     68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 * 12/ 12/ 1 1
y@C2194:cs_invvn07c         -> N1681                       261.00 / 261.00 / 271.46 * 290.00 /
290.00 / 261.53    12/ 12/ 7 7
y@C2393:cs_nnd2v02c         -> iu_reset_op_c_t1&0          71.00 / 71.00 / 1044.40 *
290.00 / 290.00 / 3371.12 * 12/ 12/ 3 3
y@C2425:cs_invvn01c         -> N1815                    68.00 / 68.00 / 125.56 * 290.00 /
290.00 / 451.90 * 12/ 12/ 1 1
y@C2496:cs_nnd4n03c         -> N1435                    85.00 / 85.00 / 97.67 * 290.00 /
290.00 / 353.82 * 12/ 12/ 5 5
y@C2646:cs_invvn04c         -> N1645                   133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 275.60    12/ 12/ 6 6
y@C2726:cs_nnd2n11c         -> dsucc_or_agi&0          500.00 / 500.00 / 540.60 *
290.00 / 290.00 / 258.01    12/ 12/ 2 2
y@C2744:cs_invvn13c         -> N2086&0                996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 271.62    12/ 12/ 7 7
y@C2800:cs_invvn08c         -> N1290                   326.00 / 326.00 / 234.15 290.00 /
290.00 / 193.42    12/ 12/ 14 * 14
y@C2728rwr:cs_invvn05c      -> N1097                   167.00 / 167.00 / 183.47 * 290.00 /
290.00 / 266.58    12/ 12/ 4 4
y@C2918:cs_nor2n04c         -> N2016                   110.00 / 110.00 / 132.34 * 290.00 /
290.00 / 428.15 * 12/ 12/ 1 1
y@gbfocell_0:cs_invvn12c    -> gbfonet_0              797.00 / 797.00 / 402.55 290.00 /
290.00 / 149.98    12/ 12/ 20 * 20
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
290.00 / 290.00 / 242.45    12/ 12/ 8 8

```

[BD-500900]: (W) There were 64 electrical violations.
> checkfan

Electrical Violations in Network 'IDCDSUC'

Fanout	Capacitance	Slew	Sink
Pin/Port	Limit / AdjLim / Actual	Limit / AdjLim / Actual	
Limit / AdjLim / Actual			
eu_iu_enter_slow_md -> eu_iu_enter_slow_md	141.00 / 141.00 / 16.73	290.00	
/ 290.00 / 352.00 * 12/ 12/ 1 1			
op_inq_stores -> op_inq_stores	141.00 / 141.00 / 159.72	290.00 /	
290.00 / 112.00 12/ 12/ 3 1			
eu_iu_mmode -> eu_iu_mmode	141.00 / 141.00 / 32.56	290.00 /	

290.00 / 326.00 *	12 / 12 / 2 1	
du_iu_hold_aa_req	-> du_iu_hold_aa_req	141.00 / 141.00 / 141.99 * 290.00
/ 290.00 / 424.00 *	12 / 12 / 2 1	
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	141.00 / 141.00 / 30.80 290.00 /
290.00 / 339.00 *	12 / 12 / 1 1	
eu_iu_misc_hold	-> eu_iu_misc_hold	141.00 / 141.00 / 19.15 290.00 /
290.00 / 332.00 *	12 / 12 / 1 1	
op_mccend_raw	-> op_mccend_raw	141.00 / 141.00 / 144.35 * 290.00 /
290.00 / 91.00	12 / 12 / 3 1	
clkg	-> clkg	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00	12 / 12 / 3 1	
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 20.50 290.00 /
290.00 / 338.00 *	12 / 12 / 1 1	
iq_empty	-> iq_empty	141.00 / 141.00 / 170.11 * 290.00 / 290.00
/ 116.00	12 / 12 / 4 1	
gptr_scan_in	-> gptr_scan_in	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00	12 / 12 / 1 1	
gptr_a_clk	-> gptr_a_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00	12 / 12 / 1 1	
gptr_b_clk	-> gptr_b_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00	12 / 12 / 1 1	
clkg2	-> clkg2	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00	12 / 12 / 3 1	
eu_iu_fxu_exc_cond	-> eu_iu_fxu_exc_cond	141.00 / 141.00 / 15.67 290.00
/ 290.00 / 390.00 *	12 / 12 / 1 1	
du_iu_store_status(2)	-> du_iu_store_status(2)	141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_actn(0)	-> eu_iu_srlz_op_actn(0)	141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 *	12 / 12 / 2 1	
eu_iu_srlz_op_actn(1)	-> eu_iu_srlz_op_actn(1)	141.00 / 141.00 / 47.57 290.00 /
290.00 / 341.00 *	12 / 12 / 2 1	
num_dcd_cyl(1)	-> num_dcd_cyl(1)	141.00 / 141.00 / 318.91 * 290.00 /
290.00 / 80.00	12 / 12 / 1 1	
eu_iu_srlz_op_encode(0)	-> eu_iu_srlz_op_encode(0)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(1)	-> eu_iu_srlz_op_encode(1)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(2)	-> eu_iu_srlz_op_encode(2)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(3)	-> eu_iu_srlz_op_encode(3)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(4)	-> eu_iu_srlz_op_encode(4)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 406.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(5)	-> eu_iu_srlz_op_encode(5)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(6)	-> eu_iu_srlz_op_encode(6)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(7)	-> eu_iu_srlz_op_encode(7)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(8)	-> eu_iu_srlz_op_encode(8)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(9)	-> eu_iu_srlz_op_encode(9)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 *	12 / 12 / 1 1	
eu_iu_srlz_op_encode(11)	-> eu_iu_srlz_op_encode(11)	141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 *	12 / 12 / 1 1	

c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1 78.50 / 78.50 / 220.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1 78.50 / 78.50 / 222.27 *
 200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1 78.50 / 78.50 / 212.39 *
 200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2 78.50 / 78.50 / 239.36 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2 78.50 / 78.50 / 228.73 *
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3 78.50 / 78.50 / 239.37 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL
 c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4 78.50 / 78.50 / 237.92 *
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 NO_SERIAL

		Capacitance	Slew	Sink
Fanout				
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual
	Limit / AdjLim / Actual			
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4		78.50 / 78.50 / 239.36 *		
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL				
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4		78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL				
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5		78.50 / 78.50 / 237.91 *		
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL				
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5		78.50 / 78.50 / 239.37 *		
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL				
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5		78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL				
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1		78.50 / 78.50 / 237.92 *		
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL				
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2		78.50 / 78.50 / 239.37 *		
200.00 / 200.00 / 60.00	12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			

NO_SERIAL

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clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka          78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79    12/   12/   14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
y@C167:cs_invvn01c          -> dcd_succ_last_t1&0          70.00 / 70.00 / 1011.00 * 301.00
/ 301.00 / 3294.02 *    12/   12/    1  1 KEEP_BTR
y@C1994:cs_invvn01c          -> N1531          68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02    12/   12/    2  2
y@C2013:cs_invvn01c          -> N18&0          68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3608.92 *    12/   12/    1  1
y@C2082:cs_invvn01c          -> N146&0          68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 *    12/   12/    1  1
y@C2194:cs_invvn07c          -> N1681          261.00 / 261.00 / 271.46 * 290.00 /
290.00 / 261.53    12/   12/    7  7
y@C2393:cs_nnd2v02c          -> iu_reset_op_c_t1&0          71.00 / 71.00 / 1044.40 *
290.00 / 290.00 / 3371.12 *    12/   12/    3  3
y@C2425:cs_invvn01c          -> N1815          68.00 / 68.00 / 125.56 * 290.00 /
290.00 / 451.90 *    12/   12/    1  1
y@C2496:cs_nnd4n03c          -> N1435          85.00 / 85.00 / 97.67 * 290.00 /
290.00 / 353.82 *    12/   12/    5  5
y@C2646:cs_invvn04c          -> N1645          133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 275.60    12/   12/    6  6
y@C2726:cs_nnd2n11c          -> dsucc_or_agi&0          500.00 / 500.00 / 540.60 *
290.00 / 290.00 / 258.01    12/   12/    2  2
y@C2744:cs_invvn13c          -> N2086&0          996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 271.62    12/   12/    7  7
y@C2800:cs_invvn08c          -> N1290          326.00 / 326.00 / 234.15 290.00 /
290.00 / 193.42    12/   12/   14 * 14
y@C2728rwr:cs_invvn05c          -> N1097          167.00 / 167.00 / 183.47 * 290.00 /
290.00 / 266.58    12/   12/    4  4
y@C2918:cs_nor2n04c          -> N2016          110.00 / 110.00 / 132.34 * 290.00 /
290.00 / 428.15 *    12/   12/    1  1
y@gbfocell_0:cs_invvn12c          -> gbfonet_0          797.00 / 797.00 / 402.55 290.00 /
290.00 / 149.98    12/   12/   20 * 20
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q          247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45    12/   12/    8  8

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[BD-500900]: (W) There were 64 electrical violations.

> nextbox fastslew

[

>>]: nextbox(fastslew);

[BD-500000]: fastslew CMVC version 1.9 compiled on Apr 13 1999 at 18:30:51

[BD-501600]: 7 gates repowered.

> checkfan

Electrical Violations in Network 'IDCDSUC'

Fanout	Capacitance	Slew	Sink
Pin/Port	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual
Limit / AdjLim / Actual	-> Net		
eu_iu_enter_slow_md	-> eu_iu_enter_slow_md	141.00 / 141.00 / 16.73	290.00
/ 290.00 / 352.00 *	12/ 12/ 1 1		
op_inq_stores	-> op_inq_stores	141.00 / 141.00 / 159.72 *	290.00 /
290.00 / 112.00	12/ 12/ 3 1		

eu_iu_mmode	-> eu_iu_mmode	141.00 / 141.00 / 32.56	290.00 /
290.00 / 326.00 *	12 / 12 / 2 1		
du_iu_hold_aa_req	-> du_iu_hold_aa_req	141.00 / 141.00 / 141.99 *	290.00
/ 290.00 / 424.00 *	12 / 12 / 2 1		
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	141.00 / 141.00 / 30.80	290.00 /
290.00 / 339.00 *	12 / 12 / 1 1		
eu_iu_misc_hold	-> eu_iu_misc_hold	141.00 / 141.00 / 19.15	290.00 /
290.00 / 332.00 *	12 / 12 / 1 1		
op_mccend_raw	-> op_mccend_raw	141.00 / 141.00 / 144.35 *	290.00 /
290.00 / 91.00	12 / 12 / 3 1		
clkg	-> clkg	141.00 / 141.00 / 145.52 *	100.00 / 100.00 /
60.00	12 / 12 / 3 1		
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 20.50	290.00 /
290.00 / 338.00 *	12 / 12 / 1 1		
iq_empty	-> iq_empty	141.00 / 141.00 / 170.11 *	290.00 / 290.00
/ 116.00	12 / 12 / 4 1		
gptr_scan_in	-> gptr_scan_in	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /
0.00	12 / 12 / 1 1		
gptr_a_clk	-> gptr_a_clk	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /
0.00	12 / 12 / 1 1		
gptr_b_clk	-> gptr_b_clk	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /
0.00	12 / 12 / 1 1		
clkg2	-> clkg2	141.00 / 141.00 / 145.52 *	100.00 / 100.00 /
60.00	12 / 12 / 3 1		
eu_iu_fxu_exc_cond	-> eu_iu_fxu_exc_cond	141.00 / 141.00 / 15.67	290.00
/ 290.00 / 390.00 *	12 / 12 / 1 1		
du_iu_store_status(2)	-> du_iu_store_status(2)	141.00 / 141.00 / 16.89	290.00 /
290.00 / 500.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_actn(0)	-> eu_iu_srlz_op_actn(0)	141.00 / 141.00 / 47.57	290.00 /
290.00 / 374.00 *	12 / 12 / 2 1		
eu_iu_srlz_op_actn(1)	-> eu_iu_srlz_op_actn(1)	141.00 / 141.00 / 47.57	290.00 /
290.00 / 341.00 *	12 / 12 / 2 1		
num_dcd_cyl(1)	-> num_dcd_cyl(1)	141.00 / 141.00 / 318.91 *	290.00 /
290.00 / 80.00	12 / 12 / 1 1		
eu_iu_srlz_op_encode(0)	-> eu_iu_srlz_op_encode(0)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 401.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(1)	-> eu_iu_srlz_op_encode(1)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 400.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(2)	-> eu_iu_srlz_op_encode(2)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 420.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(3)	-> eu_iu_srlz_op_encode(3)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 302.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(4)	-> eu_iu_srlz_op_encode(4)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 406.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(5)	-> eu_iu_srlz_op_encode(5)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 373.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(6)	-> eu_iu_srlz_op_encode(6)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 354.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(7)	-> eu_iu_srlz_op_encode(7)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 398.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(8)	-> eu_iu_srlz_op_encode(8)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 367.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(9)	-> eu_iu_srlz_op_encode(9)	141.00 / 141.00 / 16.89	
290.00 / 290.00 / 323.00 *	12 / 12 / 1 1		
eu_iu_srlz_op_encode(11)	-> eu_iu_srlz_op_encode(11)	141.00 / 141.00 / 16.89	

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290.00 / 290.00 / 500.00 * 12 / 12 / 1 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1 78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1 78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1 78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2 78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2 78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3 78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3 78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4 78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL

```

Fanout	Capacitance	Slew	Sink
Pin/Port	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual
Limit / AdjLim / Actual	-> Net		
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4	78.50 / 78.50 / 239.36 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4	78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5	78.50 / 78.50 / 237.91 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5	78.50 / 78.50 / 239.37 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5	78.50 / 78.50 / 228.73 *		
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1	78.50 / 78.50 / 237.92 *		
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2	78.50 / 78.50 / 239.37 *		

```

200.00 / 200.00 / 60.00    12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka          78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79    12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
y@C167:cs_invv11e          -> dcd_succ_last_t1&0          638.00 / 638.00 / 1011.00 *
301.00 / 301.00 / 300.47    12 / 12 / 1 1 KEEP_BTR
y@C1994:cs_invvn01c        -> N1531          68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02    12 / 12 / 2 2
y@C2013:cs_invvn12d        -> N18&0          796.00 / 796.00 / 1011.00 * 301.00 /
301.00 / 279.84    12 / 12 / 1 1
y@C2082:cs_invvn12d        -> N146&0          796.00 / 796.00 / 1011.00 * 301.00 /
301.00 / 281.78    12 / 12 / 1 1
y@C2194:cs_invvn07c        -> N1681          261.00 / 261.00 / 271.46 * 290.00 /
290.00 / 261.53    12 / 12 / 7 7
y@C2393:cs_nnd2v13d        -> iu_reset_op_c_t1&0          813.00 / 813.00 / 1044.40 *
290.00 / 290.00 / 267.22    12 / 12 / 3 3
y@C2646:cs_invvn04c        -> N1645          133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 275.60    12 / 12 / 6 6
y@C2726:cs_nnd2n11c        -> dsucc_or_agi&0          500.00 / 500.00 / 540.60 *
290.00 / 290.00 / 258.01    12 / 12 / 2 2
y@C2744:cs_invvn13c        -> N2086&0          996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 269.95    12 / 12 / 7 7
y@C2800:cs_invvn08c        -> N1290          326.00 / 326.00 / 234.15 290.00 /
290.00 / 193.42    12 / 12 / 14 * 14
y@C2728rwr:cs_invvn05c     -> N1097          167.00 / 167.00 / 183.47 * 290.00 /
290.00 / 266.58    12 / 12 / 4 4
y@gbfocell_0:cs_invvn12c   -> gbfontet_0          797.00 / 797.00 / 402.55 290.00 /
290.00 / 149.98    12 / 12 / 20 * 20
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q          247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45    12 / 12 / 8 8

```

[BD-500900]: (W) There were 61 electrical violations.

> write_end_point_report -points 2

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end_point_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:47 1999

Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 2

Cause of Slack Abbreviation Comparison/Description

```

-----
Slack Continuation      SlkCont      Slack due to a point downstream on path
Required Arrival Time    RAT          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup       ClkGSet      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold        ClkGHld      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width   ClkTPW       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

```

TRAILING EDGE)
 Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 ADJUST)
 Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
 ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST)
 Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST)
 Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ Test PinName NetName	LimitedAT/ E Phase	AT	Slack	Slew	CL	FO Cell	Delay/ P Func	Failed Test/ T.Adj
---------------------------------	-----------------------	----	-------	------	----	---------	------------------	-----------------------

1 eu_dsbl_aftr.reg_n.lat_0/a	F C3+R	1761	-448	88	31	1 cl_invvn	07d SRL	
47 N1013								
Setup eu_dsbl_aftr.reg_n.lat_0/c1	F C3-	160		60	221.13	cl_invvn	07d	
1200 slow_mode.c1_1								
---->{a} C2856/y	F C3+R	1761	-448	88	31	1 cs_nnd2n	02c NAND	
0 N1013								
----> C2856/b	R C3+R	1699	-448	104	17	1 cs_nnd2n	02c NAND	
62 N522								
---->{b} C2833/y	R C3+R	1699	-448	104	17	1 cs_nnd2n	02c NAND	
0 N522								
----> C2833/b	F C3+R	1625	-448	129	234	14 cs_nnd2n	02c NAND	
74 N1290								
----> C2800/y	F C3+R	1625	-448	129	234	14 cs_invvn	08c NOT	
0 N1290								
----> C2800/a	R C3+R	1533	-448	170	37	1 cs_invvn	08c NOT	
92 N1648								
---->{c} C2779/y	R C3+R	1533	-448	170	37	1 cs_nnd2n	02c NAND	
0 N1648								
----> C2779/b	F C3+R	1419	-448	164	151	6 cs_nnd2n	02c NAND	
114 N1645								
----> C2646/y	F C3+R	1419	-448	164	151	6 cs_invvn	04c NOT	0
N1645								
----> C2646/a	R C3+R	1305	-448	110	21	1 cs_invvn	04c NOT	
114 N1746								
---->{d} C2620/y	R C3+R	1305	-448	110	21	1 cs_nnd2n	02c NAND	
0 N1746								
----> C2620/a	F C3+R	1230	-448	133	67	4 cs_nnd2n	02c NAND	
75 N1740								
----> C2602/y	F C3+R	1230	-448	133	67	4 cs_invvn	02c NOT	0
N1740								
----> C2602/a	R C3+R	1135	-448	146	37	2 cs_invvn	02c NOT	
95 N905								
---->{e} C2546/y	R C3+R	1135	-448	146	37	2 cs_nnd2n	02c NAND	
0 N905								
----> C2546/a	F C3+R	1045	-448	96	17	1 cs_nnd2n	02c NAND	

```

90 N1647
----> C1928/y          F C3+R   1045  -448   96   17 1 cs_invvn  01c NOT    0
N1647
----> C1928/a          R C3+R    988  -448  390   16 1 cs_invvn  01c NOT    57
eu_iu_fxu_exc_cond&0
----> BOX665/OUT       R C3+R    988  -448  390   16 1 IOPAD    IOPAD
0 eu_iu_fxu_exc_cond&0
----> BOX665/IN       R C3+R    988  -448  390   16 1 IOPAD    IOPAD    0
eu_iu_fxu_exc_cond
----> eu_iu_fxu_exc_cond R C3+R    988  -448  390   16 1 PI          0
eu_iu_fxu_exc_cond
-----
--
2 eu_frc_milli.reg_n.lat_0/a      F C3+R   1761  -448   88   31 1 cl_invvn  07d SRL
47 N994
Setup eu_frc_milli.reg_n.lat_0/c1  F C3-    160          60  238 14 cl_invvn  07d
1200 slow_mode.c1_5
---->{a} C2857/y      F C3+R   1761  -448   88   31 1 cs_nnd2n  02c NAND
0 N994
----> C2857/b        R C3+R   1699  -448  104   17 1 cs_nnd2n  02c NAND
62 N505
---->{b} C2834/y      R C3+R   1699  -448  104   17 1 cs_nnd2n  02c NAND
0 N505
----> C2834/b        F C3+R   1625  -448  129  234 14 cs_nnd2n  02c NAND
74 N1290
----> C2800/y        F C3+R   1625  -448  129  234 14 cs_invvn  08c NOT
0 N1290
----> C2800/a        R C3+R   1533  -448  170   37 1 cs_invvn  08c NOT
92 N1648
---->{c} C2779/y      R C3+R   1533  -448  170   37 1 cs_nnd2n  02c NAND
0 N1648
----> C2779/b        F C3+R   1419  -448  164  151 6 cs_nnd2n  02c NAND
114 N1645
----> C2646/y        F C3+R   1419  -448  164  151 6 cs_invvn  04c NOT    0
N1645
----> C2646/a        R C3+R   1305  -448  110   21 1 cs_invvn  04c NOT
114 N1746
---->{d} C2620/y      R C3+R   1305  -448  110   21 1 cs_nnd2n  02c NAND
0 N1746
----> C2620/a        F C3+R   1230  -448  133   67 4 cs_nnd2n  02c NAND
75 N1740
----> C2602/y        F C3+R   1230  -448  133   67 4 cs_invvn  02c NOT    0
N1740
----> C2602/a        R C3+R   1135  -448  146   37 2 cs_invvn  02c NOT
95 N905
---->{e} C2546/y      R C3+R   1135  -448  146   37 2 cs_nnd2n  02c NAND
0 N905
----> C2546/a        F C3+R   1045  -448   96   17 1 cs_nnd2n  02c NAND
90 N1647
----> C1928/y          F C3+R   1045  -448   96   17 1 cs_invvn  01c NOT    0
N1647
----> C1928/a          R C3+R    988  -448  390   16 1 cs_invvn  01c NOT    57
eu_iu_fxu_exc_cond&0
----> BOX665/OUT       R C3+R    988  -448  390   16 1 IOPAD    IOPAD
0 eu_iu_fxu_exc_cond&0

```

```

----> BOX665/IN          R C3+R   988  -448  390  16 1 IOPAD   IOPAD   0
eu_iu_fxu_exc_cond
----> eu_iu_fxu_exc_cond      R C3+R   988  -448  390  16 1 PI           0
eu_iu_fxu_exc_cond

```

```
--
```

```

> idm::get_active_network
> idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...
> idm::object_name __CiType_17_30aac34c
> idm::get_net_from_proto_pin __CiType_17_30aac34c
> idm::object_name __CiType_20_3057fc90
> idm::object_name __CiType_17_30aac328
> idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
> idm::object_name __CiType_17_30aac304
> idm::get_net_from_proto_pin __CiType_17_30aac304
> idm::object_name __CiType_20_3058f6e0
> idm::object_name __CiType_17_30aac2e0
> idm::get_net_from_proto_pin __CiType_17_30aac2e0
> idm::object_name __CiType_20_3057f6c8
> idm::object_name __CiType_17_30aac2bc
> idm::get_net_from_proto_pin __CiType_17_30aac2bc
> idm::object_name __CiType_20_3057fe48
> idm::object_name __CiType_17_30aac298
> idm::get_net_from_proto_pin __CiType_17_30aac298
> idm::object_name __CiType_20_3059af68
> idm::object_name __CiType_17_30a4bda8
> idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
> idm::object_name __CiType_17_30a4bd84
> idm::get_net_from_proto_pin __CiType_17_30a4bd84
> idm::object_name __CiType_20_3057fd58
> idm::object_name __CiType_17_30a4bd60
> idm::get_net_from_proto_pin __CiType_17_30a4bd60
> idm::object_name __CiType_20_30568e50
> idm::object_name __CiType_17_30a4bd3c
> idm::get_net_from_proto_pin __CiType_17_30a4bd3c
> idm::object_name __CiType_20_3057fcb8
> idm::object_name __CiType_17_30a4bd18
> idm::get_net_from_proto_pin __CiType_17_30a4bd18
> idm::object_name __CiType_20_3057fdf8
> idm::object_name __CiType_17_30a4bcf4
> idm::get_net_from_proto_pin __CiType_17_30a4bcf4
> idm::object_name __CiType_20_3057f6a0
> idm::object_name __CiType_17_30a4bcd0
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
> idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
> idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
> idm::object_name __CiType_20_3057ff60
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64

```

```
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
> idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
> idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
> idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
> idm::object_name __CiType_20_3057fa60
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
> idm::object_name __CiType_20_3057f628
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
> idm::object_name __CiType_20_3057fa38
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
> idm::object_name __CiType_20_3057fc68
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
> idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
> idm::object_name __CiType_20_3057fa10
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
> idm::object_name __CiType_20_3057fd80
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
> idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
> idm::object_name __CiType_20_3057f650
> idm::object_name __CiType_17_30a4ba24
> idm::get_net_from_proto_pin __CiType_17_30a4ba24
> idm::object_name __CiType_20_3057f7b8
> idm::object_name __CiType_17_30a4ba00
> idm::get_net_from_proto_pin __CiType_17_30a4ba00
> idm::object_name __CiType_20_3058fbb8
> idm::object_name __CiType_17_30a4b9dc
> idm::get_net_from_proto_pin __CiType_17_30a4b9dc
> idm::object_name __CiType_20_3059b1c0
> idm::object_name __CiType_17_30a4b9b8
> idm::get_net_from_proto_pin __CiType_17_30a4b9b8
> idm::object_name __CiType_20_3057f808
> idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin __CiType_17_30a4b994
> idm::object_name __CiType_20_3059b648
> idm::object_name __CiType_17_30a4b970
> idm::get_net_from_proto_pin __CiType_17_30a4b970
> idm::object_name __CiType_20_3057fec0
```

```
> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
> idm::object_name __CiType_20_3057fda8
> idm::object_name __CiType_17_30a4b928
> idm::get_net_from_proto_pin __CiType_17_30a4b928
> idm::object_name __CiType_20_3059b7d8
> idm::object_name __CiType_17_30a4b904
> idm::get_net_from_proto_pin __CiType_17_30a4b904
> idm::object_name __CiType_20_3057ff10
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto_pin __CiType_17_30a4b8bc
> idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::get_net_from_proto_pin __CiType_17_30a4b898
> idm::object_name __CiType_20_30590540
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
> idm::object_name __CiType_20_3057fe70
> idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17_30a4b82c
> idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17_30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
> idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17_30a4b7e4
> idm::object_name __CiType_20_3057f948
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
> idm::object_name __CiType_20_3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::get_net_from_proto_pin __CiType_17_30a4b79c
> idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType_17_30a4b778
> idm::object_name __CiType_20_3057f880
> idm::object_name __CiType_17_30a4b754
> idm::get_net_from_proto_pin __CiType_17_30a4b754
> idm::object_name __CiType_20_3057f858
> idm::object_name __CiType_17_30a4b730
> idm::get_net_from_proto_pin __CiType_17_30a4b730
> idm::object_name __CiType_20_3057f830
> idm::object_name __CiType_17_30a4b70c
> idm::get_net_from_proto_pin __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::get_net_from_proto_pin __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
> idm::object_name __CiType_17_30a4b6c4
> idm::get_net_from_proto_pin __CiType_17_30a4b6c4
> idm::object_name __CiType_20_3057fbf0
> idm::object_name __CiType_17_30a4b6a0
```



```
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
> idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
> idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_20_3057fb28
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
> idm::object_name __CiType_20_3057fab0
> idm::object_name __CiType_17_30a4b514
> idm::get_net_from_proto_pin __CiType_17_30a4b514
> idm::object_name __CiType_20_3057fa88
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin __CiType_17_30a4b4f0
> idm::object_name __CiType_20_3057f9e8
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
> idm::object_name __CiType_20_3057f9c0
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin __CiType_17_30a4b4a8
> idm::object_name __CiType_20_3057fd08
> idm::object_name __CiType_17_30a4b484
> idm::get_net_from_proto_pin __CiType_17_30a4b484
> idm::object_name __CiType_20_3057fce0
> idm::object_name __CiType_17_30a4b460
> idm::get_net_from_proto_pin __CiType_17_30a4b460
> idm::object_name __CiType_20_3057f5d8
> idm::object_name __CiType_17_30a4b43c
> idm::get_net_from_proto_pin __CiType_17_30a4b43c
> idm::object_name __CiType_20_3057f5b0
> idm::object_name __CiType_17_30a4b418
> idm::get_net_from_proto_pin __CiType_17_30a4b418
> idm::object_name __CiType_20_3057f588
> idm::object_name __CiType_17_30a4b3f4
> idm::get_net_from_proto_pin __CiType_17_30a4b3f4
> idm::object_name __CiType_20_3057f560
> idm::object_name __CiType_17_30a4b3d0
> idm::get_net_from_proto_pin __CiType_17_30a4b3d0
> idm::object_name __CiType_20_3057f718
> idm::object_name __CiType_17_30a4b3ac
> idm::get_net_from_proto_pin __CiType_17_30a4b3ac
```

```

> idm::object_name __CiType_20_3057f6f0
> idm::object_name __CiType_17_30a4b364
> idm::get_net_from_proto_pin __CiType_17_30a4b364
> idm::object_name __CiType_20_3057f768
> idm::object_name __CiType_17_30a4b340
> idm::get_net_from_proto_pin __CiType_17_30a4b340
> idm::object_name __CiType_20_3057f740
> dfstree {delbrkpt ALL }
> delbrkpt ALL
[delbrkpt]: CMVC version 1.21 compiled on Mar 10 1999 at 05:04:49.
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[delbrkpt]: Removed 180 BRKPT gates
> unpadnet
[unpadnet]: Removed 195 IOPADs.
> idm::get_active_network
> idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...
> idm::object_name __CiType_17_30aac34c
> idm::get_net_from_proto_pin __CiType_17_30aac34c
> idm::object_name __CiType_20_3057fc90
> idm::object_name __CiType_17_30aac328
> idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
> idm::object_name __CiType_17_30aac304
> idm::get_net_from_proto_pin __CiType_17_30aac304
> idm::object_name __CiType_20_3058f6e0
> idm::object_name __CiType_17_30aac2e0
> idm::get_net_from_proto_pin __CiType_17_30aac2e0
> idm::object_name __CiType_20_3057f6c8
> idm::object_name __CiType_17_30aac2bc
> idm::get_net_from_proto_pin __CiType_17_30aac2bc
> idm::object_name __CiType_20_3057fe48
> idm::object_name __CiType_17_30aac298
> idm::get_net_from_proto_pin __CiType_17_30aac298
> idm::object_name __CiType_20_3059af68
> idm::object_name __CiType_17_30a4bda8
> idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
> idm::object_name __CiType_17_30a4bd84
> idm::get_net_from_proto_pin __CiType_17_30a4bd84
> idm::object_name __CiType_20_3057fd58
> idm::object_name __CiType_17_30a4bd60
> idm::get_net_from_proto_pin __CiType_17_30a4bd60
> idm::object_name __CiType_20_30568e50
> idm::object_name __CiType_17_30a4bd3c
> idm::get_net_from_proto_pin __CiType_17_30a4bd3c
> idm::object_name __CiType_20_3057fcb8
> idm::object_name __CiType_17_30a4bd18
> idm::get_net_from_proto_pin __CiType_17_30a4bd18
> idm::object_name __CiType_20_3057fdf8
> idm::object_name __CiType_17_30a4bcf4
> idm::get_net_from_proto_pin __CiType_17_30a4bcf4

```

```
> idm::object_name __CiType_20_3057f6a0
> idm::object_name __CiType_17_30a4bcd0
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
> idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
> idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
> idm::object_name __CiType_20_3057ff60
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
> idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
> idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
> idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
> idm::object_name __CiType_20_3057fa60
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
> idm::object_name __CiType_20_3057f628
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
> idm::object_name __CiType_20_3057fa38
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
> idm::object_name __CiType_20_3057fc68
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
> idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
> idm::object_name __CiType_20_3057fa10
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
> idm::object_name __CiType_20_3057fd80
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
> idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
> idm::object_name __CiType_20_3057f650
> idm::object_name __CiType_17_30a4ba24
> idm::get_net_from_proto_pin __CiType_17_30a4ba24
> idm::object_name __CiType_20_3057f7b8
> idm::object_name __CiType_17_30a4ba00
> idm::get_net_from_proto_pin __CiType_17_30a4ba00
> idm::object_name __CiType_20_3058fbb8
```

```
> idm::object_name __CiType_17_30a4b9dc
> idm::get_net_from_proto_pin __CiType_17_30a4b9dc
> idm::object_name __CiType_20_3059b1c0
> idm::object_name __CiType_17_30a4b9b8
> idm::get_net_from_proto_pin __CiType_17_30a4b9b8
> idm::object_name __CiType_20_3057f808
> idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin __CiType_17_30a4b994
> idm::object_name __CiType_20_3059b648
> idm::object_name __CiType_17_30a4b970
> idm::get_net_from_proto_pin __CiType_17_30a4b970
> idm::object_name __CiType_20_3057fec0
> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
> idm::object_name __CiType_20_3057fda8
> idm::object_name __CiType_17_30a4b928
> idm::get_net_from_proto_pin __CiType_17_30a4b928
> idm::object_name __CiType_20_3059b7d8
> idm::object_name __CiType_17_30a4b904
> idm::get_net_from_proto_pin __CiType_17_30a4b904
> idm::object_name __CiType_20_3057ff10
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto_pin __CiType_17_30a4b8bc
> idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::get_net_from_proto_pin __CiType_17_30a4b898
> idm::object_name __CiType_20_30590540
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
> idm::object_name __CiType_20_3057fe70
> idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17_30a4b82c
> idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17_30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
> idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17_30a4b7e4
> idm::object_name __CiType_20_3057f948
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
> idm::object_name __CiType_20_3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::get_net_from_proto_pin __CiType_17_30a4b79c
> idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType_17_30a4b778
> idm::object_name __CiType_20_3057f880
> idm::object_name __CiType_17_30a4b754
> idm::get_net_from_proto_pin __CiType_17_30a4b754
> idm::object_name __CiType_20_3057f858
> idm::object_name __CiType_17_30a4b730
```

```
> idm::get_net_from_proto_pin __CiType_17_30a4b730
> idm::object_name __CiType_20_3057f830
> idm::object_name __CiType_17_30a4b70c
> idm::get_net_from_proto_pin __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::get_net_from_proto_pin __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
> idm::object_name __CiType_17_30a4b6c4
> idm::get_net_from_proto_pin __CiType_17_30a4b6c4
> idm::object_name __CiType_20_3057fbf0
> idm::object_name __CiType_17_30a4b6a0
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
> idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
> idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_20_3057fb28
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
> idm::object_name __CiType_20_3057fab0
> idm::object_name __CiType_17_30a4b514
> idm::get_net_from_proto_pin __CiType_17_30a4b514
> idm::object_name __CiType_20_3057fa88
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin __CiType_17_30a4b4f0
> idm::object_name __CiType_20_3057f9e8
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
> idm::object_name __CiType_20_3057f9c0
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin __CiType_17_30a4b4a8
> idm::object_name __CiType_20_3057fd08
> idm::object_name __CiType_17_30a4b484
> idm::get_net_from_proto_pin __CiType_17_30a4b484
> idm::object_name __CiType_20_3057fce0
> idm::object_name __CiType_17_30a4b460
> idm::get_net_from_proto_pin __CiType_17_30a4b460
> idm::object_name __CiType_20_3057fd8
> idm::object_name __CiType_17_30a4b43c
> idm::get_net_from_proto_pin __CiType_17_30a4b43c
```

```

> idm::object_name __CiType_20_3057f5b0
> idm::object_name __CiType_17_30a4b418
> idm::get_net_from_proto_pin __CiType_17_30a4b418
> idm::object_name __CiType_20_3057f588
> idm::object_name __CiType_17_30a4b3f4
> idm::get_net_from_proto_pin __CiType_17_30a4b3f4
> idm::object_name __CiType_20_3057f560
> idm::object_name __CiType_17_30a4b3d0
> idm::get_net_from_proto_pin __CiType_17_30a4b3d0
> idm::object_name __CiType_20_3057f718
> idm::object_name __CiType_17_30a4b3ac
> idm::get_net_from_proto_pin __CiType_17_30a4b3ac
> idm::object_name __CiType_20_3057f6f0
> idm::object_name __CiType_17_30a4b364
> idm::get_net_from_proto_pin __CiType_17_30a4b364
> idm::object_name __CiType_20_3057f768
> idm::object_name __CiType_17_30a4b340
> idm::get_net_from_proto_pin __CiType_17_30a4b340
> idm::object_name __CiType_20_3057f740
> sweep
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 754 signals, 531 usage boxes and 1369 connections.
> checkfan

```

Electrical Violations in Network 'IDCDSUC'

Fanout		Capacitance		Slew		Sink	
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual	Limit / AdjLim / Actual
eu_iu_enter_slow_md	-> eu_iu_enter_slow_md	290.00 / 352.00 *	12 / 12 / 1 1	141.00 / 141.00 / 16.73	290.00 /		
op_inq_stores	-> op_inq_stores	290.00 / 112.00	12 / 12 / 3 3	141.00 / 141.00 / 159.72 *	290.00 /		
eu_iu_mmode	-> eu_iu_mmode	290.00 / 326.00 *	12 / 12 / 2 2	141.00 / 141.00 / 32.56	290.00 /		
du_iu_hold_aa_req	-> du_iu_hold_aa_req	290.00 / 424.00 *	12 / 12 / 2 2	141.00 / 141.00 / 141.99 *	290.00		
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	290.00 / 339.00 *	12 / 12 / 1 1	141.00 / 141.00 / 30.80	290.00 /		
eu_iu_misc_hold	-> eu_iu_misc_hold	290.00 / 332.00 *	12 / 12 / 1 1	141.00 / 141.00 / 19.15	290.00 /		
op_mccend_raw	-> op_mccend_raw	290.00 / 91.00	12 / 12 / 3 3	141.00 / 141.00 / 144.35 *	290.00 /		
clkg	-> clkg	60.00	12 / 12 / 3 3	141.00 / 141.00 / 145.52 *	100.00 / 100.00 /		
du_iu_quiesced	-> du_iu_quiesced	290.00 / 338.00 *	12 / 12 / 1 1	141.00 / 141.00 / 20.50	290.00 /		
iq_empty	-> iq_empty	116.00	12 / 12 / 4 4	141.00 / 141.00 / 170.11 *	290.00 / 290.00		
gptr_scan_in	-> gptr_scan_in	0.00	12 / 12 / 1 1	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /		
gptr_a_clk	-> gptr_a_clk	0.00	12 / 12 / 1 1	141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /		
gptr_b_clk	-> gptr_b_clk			141.00 / 141.00 / 1011.00 *	0.00 / 0.00 /		

```

0.00    12/ 12/ 1 1
clk2          -> clk2          141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00    12/ 12/ 3 3
eu_iu_fxu_exc_cond      -> eu_iu_fxu_exc_cond      141.00 / 141.00 / 15.67 290.00
/ 290.00 / 390.00 * 12/ 12/ 1 1
du_iu_store_status(2)    -> du_iu_store_status(2)    141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 * 12/ 12/ 1 1
eu_iu_srlz_op_actn(0)    -> eu_iu_srlz_op_actn(0)    141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 * 12/ 12/ 2 2
eu_iu_srlz_op_actn(1)    -> eu_iu_srlz_op_actn(1)    141.00 / 141.00 / 47.57 290.00 /
290.00 / 341.00 * 12/ 12/ 2 2
num_dcd_cyl(1)          -> num_dcd_cyl(1)          141.00 / 141.00 / 318.91 * 290.00 /
290.00 / 80.00 12/ 12/ 1 1
eu_iu_srlz_op_encode(0)  -> eu_iu_srlz_op_encode(0)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(1)  -> eu_iu_srlz_op_encode(1)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(2)  -> eu_iu_srlz_op_encode(2)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(3)  -> eu_iu_srlz_op_encode(3)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(4)  -> eu_iu_srlz_op_encode(4)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 406.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(5)  -> eu_iu_srlz_op_encode(5)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(6)  -> eu_iu_srlz_op_encode(6)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(7)  -> eu_iu_srlz_op_encode(7)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(8)  -> eu_iu_srlz_op_encode(8)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(9)  -> eu_iu_srlz_op_encode(9)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 12/ 12/ 1 1
eu_iu_srlz_op_encode(11) -> eu_iu_srlz_op_encode(11)  141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 * 12/ 12/ 1 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1      78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00 12/ 12/ 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1      78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00 12/ 12/ 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1    78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 12/ 12/ 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2      78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3      78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12/ 12/ 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL

```

NO_SERIAL

c2@slow_mode.clockblock_2:cb_clk_32 -> slow_mode.c2_3 78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL

NO_SERIAL

clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL

NO_SERIAL

c1@slow_mode.clockblock_3:cb_clk_32 -> slow_mode.c1_4 78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL

NO_SERIAL

Fanout	Capacitance	Slew	Sink
Pin/Port	-> Net	Limit / AdjLim / Actual	Limit / AdjLim / Actual
Limit / AdjLim / Actual			
c2@slow_mode.clockblock_3:cb_clk_32 -> slow_mode.c2_4		78.50 / 78.50 / 239.36 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_4:cb_clk_32 -> slow_mode.c1_5		78.50 / 78.50 / 237.91 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_4:cb_clk_32 -> slow_mode.c2_5		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c1@slow_mode.clockblock_5:cb_clk_32 -> slow_mode.c1		78.50 / 78.50 / 237.92 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
c2@slow_mode.clockblock_5:cb_clk_32 -> slow_mode.c2		78.50 / 78.50 / 239.37 *	
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka		78.50 / 78.50 / 228.73 *	
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL			
NO_SERIAL			
y@C167:cs_invv11e -> dcd_succ_last_t1		638.00 / 638.00 / 1011.00 *	
301.00 / 301.00 / 300.47 12 / 12 / 1 1 KEEP_BTR			
y@C1994:cs_invvn01c -> N1531		68.00 / 68.00 / 77.40 * 290.00 /	
290.00 / 286.02 12 / 12 / 2 2			
y@C2013:cs_invvn12d -> iu_slow_mode_t1		796.00 / 796.00 / 1011.00 *	
301.00 / 301.00 / 279.84 12 / 12 / 1 1			
y@C2082:cs_invvn12d -> idcdsuc_err		796.00 / 796.00 / 1011.00 * 301.00	
/ 301.00 / 281.78 12 / 12 / 1 1			
y@C2194:cs_invvn07c -> N1681		261.00 / 261.00 / 271.46 * 290.00 /	
290.00 / 261.53 12 / 12 / 7 7			
y@C2393:cs_nnd2v13d -> iu_reset_op_c_t1		813.00 / 813.00 / 1044.40 *	
290.00 / 290.00 / 267.22 12 / 12 / 3 3			
y@C2646:cs_invvn04c -> N1645		133.00 / 133.00 / 150.69 * 290.00 /	
290.00 / 275.60 12 / 12 / 6 6			
y@C2726:cs_nnd2n11c -> dsucc_or_agi		500.00 / 500.00 / 540.60 * 290.00	
/ 290.00 / 258.01 12 / 12 / 2 2			

y@C2744:cs_invvn13c	-> dcd_succ_last	996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 269.95	12 / 12 / 7 7	
y@C2800:cs_invvn08c	-> N1290	326.00 / 326.00 / 234.15 290.00 /
290.00 / 193.42	12 / 12 / 14 * 14	
y@C2728rwr:cs_invvn05c	-> N1097	167.00 / 167.00 / 183.47 * 290.00 /
290.00 / 266.58	12 / 12 / 4 4	
y@gbfocell_0:cs_invvn12c	-> gbfonet_0	797.00 / 797.00 / 402.55 290.00 /
290.00 / 149.98	12 / 12 / 20 * 20	
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q		247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45	12 / 12 / 8 8	

[BD-500900]: (W) There were 61 electrical violations.

> source cte_timing_reports.tcl

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_timing_reports.tcl

> summary_report -file /afs/apd/func/vlsi/alliance00/timin...

[measure]: Execution time was 0.0 seconds.

> write_histogram_report -file /afs/apd/func/vlsi/alliance...

[ET-0018]: >Begin...Histogram Report

for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.histogram.

[ET-0019]: <End.....Histogram Report.

> write_checks_report -file /afs/apd/func/vlsi/alliance00/...

[ET-0018]: >Begin...Checks Report

for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.check.

[ET-0916]: No User Define Setup Tests.

[ET-0916]: No User Define Hold Tests.

[ET-0917]: No Clock Pulse Width Tests.

[ET-0918]: No Clock Separation Tests.

[ET-0919]: No End Of Cycle Tests.

[ET-0922]: No Loop Tests.

[ET-0915]: No User Defined Required Arrival Times Late Tests.

[ET-0915]: No User Defined Required Arrival Times Early Tests.

[ET-0916]: No Abstract Tests.

[ET-0019]: <End.....Checks Report.

> write_end_point_report -file /afs/apd/func/vlsi/alliance...

[ET-0018]: >Begin...New EndPoint Report

for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.endpoint.

[ET-0019]: <End.....New Endpoint Report.

> write_net_report -late -file /afs/apd/func/vlsi/alliance...

[ET-0018]: >Begin...Nets Report

for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.net.

[ET-0019]: <End.....Nets Report.

> write_comprehensive_report -file /afs/apd/func/vlsi/alli...

[ET-0018]: >Begin...Comprehensive Report
for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.comp.
[ET-0019]: <End.....Comprehensive Report.

> write_audit_report -file /afs/apd/func/vlsi/alliance00/t...
[ET-0018]: >Begin...Generate Audit Report
for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.audit.
[ET-0019]: <End.....Generate Audit Report.

> CTE::writeverilog {FILE(/afs/apd/func/vlsi/alliance00/ti...
[writeverilog]: Release 1.0 Compiled on Jan 7 1999 at 18:31:22.
[writeverilog]: Writing out the proto for IDCDSUC
[writeverilog]: Writing out the proto for IDCDSUC in top proto IDCDSUC
> source cte_bd2epic
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_bd2epic.tcl
> unpadnet
[unpadnet]: Removed 0 IOPADs.
> idm::get_active_network
> idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...
> idm::object_name __CiType_17_30aac34c
> idm::get_net_from_proto_pin __CiType_17_30aac34c
> idm::object_name __CiType_20_3057fc90
> idm::object_name __CiType_17_30aac328
> idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
> idm::object_name __CiType_17_30aac304
> idm::get_net_from_proto_pin __CiType_17_30aac304
> idm::object_name __CiType_20_3058f6e0
> idm::object_name __CiType_17_30aac2e0
> idm::get_net_from_proto_pin __CiType_17_30aac2e0
> idm::object_name __CiType_20_3057f6c8
> idm::object_name __CiType_17_30aac2bc
> idm::get_net_from_proto_pin __CiType_17_30aac2bc
> idm::object_name __CiType_20_3057fe48
> idm::object_name __CiType_17_30aac298
> idm::get_net_from_proto_pin __CiType_17_30aac298
> idm::object_name __CiType_20_3059af68
> idm::object_name __CiType_17_30a4bda8
> idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
> idm::object_name __CiType_17_30a4bd84
> idm::get_net_from_proto_pin __CiType_17_30a4bd84
> idm::object_name __CiType_20_3057fd58
> idm::object_name __CiType_17_30a4bd60
> idm::get_net_from_proto_pin __CiType_17_30a4bd60
> idm::object_name __CiType_20_30568e50
> idm::object_name __CiType_17_30a4bd3c
> idm::get_net_from_proto_pin __CiType_17_30a4bd3c
> idm::object_name __CiType_20_3057fcb8
> idm::object_name __CiType_17_30a4bd18
> idm::get_net_from_proto_pin __CiType_17_30a4bd18
> idm::object_name __CiType_20_3057fdf8
> idm::object_name __CiType_17_30a4bcf4
> idm::get_net_from_proto_pin __CiType_17_30a4bcf4
> idm::object_name __CiType_20_3057f6a0

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> idm::object_name __CiType_17_30a4bcd0
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
> idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
> idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
> idm::object_name __CiType_20_3057ff60
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
> idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
> idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
> idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
> idm::object_name __CiType_20_3057fa60
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
> idm::object_name __CiType_20_3057f628
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
> idm::object_name __CiType_20_3057fa38
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
> idm::object_name __CiType_20_3057fc68
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
> idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
> idm::object_name __CiType_20_3057fa10
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
> idm::object_name __CiType_20_3057fd80
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
> idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
> idm::object_name __CiType_20_3057f650
> idm::object_name __CiType_17_30a4ba24
> idm::get_net_from_proto_pin __CiType_17_30a4ba24
> idm::object_name __CiType_20_3057f7b8
> idm::object_name __CiType_17_30a4ba00
> idm::get_net_from_proto_pin __CiType_17_30a4ba00
> idm::object_name __CiType_20_3058fbb8
> idm::object_name __CiType_17_30a4b9dc
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> idm::get_net_from_proto_pin __CiType_17_30a4b9dc
> idm::object_name __CiType_20_3059b1c0
> idm::object_name __CiType_17_30a4b9b8
> idm::get_net_from_proto_pin __CiType_17_30a4b9b8
> idm::object_name __CiType_20_3057f808
> idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin __CiType_17_30a4b994
> idm::object_name __CiType_20_3059b648
> idm::object_name __CiType_17_30a4b970
> idm::get_net_from_proto_pin __CiType_17_30a4b970
> idm::object_name __CiType_20_3057fec0
> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
> idm::object_name __CiType_20_3057fda8
> idm::object_name __CiType_17_30a4b928
> idm::get_net_from_proto_pin __CiType_17_30a4b928
> idm::object_name __CiType_20_3059b7d8
> idm::object_name __CiType_17_30a4b904
> idm::get_net_from_proto_pin __CiType_17_30a4b904
> idm::object_name __CiType_20_3057ff10
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto_pin __CiType_17_30a4b8bc
> idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::get_net_from_proto_pin __CiType_17_30a4b898
> idm::object_name __CiType_20_30590540
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
> idm::object_name __CiType_20_3057fe70
> idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17_30a4b82c
> idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17_30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
> idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17_30a4b7e4
> idm::object_name __CiType_20_3057f948
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
> idm::object_name __CiType_20_3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::get_net_from_proto_pin __CiType_17_30a4b79c
> idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType_17_30a4b778
> idm::object_name __CiType_20_3057f880
> idm::object_name __CiType_17_30a4b754
> idm::get_net_from_proto_pin __CiType_17_30a4b754
> idm::object_name __CiType_20_3057f858
> idm::object_name __CiType_17_30a4b730
> idm::get_net_from_proto_pin __CiType_17_30a4b730
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> idm::object_name __CiType_20_3057f830
> idm::object_name __CiType_17_30a4b70c
> idm::get_net_from_proto_pin __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::get_net_from_proto_pin __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
> idm::object_name __CiType_17_30a4b6c4
> idm::get_net_from_proto_pin __CiType_17_30a4b6c4
> idm::object_name __CiType_20_3057fbf0
> idm::object_name __CiType_17_30a4b6a0
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
> idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
> idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_20_3057fb28
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
> idm::object_name __CiType_20_3057fab0
> idm::object_name __CiType_17_30a4b514
> idm::get_net_from_proto_pin __CiType_17_30a4b514
> idm::object_name __CiType_20_3057fa88
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin __CiType_17_30a4b4f0
> idm::object_name __CiType_20_3057f9e8
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
> idm::object_name __CiType_20_3057f9c0
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin __CiType_17_30a4b4a8
> idm::object_name __CiType_20_3057fd08
> idm::object_name __CiType_17_30a4b484
> idm::get_net_from_proto_pin __CiType_17_30a4b484
> idm::object_name __CiType_20_3057fce0
> idm::object_name __CiType_17_30a4b460
> idm::get_net_from_proto_pin __CiType_17_30a4b460
> idm::object_name __CiType_20_3057f5d8
> idm::object_name __CiType_17_30a4b43c
> idm::get_net_from_proto_pin __CiType_17_30a4b43c
> idm::object_name __CiType_20_3057f5b0
```

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> idm::object_name __CiType_17_30a4b418
> idm::get_net_from_proto_pin __CiType_17_30a4b418
> idm::object_name __CiType_20_3057f588
> idm::object_name __CiType_17_30a4b3f4
> idm::get_net_from_proto_pin __CiType_17_30a4b3f4
> idm::object_name __CiType_20_3057f560
> idm::object_name __CiType_17_30a4b3d0
> idm::get_net_from_proto_pin __CiType_17_30a4b3d0
> idm::object_name __CiType_20_3057f718
> idm::object_name __CiType_17_30a4b3ac
> idm::get_net_from_proto_pin __CiType_17_30a4b3ac
> idm::object_name __CiType_20_3057f6f0
> idm::object_name __CiType_17_30a4b364
> idm::get_net_from_proto_pin __CiType_17_30a4b364
> idm::object_name __CiType_20_3057f768
> idm::object_name __CiType_17_30a4b340
> idm::get_net_from_proto_pin __CiType_17_30a4b340
> idm::object_name __CiType_20_3057f740
> delbrkpt ALL
[
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[delbrkpt]: Removed 0 BRKPT gates
> cleanse
Removed 0 boxes[sweep]: sweep deleted 2 signals and 0 usage boxes.
The model has 754 signals, 531 usage boxes and 1369 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 754 signals, 531 usage boxes and 1369 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
The model has 754 signals, 531 usage boxes and 1369 connections.
[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
> timing_reset
[timing_reset]: Timing has been reset.
> write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.

```

Sun Apr 18 22:10:04 1999

Part : IDCDSUC

Mode : Late Mode / Nominal

EDA EinsTimer EndPoint Report

Release Level : 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack

Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path
Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME)
Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST)
Clock Gating Hold ClkGHld (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST)
Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST)
Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST)
EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth ClkPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE)
ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST)
Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ LimitedAT/ Delay/ Failed Test/
Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj
NetName

1 xeu_dsbl_aftr_reg_n_lat_0/a F C3+R 1761 -448 88 31 1 cl_invvn 07d SRL
47 n1013
Setup xeu_dsbl_aftr_reg_n_lat_0/c1 F C3- 160 60 221 13 cl_invvn 07d
1200 slow_mode.c1_1
---->{a} xc2856/y F C3+R 1761 -448 88 31 1 cs_nnd2n 02c NAND
0 n1013
----> xc2856/b R C3+R 1699 -448 104 17 1 cs_nnd2n 02c NAND
62 n522
---->{b} xc2833/y R C3+R 1699 -448 104 17 1 cs_nnd2n 02c NAND
0 n522
----> xc2833/b F C3+R 1625 -448 129 234 14 cs_nnd2n 02c NAND
74 n1290
----> xc2800/y F C3+R 1625 -448 129 234 14 cs_invvn 08c NOT
0 n1290
----> xc2800/a R C3+R 1533 -448 170 37 1 cs_invvn 08c NOT
92 n1648
---->{c} xc2779/y R C3+R 1533 -448 170 37 1 cs_nnd2n 02c NAND
0 n1648

----> xc2779/b 114 n1645	F C3+R	1419	-448	164	151	6	cs_nnd2n	02c	NAND	
----> xc2646/y 0 n1645	F C3+R	1419	-448	164	151	6	cs_invvn	04c	NOT	
----> xc2646/a 114 n1746	R C3+R	1305	-448	110	21	1	cs_invvn	04c	NOT	
---->{d} xc2620/y 0 n1746	R C3+R	1305	-448	110	21	1	cs_nnd2n	02c	NAND	
----> xc2620/a 75 n1740	F C3+R	1230	-448	133	67	4	cs_nnd2n	02c	NAND	
----> xc2602/y n1740	F C3+R	1230	-448	133	67	4	cs_invvn	02c	NOT	0
----> xc2602/a 95 n905	R C3+R	1135	-448	146	37	2	cs_invvn	02c	NOT	
---->{e} xc2546/y 0 n905	R C3+R	1135	-448	146	37	2	cs_nnd2n	02c	NAND	
----> xc2546/a 90 n1647	F C3+R	1045	-448	96	17	1	cs_nnd2n	02c	NAND	
----> xc1928/y n1647	F C3+R	1045	-448	96	17	1	cs_invvn	01c	NOT	0
----> xc1928/a 57 eu_iu_fxu_exc_cond	R C3+R	988	-448	390	16	1	cs_invvn	01c	NOT	
----> eu_iu_fxu_exc_cond eu_iu_fxu_exc_cond	R C3+R	988	-448	390	16	1	PI			0

2 xeu_frc_milli_reg_n_lat_0/a 47 n994	F C3+R	1761	-448	88	31	1	cl_invvn	07d	SRL	
Setup xeu_frc_milli_reg_n_lat_0/c1 1200 slow_mode.c1_5	F C3-	160		60	238	14	cl_invvn	07d		
---->{a} xc2857/y 0 n994	F C3+R	1761	-448	88	31	1	cs_nnd2n	02c	NAND	
----> xc2857/b 62 n505	R C3+R	1699	-448	104	17	1	cs_nnd2n	02c	NAND	
---->{b} xc2834/y 0 n505	R C3+R	1699	-448	104	17	1	cs_nnd2n	02c	NAND	
----> xc2834/b 74 n1290	F C3+R	1625	-448	129	234	14	cs_nnd2n	02c	NAND	
----> xc2800/y 0 n1290	F C3+R	1625	-448	129	234	14	cs_invvn	08c	NOT	
----> xc2800/a 92 n1648	R C3+R	1533	-448	170	37	1	cs_invvn	08c	NOT	
---->{c} xc2779/y 0 n1648	R C3+R	1533	-448	170	37	1	cs_nnd2n	02c	NAND	
----> xc2779/b 114 n1645	F C3+R	1419	-448	164	151	6	cs_nnd2n	02c	NAND	
----> xc2646/y 0 n1645	F C3+R	1419	-448	164	151	6	cs_invvn	04c	NOT	
----> xc2646/a 114 n1746	R C3+R	1305	-448	110	21	1	cs_invvn	04c	NOT	
---->{d} xc2620/y 0 n1746	R C3+R	1305	-448	110	21	1	cs_nnd2n	02c	NAND	
----> xc2620/a 75 n1740	F C3+R	1230	-448	133	67	4	cs_nnd2n	02c	NAND	
----> xc2602/y	F C3+R	1230	-448	133	67	4	cs_invvn	02c	NOT	0


```

n1740
----> xc2602/a          R C3+R   1135  -448   146   37 2 cs_invrn  02c NOT
95 n905
----> {e} xc2546/y      R C3+R   1135  -448   146   37 2 cs_nnd2n  02c NAND
0 n905
----> xc2546/a          F C3+R   1045  -448    96   17 1 cs_nnd2n  02c NAND
90 n1647
----> xc1928/y          F C3+R   1045  -448    96   17 1 cs_invrn  01c NOT    0
n1647
----> xc1928/a          R C3+R    988  -448   390   16 1 cs_invrn  01c NOT
57 eu_iu_fxu_exc_cond
----> eu_iu_fxu_exc_cond R C3+R    988  -448   390   16 1 PI          0
eu_iu_fxu_exc_cond

```

```

---
[CTE::cte_bd2epic]: pathmill_options: -b 3 -u -p

```

```

/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill%/afs/apd/func/vlsi/alliance00/local/cmos8s/cm
os8s.pathmill.early -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c

```

```

[CTE::cte_bd2epic]: bd2epic_options:

```

```

ASSERT(/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/IDCDSUC.assert)
WLCOUNT_CAP(/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/IDCDSUC.nodeca
p) WLCOUNT_CAP_NODES() WIRE_CAP_CASE() PM_OPTIONS(-b 3 -u -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill%/afs/apd/func/vlsi/alliance00/local/cmos8s/cm
os8s.pathmill.early -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c)

```

```

> CTE::bd2epic { NETLIST(/afs/apd/func/vlsi/alliance00/tim...

```

```

[bd2epic]: Release 1.2 Compiled on Jan 29 1999 at 16:19:04.

```

```

[bd2epic]: Asserting pathmill wire cap based on wlcount table estimates

```

```

[bd2epic]: Pathmill wire cap based on cap values

```

```

[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clk1_mode4) is missing timing information!

```

```

[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clk1_mode5) is missing timing information!

```

```

[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clk1_mode6) is missing timing information!

```

```

[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clk1_mode8) is missing timing information!

```

```

> padnet

```

```

[padnet]: Added 195 IOPADS:

```

```

> idm::get_active_network

```

```

> idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...

```

```

> idm::object_name __CiType_17_30aac34c

```

```

> idm::get_net_from_proto_pin __CiType_17_30aac34c

```

```

> idm::object_name __CiType_20_3057fc90

```

```

> idm::object_name __CiType_17_30aac328

```

```

> idm::get_net_from_proto_pin __CiType_17_30aac328

```

```

> idm::object_name __CiType_20_30590568

```

```

> idm::object_name __CiType_17_30aac304

```

```

> idm::get_net_from_proto_pin __CiType_17_30aac304

```

```

> idm::object_name __CiType_20_3058f6e0

```

```

> idm::object_name __CiType_17_30aac2e0

```

```

> idm::get_net_from_proto_pin __CiType_17_30aac2e0

```

```

> idm::object_name __CiType_20_3057f6c8

```

```

> idm::object_name __CiType_17_30aac2bc

```

```

> idm::get_net_from_proto_pin __CiType_17_30aac2bc

```

```

> idm::object_name __CiType_20_3057fe48

```

```

> idm::object_name __CiType_17_30aac298

```

```

> idm::get_net_from_proto_pin __CiType_17_30aac298

```

```

> idm::object_name __CiType_20_3059af68

```

```

> idm::object_name __CiType_17_30a4bda8

```

```
> idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
> idm::object_name __CiType_17_30a4bd84
> idm::get_net_from_proto_pin __CiType_17_30a4bd84
> idm::object_name __CiType_20_3057fd58
> idm::object_name __CiType_17_30a4bd60
> idm::get_net_from_proto_pin __CiType_17_30a4bd60
> idm::object_name __CiType_20_30568e50
> idm::object_name __CiType_17_30a4bd3c
> idm::get_net_from_proto_pin __CiType_17_30a4bd3c
> idm::object_name __CiType_20_3057fcb8
> idm::object_name __CiType_17_30a4bd18
> idm::get_net_from_proto_pin __CiType_17_30a4bd18
> idm::object_name __CiType_20_3057fdf8
> idm::object_name __CiType_17_30a4bcf4
> idm::get_net_from_proto_pin __CiType_17_30a4bcf4
> idm::object_name __CiType_20_3057f6a0
> idm::object_name __CiType_17_30a4bcd0
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
> idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
> idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
> idm::object_name __CiType_20_3057ff60
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
> idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
> idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
> idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
> idm::object_name __CiType_20_3057fa60
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
> idm::object_name __CiType_20_3057f628
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
> idm::object_name __CiType_20_3057fa38
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
> idm::object_name __CiType_20_3057fc68
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
> idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
```

```

> idm::object_name __CiType_20_3057fa10
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
> idm::object_name __CiType_20_3057fd80
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
> idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
> idm::object_name __CiType_20_3057f650
> idm::object_name __CiType_17_30a4ba24
> idm::get_net_from_proto_pin __CiType_17_30a4ba24
> idm::object_name __CiType_20_3057f7b8
> idm::object_name __CiType_17_30a4ba00
> idm::get_net_from_proto_pin __CiType_17_30a4ba00
> idm::object_name __CiType_20_3058fbb8
> idm::object_name __CiType_17_30a4b9dc
> idm::get_net_from_proto_pin __CiType_17_30a4b9dc
> idm::object_name __CiType_20_3059b1c0
> idm::object_name __CiType_17_30a4b9b8
> idm::get_net_from_proto_pin __CiType_17_30a4b9b8
> idm::object_name __CiType_20_3057f808
> idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin __CiType_17_30a4b994
> idm::object_name __CiType_20_3059b648
> idm::object_name __CiType_17_30a4b970
> idm::get_net_from_proto_pin __CiType_17_30a4b970
> idm::object_name __CiType_20_3057fec0
> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
> idm::object_name __CiType_20_3057fda8
> idm::object_name __CiType_17_30a4b928
> idm::get_net_from_proto_pin __CiType_17_30a4b928
> idm::object_name __CiType_20_3059b7d8
[CTE::fixup_po_nets]: (I) PO net 'gpnr_scan_out&0' doesn't match PO 'gpnr_scan_out' -> attempting to
rename

```

```

> idm::locate_net -name gpnr_scan_out -proto_box __CiType_...
> idm::set_net_name -net __CiType_20_3059b7d8 -name gpnr_s...
> idm::object_name __CiType_17_30a4b904
> idm::get_net_from_proto_pin __CiType_17_30a4b904
> idm::object_name __CiType_20_3057ff10
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto_pin __CiType_17_30a4b8bc
> idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::get_net_from_proto_pin __CiType_17_30a4b898
> idm::object_name __CiType_20_30590540
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
> idm::object_name __CiType_20_3057fe70
> idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17_30a4b82c

```

```
> idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17_30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
> idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17_30a4b7e4
> idm::object_name __CiType_20_3057f948
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
> idm::object_name __CiType_20_3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::get_net_from_proto_pin __CiType_17_30a4b79c
> idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType_17_30a4b778
> idm::object_name __CiType_20_3057f880
> idm::object_name __CiType_17_30a4b754
> idm::get_net_from_proto_pin __CiType_17_30a4b754
> idm::object_name __CiType_20_3057f858
> idm::object_name __CiType_17_30a4b730
> idm::get_net_from_proto_pin __CiType_17_30a4b730
> idm::object_name __CiType_20_3057f830
> idm::object_name __CiType_17_30a4b70c
> idm::get_net_from_proto_pin __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::get_net_from_proto_pin __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
> idm::object_name __CiType_17_30a4b6c4
> idm::get_net_from_proto_pin __CiType_17_30a4b6c4
> idm::object_name __CiType_20_3057fbf0
> idm::object_name __CiType_17_30a4b6a0
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
> idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
> idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_20_3057fb28
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
> idm::object_name __CiType_20_3057fab0
```

```

> idm::object_name __CiType_17_30a4b514
> idm::get_net_from_proto_pin __CiType_17_30a4b514
> idm::object_name __CiType_20_3057fa88
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin __CiType_17_30a4b4f0
> idm::object_name __CiType_20_3057f9e8
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
> idm::object_name __CiType_20_3057f9c0
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin __CiType_17_30a4b4a8
> idm::object_name __CiType_20_3057fd08
> idm::object_name __CiType_17_30a4b484
> idm::get_net_from_proto_pin __CiType_17_30a4b484
> idm::object_name __CiType_20_3057fce0
> idm::object_name __CiType_17_30a4b460
> idm::get_net_from_proto_pin __CiType_17_30a4b460
> idm::object_name __CiType_20_3057f5d8
> idm::object_name __CiType_17_30a4b43c
> idm::get_net_from_proto_pin __CiType_17_30a4b43c
> idm::object_name __CiType_20_3057f5b0
> idm::object_name __CiType_17_30a4b418
> idm::get_net_from_proto_pin __CiType_17_30a4b418
> idm::object_name __CiType_20_3057f588
> idm::object_name __CiType_17_30a4b3f4
> idm::get_net_from_proto_pin __CiType_17_30a4b3f4
> idm::object_name __CiType_20_3057f560
> idm::object_name __CiType_17_30a4b3d0
> idm::get_net_from_proto_pin __CiType_17_30a4b3d0
> idm::object_name __CiType_20_3057f718
> idm::object_name __CiType_17_30a4b3ac
> idm::get_net_from_proto_pin __CiType_17_30a4b3ac
> idm::object_name __CiType_20_3057f6f0
> idm::object_name __CiType_17_30a4b364
> idm::get_net_from_proto_pin __CiType_17_30a4b364
> idm::object_name __CiType_20_3057f768
> idm::object_name __CiType_17_30a4b340
> idm::get_net_from_proto_pin __CiType_17_30a4b340
> idm::object_name __CiType_20_3057f740
> write_vim -library /afs/apd/func/vlsi/alliance00/timing/...
bdz> vim_preexport __CiType_16_30a98de8
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booleadozer/4.1/tcl/constant_support.tcl
    > str_parm one_net_name
    > str_parm zero_net_name
    > is_parm custom_constants_kill_fanout_tree
    > is_parm custom_constants_kill_const_boxes
    > nextbox dot2ms()
[
>>]: nextbox( dot2ms() );
bdz> vim_postexport __CiType_16_30a98de8
    > str_parm one_net_name
    > str_parm zero_net_name
    > is_parm standard_constants_run_tiegen
    > nextnet ms2dot(BUS)
[

```

>>]: nextnet(ms2dot(BUS));
Process took 709.21 cpu seconds or 00:20:19 wall time.
Used 39924388 bytes or 38 megs.
Highest message level was ERROR: 97 WARNING, 65 ERROR.
Return code 0
cte_ci_term

[DCL-17025]: *****
** Start of Limit checking messages **

[DCL-17025]: *****
** End of Limit checking messages **

Info Running Pathmill Model Build
CTE: Initializing for technology cmos8s

WARNING: Overriding technology files by command line parameter.

Preprocessing configuration file epic.inp --> epic.inp.final

Include path for cpp...

/afs/apd/func/vlsi/alliance00/libraries/pathmill/config
/afs/watson/projects/vlsi/cte/tech/cmos8s/base/prod/pathmill/config
/afs/apd/func/vlsi/alliance00/bssc8/prod/cc8s/pathmill/config
/afs/watson/projects/vlsi/cte/tools/epic/5.1/local/pathmill/config

Locating cpp include files for epic.inp...

/afs/apd/func/vlsi/alliance00/libraries/pathmill/config/template.cfg
./IDCDSUC.assert
/afs/apd/func/vlsi/alliance00/libraries/pathmill/config/sets.cfg
./IDCDSUC.nodecap

Executing /usr/ccs/lib/cpp...

Executing PERL: substituting CTE vars and generating node lists...

Preprocessing completed successfully

EXEC /afs/apd/func/vlsi/alliance00/libraries/pathmill/audit/pm_audit_alli00 -U
/afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo
s8s.pathmill.early -x -n netlist -c epic.inp.final -L
/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice -b 3 -u -o build_model

[pm_audit_alli00] Alliance 2000 Pathmill Audit Program (version 0.1)

[pm_audit_alli00] Executed: Sun Apr 18 22:10:20 EDT 1999

[pm_audit_alli00] WARNING -- Specified 2 tech files:

/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill

/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early!

[pm_audit_alli00] CTE environment specifies...

[pm_audit_alli00] technology: cmos8s

[pm_audit_alli00] ibmtech verion: 5.1

[pm_audit_alli00] pathmill install: 5.1

[pm_audit_alli00] Checking netlist file: netlist

[pm_audit_alli00] WARNING -- Netlist is missing technology audit data!
[pm_audit_alli00] Completed successfully

EPIC_CC_OPTIONS is set to: -D_ENABLE_HOOKS -D_ENABLE_HOOKS -D_PROCESS_MODEL

pathmill -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo
s8s.pathmill.early -x -n netlist -c epic.inp.final -L
/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice -b 3 -u -o build_model

Building libCustom.o

#! .epicrun/libCustom.o

if_setup

epic_mti_if_quit_ack

epicState

shm_put_msg

put_msg

ld: 0711-319 WARNING: Exported symbol not defined: estimateDeviceParameters

ld: 0711-319 WARNING: Exported symbol not defined: timemill_user_init

ld: 0711-319 WARNING: Exported symbol not defined: powrmill_user_init

ld: 0711-319 WARNING: Exported symbol not defined: iAreaCap

ld: 0711-319 WARNING: Exported symbol not defined: iDiffCap

ld: 0711-319 WARNING: Exported symbol not defined: iFringeCap

ld: 0711-319 WARNING: Exported symbol not defined: ilnit

ld: 0711-319 WARNING: Exported symbol not defined: m12cc

ld: 0711-319 WARNING: Exported symbol not defined: m12dw

ld: 0711-319 WARNING: Exported symbol not defined: epicUserControl

ld: 0711-319 WARNING: Exported symbol not defined: epicUserMain

ld: 0711-319 WARNING: Exported symbol not defined: epic_mti_if_quit_ack

ld: 0711-319 WARNING: Exported symbol not defined: if_setup

ld: 0711-319 WARNING: Exported symbol not defined: epicState

ld: 0711-319 WARNING: Exported symbol not defined: shm_put_msg

ld: 0711-319 WARNING: Exported symbol not defined: put_msg

Using /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/libCustom.o ...

Notice: License pathmill will expire on 4/30/99.

options:

pathmill -t -c epic.inp.final -p

/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo

s8s.pathmill.early -o build_model -b 3

Simulator execution begins...

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Compiling "netlist"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cb_mode_block.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_mode_block.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_invvn02.spi"

Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oPfet"

Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oNfet"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_invvn.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_lat_core_s.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cb_clk_32_1.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_32_1.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_core.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_se.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_clka.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv11e.spi"

Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oPfetLowVt"

Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oNfetLowVt"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn12c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn09c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn01c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n04c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn15c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn11c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn13c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn19b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn08c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn12d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn04c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n12c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3v02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v13c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2n04c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao12n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_xbn2n01b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor3n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao21n10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n11c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_xbo2n01d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2x14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao12n10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v13d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn06d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n04c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2x14e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4n05d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2x14b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3i11b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4v10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2g14e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4v10b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao21n10e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao12n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n08c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv13b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2g12e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv13c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2n06d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor3v10e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn16c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv09c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2v11c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v11c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2g11b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3z10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn07d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_lat_core_b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_nnd2n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_nnd2n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_ao22n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_ao22n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn06d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn05d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_nnd3n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_nnd3n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_nor2n06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_nor2n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_ao21n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_ao21n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_ao21n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_ao21n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2f03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3z07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4v06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn01e.spi"

PathMill Version 5.1plus
SN: P013098-AIX
Copyright (c) 1997 Synopsys Inc., All Rights Reserved.

Built by olevi in " PM_DEV " on Fri Jan 30 12:01:27 PST 1998

Enabling ibmgray model bulding code.

Warning: invalid command or arguments on line 69 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.
corners 10 1.45

Warning: invalid command or arguments on line 1920 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.
corners 10 1.45

Warning: invalid command or arguments on line 68 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early.
corners -10 1.70

Warning: invalid command or arguments on line 1919 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early.
corners -10 1.70

Done building data structure

CTE Pathmill post-processor: Determining clock nodes to ignore

CTE Pathmill post-processor: Determining pattern files from configuration file

WARNING:PathMill:0x20521001:Node gpтр_scan_out does not exist in netlist

WARNING:PathMill:0x20521001:Node gpтр_scan_out does not exist in netlist

WARNING:PathMill:0x20525001:source_node test_c1 is set to LOW

WARNING:PathMill:0x20525001:source_node scan_in is set to LOW

WARNING:PathMill:0x20521001:Node scan_in<0> does not exist in netlist

WARNING:PathMill:0x20521001:Node scan_in<1> does not exist in netlist

WARNING:PathMill:0x20521001:Node scan_in<2> does not exist in netlist

WARNING:PathMill:0x20525001:source_node a_clk is set to LOW

WARNING:PathMill:0x20525001:source_node b_clk is set to LOW

WARNING:PathMill:0x20525001:source_node clk1_mode7 is set to HIGH

WARNING:PathMill:0x20525001:source_node gpтр_a_clk is set to LOW

WARNING:PathMill:0x20525001:source_node gpтр_b_clk is set to LOW

WARNING:PathMill:0x20525001:source_node gpтр_scan_in is set to LOW

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_P465.IBMtech_P(pf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_P465.IBMtech_P(pf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_N468.IBMtech_N(nf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_N468.IBMtech_N(nf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_P346.IBMtech_P(pf_e
pic) (l=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_P346.IBMtech_P(pf_e
pic) (l=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_N344.IBMtech_N(nf_e
pic) (l=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_N344.IBMtech_N(nf_e
pic) (l=0.65u) is not in tech file

Working in timing verify mode - clock edge reference, turning on the transparent_mode

Unlimited transparency depth

data_to_latch report is on

latch_to_latch report is on

gated_clock report is on

pattern acac_drv2000: 0 matched

pattern invmux: 0 matched

pattern buffer2: 0 matched

pattern zljs_clk_core_padc1: 0 matched

==> ibm_gray: Opened the NT latch pattern list named:

/afs/apd/func/vlsi/alliance00/libraries/pathmill/patterns/nt_latch_pattern_list

pattern zljs_clk_32_1: 6 matched
pattern zljs_clk_core: 6 matched
pattern zljs_clk_corepar: 0 matched
pattern zljs_clk_32_2: 0 matched
pattern zljs_clk_core: 0 matched
pattern zljs_clk_corepar: 0 matched
pattern zljs_clk_32_3: 0 matched
pattern zljs_clk_core3: 0 matched
pattern zljs_clk_core3par: 0 matched
pattern zljs_lat_core_a: 0 matched
pattern zljs_lat_core_b: 83 matched
pattern zljs_lat_core_c: 0 matched
pattern tg: 42 matched
pattern 4ns: 0 matched
pattern 4ps: 9 matched
pattern 2ns: 96 matched
pattern 2ps: 714 matched
pattern 2ns1a: 28 matched
pattern 2ps1a: 104 matched
pattern 2ns1: 32 matched
pattern 2ps1: 32 matched
pattern 2ns2: 118 matched
pattern 2ps2: 40 matched
pattern XN4: 0 matched
pattern XR4: 0 matched
pattern XN3: 0 matched
pattern XR3: 0 matched
pattern XN2: 0 matched
pattern XN2B: 1 matched
pattern XN2BGoofyExtract: 0 matched
pattern XR2: 0 matched
pattern XR2B: 1 matched
build model name idcdsuc_mac

Done reading setup file for build_model characterize.file

pattern zljs_mode_block: 0 matched
pattern zljs_mode_block: 1 matched

Marking Inverters, Latches and RAM cells
Finished Marking Inverters, Latches and RAM cells

Marking Transfer gates
Finished Marking Transfer gates

Setting transistor Directions
The percentage of elements with direction set is (including bi-directional) 100.00%.
Clock Propagation Begins
Clock Propagation End
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<4>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<4>.l1_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock

xgptr_latch.X_mb.X_mode<5>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<5>.l1_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<6>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<6>.l1_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<7>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<7>.l1_n

*** start calculating MAX clock skew ***

start propagating clock information for node clk_g
stop propagating clock information from node clk_g

start propagating clock information for node clk_{g2}
stop propagating clock information from node clk_{g2}

*** finished calculating MAX clock skew ***

*** start calculating MIN clock skew ***

start propagating clock information for node clk_g
stop propagating clock information from node clk_g

start propagating clock information for node clk_{g2}
stop propagating clock information from node clk_{g2}

*** finished calculating MIN clock skew ***

Path Search Begins

*** start searching LONGEST paths ***

start searching for source node clk_g
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
stop searching from source node clk_g

start searching for source node clk_{g2}
stop searching from source node clk_{g2}

start searching for source node op_dsbl_after
stop searching from source node op_dsbl_after

start searching for source node eu_iu_spare1

stop searching from source node eu_iu_spare1

start searching for source node second_op_lat
stop searching from source node second_op_lat

start searching for source node mcr41_trap
stop searching from source node mcr41_trap

start searching for source node ifet_xcptn
stop searching from source node ifet_xcptn

start searching for source node iu_eu_xcpt_pend
stop searching from source node iu_eu_xcpt_pend

start searching for source node iq_blk_d1
stop searching from source node iq_blk_d1

start searching for source node dcd_op_44
stop searching from source node dcd_op_44

start searching for source node ru_write_in_iq
stop searching from source node ru_write_in_iq

start searching for source node ru_iu_rcvy_rst
stop searching from source node ru_iu_rcvy_rst

start searching for source node eu_iu_enter_slow_md
stop searching from source node eu_iu_enter_slow_md

start searching for source node id_instr_stores
stop searching from source node id_instr_stores

start searching for source node op_inq_stores

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xc2766.X_P1.IBMtech_P to node n1115
DC path exists through the following transistors from node: n1115 to vdd
xc2766.X_P2.IBMtech_P

stop searching from source node op_inq_stores

start searching for source node iq_blk_aa
stop searching from source node iq_blk_aa

start searching for source node aa_ofc_available
stop searching from source node aa_ofc_available

start searching for source node eu_iu_mmode
stop searching from source node eu_iu_mmode

start searching for source node eu_iu_mcset_e1
stop searching from source node eu_iu_mcset_e1

start searching for source node aa_ofc_hold
stop searching from source node aa_ofc_hold

start searching for source node ru_98_43

stop searching from source node ru_98_43

start searching for source node srlz_op_match
stop searching from source node srlz_op_match

start searching for source node first_op_lat
stop searching from source node first_op_lat

start searching for source node zero_branches
stop searching from source node zero_branches

start searching for source node dcd_mcr41_blk
stop searching from source node dcd_mcr41_blk

start searching for source node xu_iu_xlat_busy
stop searching from source node xu_iu_xlat_busy

start searching for source node du_iu_hold_aa_req
stop searching from source node du_iu_hold_aa_req

start searching for source node eu_iu_fpu_end_op
stop searching from source node eu_iu_fpu_end_op

start searching for source node eu_iu_misc_hold
stop searching from source node eu_iu_misc_hold

start searching for source node op_cmp_raw
stop searching from source node op_cmp_raw

start searching for source node op_dsbl_before
stop searching from source node op_dsbl_before

start searching for source node op_drain
stop searching from source node op_drain

start searching for source node eu_iu_fxu_end_op
stop searching from source node eu_iu_fxu_end_op

start searching for source node op_mccnd_raw
stop searching from source node op_mccnd_raw

start searching for source node eu_iu_br_wrong

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node
xex_in_prog_reg_n_lat_0.X_core.l1_n

DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd
xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P

stop searching from source node eu_iu_br_wrong

start searching for source node need_opnd_req
stop searching from source node need_opnd_req

start searching for source node legal_bht_br
stop searching from source node legal_bht_br

start searching for source node bht_branch_req
stop searching from source node bht_branch_req

start searching for source node id_ex_in_mm
stop searching from source node id_ex_in_mm

start searching for source node du_iu_quiesced
stop searching from source node du_iu_quiesced

start searching for source node iu_op_cmp_hit_a
stop searching from source node iu_op_cmp_hit_a

start searching for source node iu_op_cmp_hit_b
stop searching from source node iu_op_cmp_hit_b

start searching for source node iu_op_cmp_hit_c
stop searching from source node iu_op_cmp_hit_c

start searching for source node iu_op_cmp_hit_d
stop searching from source node iu_op_cmp_hit_d

start searching for source node dcd_frc_milli
stop searching from source node dcd_frc_milli

start searching for source node iq_empty
stop searching from source node iq_empty

start searching for source node op_serialize
stop searching from source node op_serialize

start searching for source node aa_agi_lat
stop searching from source node aa_agi_lat

start searching for source node branch_request
stop searching from source node branch_request

start searching for source node ru_9a_52
stop searching from source node ru_9a_52

start searching for source node bu_iu_quiesced
stop searching from source node bu_iu_quiesced

start searching for source node dcd_blk_dsucc
stop searching from source node dcd_blk_dsucc

start searching for source node op_eim_dcd
stop searching from source node op_eim_dcd

start searching for source node iqmcode_mod_390gr
stop searching from source node iqmcode_mod_390gr

start searching for source node eu_iu_e1_exc_cond
stop searching from source node eu_iu_e1_exc_cond

start searching for source node aa_ofc_block_req

stop searching from source node aa_ofc_block_req

start searching for source node eu_iu_fpu_excprn
stop searching from source node eu_iu_fpu_excprn

start searching for source node block_aa_branch
stop searching from source node block_aa_branch

start searching for source node ru_iu_rq_blk
stop searching from source node ru_iu_rq_blk

start searching for source node op_chkpt_synch
stop searching from source node op_chkpt_synch

start searching for source node ireg_valid

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xc2752.X_P1.IBMtech_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X_P2.IBMtech_P

stop searching from source node ireg_valid

start searching for source node ru_9a_36
stop searching from source node ru_9a_36

start searching for source node three_branches
stop searching from source node three_branches

start searching for source node bht_block_dcd
stop searching from source node bht_block_dcd

start searching for source node ru_9a_20
stop searching from source node ru_9a_20

start searching for source node iu_eu_data_blocked
stop searching from source node iu_eu_data_blocked

start searching for source node op_is_44
stop searching from source node op_is_44

start searching for source node inst_fetches
stop searching from source node inst_fetches

start searching for source node eu_iu_fxu_exc_cond
stop searching from source node eu_iu_fxu_exc_cond

start searching for source node ru_9a_04
stop searching from source node ru_9a_04

start searching for source node br_wrong_targ

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node
xex_in_prog_reg_n_lat_0.X_core.l1_n
DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd
xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P

stop searching from source node br_wrong_targ

start searching for source node scan_enable
stop searching from source node scan_enable

start searching for source node du_iu_store_status<0>
stop searching from source node du_iu_store_status<0>

start searching for source node du_iu_store_status<1>
stop searching from source node du_iu_store_status<1>

start searching for source node du_iu_store_status<2>
stop searching from source node du_iu_store_status<2>

start searching for source node eu_iu_srlz_op_actn<0>
stop searching from source node eu_iu_srlz_op_actn<0>

start searching for source node eu_iu_srlz_op_actn<1>
stop searching from source node eu_iu_srlz_op_actn<1>

start searching for source node ru_9a_0001<0>
stop searching from source node ru_9a_0001<0>

start searching for source node ru_9a_0001<1>
stop searching from source node ru_9a_0001<1>

start searching for source node ireg_0_1<0>
stop searching from source node ireg_0_1<0>

start searching for source node ireg_0_1<1>
stop searching from source node ireg_0_1<1>

start searching for source node num_dcd_cyl<0>
stop searching from source node num_dcd_cyl<0>

start searching for source node num_dcd_cyl<1>
stop searching from source node num_dcd_cyl<1>

start searching for source node ru_9a_3233<32>
stop searching from source node ru_9a_3233<32>

start searching for source node ru_9a_3233<33>
stop searching from source node ru_9a_3233<33>

start searching for source node eu_iu_interrupt_info<0>
stop searching from source node eu_iu_interrupt_info<0>

start searching for source node eu_iu_interrupt_info<1>
stop searching from source node eu_iu_interrupt_info<1>

start searching for source node eu_iu_interrupt_info<2>
stop searching from source node eu_iu_interrupt_info<2>

start searching for source node eu_iu_interrupt_info<3>
stop searching from source node eu_iu_interrupt_info<3>

start searching for source node ru_9a_1617<16>

stop searching from source node ru_9a_1617<16>

start searching for source node ru_9a_1617<17>
stop searching from source node ru_9a_1617<17>

start searching for source node eu_iu_srlz_op_encode<0>
stop searching from source node eu_iu_srlz_op_encode<0>

start searching for source node eu_iu_srlz_op_encode<1>
stop searching from source node eu_iu_srlz_op_encode<1>

start searching for source node eu_iu_srlz_op_encode<2>
stop searching from source node eu_iu_srlz_op_encode<2>

start searching for source node eu_iu_srlz_op_encode<3>
stop searching from source node eu_iu_srlz_op_encode<3>

start searching for source node eu_iu_srlz_op_encode<4>
stop searching from source node eu_iu_srlz_op_encode<4>

start searching for source node eu_iu_srlz_op_encode<5>
stop searching from source node eu_iu_srlz_op_encode<5>

start searching for source node eu_iu_srlz_op_encode<6>
stop searching from source node eu_iu_srlz_op_encode<6>

start searching for source node eu_iu_srlz_op_encode<7>
stop searching from source node eu_iu_srlz_op_encode<7>

start searching for source node eu_iu_srlz_op_encode<8>
stop searching from source node eu_iu_srlz_op_encode<8>

start searching for source node eu_iu_srlz_op_encode<9>
stop searching from source node eu_iu_srlz_op_encode<9>

start searching for source node eu_iu_srlz_op_encode<10>
stop searching from source node eu_iu_srlz_op_encode<10>

start searching for source node eu_iu_srlz_op_encode<11>
stop searching from source node eu_iu_srlz_op_encode<11>

start searching for source node ru_9a_4849<48>
stop searching from source node ru_9a_4849<48>

start searching for source node ru_9a_4849<49>
stop searching from source node ru_9a_4849<49>

start searching for source node ireg_1631<22>
stop searching from source node ireg_1631<22>

start searching for source node ireg_1631<23>
stop searching from source node ireg_1631<23>

start searching for source node ireg_1631<24>
stop searching from source node ireg_1631<24>

start searching for source node ireg_1631<25>
stop searching from source node ireg_1631<25>

start searching for source node ireg_1631<26>
stop searching from source node ireg_1631<26>

start searching for source node ireg_1631<27>
stop searching from source node ireg_1631<27>

start searching for source node ireg_1631<28>
stop searching from source node ireg_1631<28>

start searching for source node ireg_1631<29>
stop searching from source node ireg_1631<29>

start searching for source node ireg_1631<30>
stop searching from source node ireg_1631<30>

*** finished searching LONGEST paths ***

*** start searching SHORTEST paths ***

start searching for source node clk
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
stop searching from source node clk

start searching for source node clk2
stop searching from source node clk2

start searching for source node op_dsbl_after
stop searching from source node op_dsbl_after

start searching for source node eu_iu_spare1
stop searching from source node eu_iu_spare1

start searching for source node second_op_lat
stop searching from source node second_op_lat

start searching for source node mcr41_trap
stop searching from source node mcr41_trap

start searching for source node ifet_xcptn
stop searching from source node ifet_xcptn

start searching for source node iu_eu_xcpt_pend
stop searching from source node iu_eu_xcpt_pend

start searching for source node iq_blk_d1
stop searching from source node iq_blk_d1

start searching for source node dcd_op_44
stop searching from source node dcd_op_44

start searching for source node ru_write_in_iq
stop searching from source node ru_write_in_iq

start searching for source node ru_iu_rcvy_rst
stop searching from source node ru_iu_rcvy_rst

start searching for source node eu_iu_enter_slow_md
stop searching from source node eu_iu_enter_slow_md

start searching for source node id_instr_stores
stop searching from source node id_instr_stores

start searching for source node op_inq_stores
stop searching from source node op_inq_stores

start searching for source node iq_blk_aa
stop searching from source node iq_blk_aa

start searching for source node aa_ofc_available
stop searching from source node aa_ofc_available

start searching for source node eu_iu_mmode
stop searching from source node eu_iu_mmode

start searching for source node eu_iu_mcset_e1
stop searching from source node eu_iu_mcset_e1

start searching for source node aa_ofc_hold
stop searching from source node aa_ofc_hold

start searching for source node ru_98_43
stop searching from source node ru_98_43

start searching for source node srlz_op_match
stop searching from source node srlz_op_match

start searching for source node first_op_lat
stop searching from source node first_op_lat

start searching for source node zero_branches
stop searching from source node zero_branches

start searching for source node dcd_mcr41_blk

stop searching from source node dcd_mcr41_blk

start searching for source node xu_iu_xlat_busy
stop searching from source node xu_iu_xlat_busy

start searching for source node du_iu_hold_aa_req
stop searching from source node du_iu_hold_aa_req

start searching for source node eu_iu_fpu_end_op
stop searching from source node eu_iu_fpu_end_op

start searching for source node eu_iu_misc_hold
stop searching from source node eu_iu_misc_hold

start searching for source node op_cmp_raw
stop searching from source node op_cmp_raw

start searching for source node op_dsbl_before
stop searching from source node op_dsbl_before

start searching for source node op_drain
stop searching from source node op_drain

start searching for source node eu_iu_fxu_end_op
stop searching from source node eu_iu_fxu_end_op

start searching for source node op_mccnd_raw
stop searching from source node op_mccnd_raw

start searching for source node eu_iu_br_wrong

WARNING:PathMill:0x20532001:

Can't simulate delay from tx.xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node
xex_in_prog_reg_n_lat_0.X_core.l1_n

DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd
xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P

stop searching from source node eu_iu_br_wrong

start searching for source node need_opnd_req
stop searching from source node need_opnd_req

start searching for source node legal_bht_br
stop searching from source node legal_bht_br

start searching for source node bht_branch_req
stop searching from source node bht_branch_req

start searching for source node id_ex_in_mm
stop searching from source node id_ex_in_mm

start searching for source node du_iu_quiesced
stop searching from source node du_iu_quiesced

start searching for source node iu_op_cmp_hit_a
stop searching from source node iu_op_cmp_hit_a

start searching for source node iu_op_cmp_hit_b
stop searching from source node iu_op_cmp_hit_b

start searching for source node iu_op_cmp_hit_c
stop searching from source node iu_op_cmp_hit_c

start searching for source node iu_op_cmp_hit_d
stop searching from source node iu_op_cmp_hit_d

start searching for source node dcd_frc_milli
stop searching from source node dcd_frc_milli

start searching for source node iq_empty
stop searching from source node iq_empty

start searching for source node op_serialize
stop searching from source node op_serialize

start searching for source node aa_agi_lat
stop searching from source node aa_agi_lat

start searching for source node branch_request
stop searching from source node branch_request

start searching for source node ru_9a_52
stop searching from source node ru_9a_52

start searching for source node bu_iu_quiesced
stop searching from source node bu_iu_quiesced

start searching for source node dcd_blk_dsucc
stop searching from source node dcd_blk_dsucc

start searching for source node op_eim_dcd
stop searching from source node op_eim_dcd

start searching for source node iqmcode_mod_390gr
stop searching from source node iqmcode_mod_390gr

start searching for source node eu_iu_e1_exc_cond
stop searching from source node eu_iu_e1_exc_cond

start searching for source node aa_ofc_block_req
stop searching from source node aa_ofc_block_req

start searching for source node eu_iu_fpu_excprn
stop searching from source node eu_iu_fpu_excprn

start searching for source node block_aa_branch
stop searching from source node block_aa_branch

start searching for source node ru_iu_rq_blk
stop searching from source node ru_iu_rq_blk

start searching for source node op_chkpt_synch

stop searching from source node op_chkpt_synch

start searching for source node ireg_valid

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xc2752.X_P1.IBMtech_P to node n1415

DC path exists through the following transistors from node: n1415 to vdd

xc2752.X_P2.IBMtech_P

stop searching from source node ireg_valid

start searching for source node ru_9a_36

stop searching from source node ru_9a_36

start searching for source node three_branches

stop searching from source node three_branches

start searching for source node bht_block_dcd

stop searching from source node bht_block_dcd

start searching for source node ru_9a_20

stop searching from source node ru_9a_20

start searching for source node iu_eu_data_blocked

stop searching from source node iu_eu_data_blocked

start searching for source node op_is_44

stop searching from source node op_is_44

start searching for source node inst_fetches

stop searching from source node inst_fetches

start searching for source node eu_iu_fxu_exc_cond

stop searching from source node eu_iu_fxu_exc_cond

start searching for source node ru_9a_04

stop searching from source node ru_9a_04

start searching for source node br_wrong_targ

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node

xex_in_prog_reg_n_lat_0.X_core.l1_n

DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd

xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P

stop searching from source node br_wrong_targ

start searching for source node scan_enable

stop searching from source node scan_enable

start searching for source node du_iu_store_status<0>

stop searching from source node du_iu_store_status<0>

start searching for source node du_iu_store_status<1>

stop searching from source node du_iu_store_status<1>

start searching for source node du_iu_store_status<2>

stop searching from source node du_iu_store_status<2>

start searching for source node eu_iu_srlz_op_actn<0>
stop searching from source node eu_iu_srlz_op_actn<0>

start searching for source node eu_iu_srlz_op_actn<1>
stop searching from source node eu_iu_srlz_op_actn<1>

start searching for source node ru_9a_0001<0>
stop searching from source node ru_9a_0001<0>

start searching for source node ru_9a_0001<1>
stop searching from source node ru_9a_0001<1>

start searching for source node ireg_0_1<0>
stop searching from source node ireg_0_1<0>

start searching for source node ireg_0_1<1>
stop searching from source node ireg_0_1<1>

start searching for source node num_dcd_cyl<0>
stop searching from source node num_dcd_cyl<0>

start searching for source node num_dcd_cyl<1>
stop searching from source node num_dcd_cyl<1>

start searching for source node ru_9a_3233<32>
stop searching from source node ru_9a_3233<32>

start searching for source node ru_9a_3233<33>
stop searching from source node ru_9a_3233<33>

start searching for source node eu_iu_interrupt_info<0>
stop searching from source node eu_iu_interrupt_info<0>

start searching for source node eu_iu_interrupt_info<1>
stop searching from source node eu_iu_interrupt_info<1>

start searching for source node eu_iu_interrupt_info<2>
stop searching from source node eu_iu_interrupt_info<2>

start searching for source node eu_iu_interrupt_info<3>
stop searching from source node eu_iu_interrupt_info<3>

start searching for source node ru_9a_1617<16>
stop searching from source node ru_9a_1617<16>

start searching for source node ru_9a_1617<17>
stop searching from source node ru_9a_1617<17>

start searching for source node eu_iu_srlz_op_encode<0>
stop searching from source node eu_iu_srlz_op_encode<0>

start searching for source node eu_iu_srlz_op_encode<1>
stop searching from source node eu_iu_srlz_op_encode<1>

start searching for source node eu_iu_srlz_op_encode<2>

stop searching from source node eu_iu_srlz_op_encode<2>

start searching for source node eu_iu_srlz_op_encode<3>
stop searching from source node eu_iu_srlz_op_encode<3>

start searching for source node eu_iu_srlz_op_encode<4>
stop searching from source node eu_iu_srlz_op_encode<4>

start searching for source node eu_iu_srlz_op_encode<5>
stop searching from source node eu_iu_srlz_op_encode<5>

start searching for source node eu_iu_srlz_op_encode<6>
stop searching from source node eu_iu_srlz_op_encode<6>

start searching for source node eu_iu_srlz_op_encode<7>
stop searching from source node eu_iu_srlz_op_encode<7>

start searching for source node eu_iu_srlz_op_encode<8>
stop searching from source node eu_iu_srlz_op_encode<8>

start searching for source node eu_iu_srlz_op_encode<9>
stop searching from source node eu_iu_srlz_op_encode<9>

start searching for source node eu_iu_srlz_op_encode<10>
stop searching from source node eu_iu_srlz_op_encode<10>

start searching for source node eu_iu_srlz_op_encode<11>
stop searching from source node eu_iu_srlz_op_encode<11>

start searching for source node ru_9a_4849<48>
stop searching from source node ru_9a_4849<48>

start searching for source node ru_9a_4849<49>
stop searching from source node ru_9a_4849<49>

start searching for source node ireg_1631<22>
stop searching from source node ireg_1631<22>

start searching for source node ireg_1631<23>
stop searching from source node ireg_1631<23>

start searching for source node ireg_1631<24>
stop searching from source node ireg_1631<24>

start searching for source node ireg_1631<25>
stop searching from source node ireg_1631<25>

start searching for source node ireg_1631<26>
stop searching from source node ireg_1631<26>

start searching for source node ireg_1631<27>
stop searching from source node ireg_1631<27>

start searching for source node ireg_1631<28>
stop searching from source node ireg_1631<28>

start searching for source node ireg_1631<29>
stop searching from source node ireg_1631<29>

start searching for source node ireg_1631<30>
stop searching from source node ireg_1631<30>

*** finished searching SHORTEST paths ***

*** Critical Paths Search Completed. ***

*** Printing Reports. ***

A total of 2000 timing errors were reported in build_model.err

A total of 200 critical paths were reported in build_model.out

***Node Slopes

NODES WITH LARGE SLOPE

=====

NODE <-> slowest slope <-> node causing this transition

eu_iu_fxu_exc_cond	0.487 F	<null>	
du_iu_quiesced	0.422 F	<null>	
eu_iu_mmode	0.407 F	<null>	
eu_iu_fpu_end_op	0.423 R	<null>	
du_iu_hold_aa_req	0.53 F	<null>	
eu_iu_enter_slow_md	0.44 R	<null>	
eu_iu_misc_hold	0.415 R	<null>	
eu_iu_srlz_op_encode<11>	0.625 F	<null>	<null>
eu_iu_srlz_op_actn<0>	0.467 F	<null>	
eu_iu_srlz_op_actn<1>	0.426 F	<null>	
eu_iu_srlz_op_encode<5>	0.466 F	<null>	<null>
eu_iu_srlz_op_encode<4>	0.507 R	<null>	<null>
eu_iu_srlz_op_encode<6>	0.442 R	<null>	<null>
eu_iu_srlz_op_encode<7>	0.497 R	<null>	<null>
eu_iu_srlz_op_encode<8>	0.458 F	<null>	<null>
eu_iu_srlz_op_encode<9>	0.403 R	<null>	<null>
eu_iu_srlz_op_encode<2>	0.525 F	<null>	<null>
eu_iu_srlz_op_encode<1>	0.5 R	<null>	<null>
eu_iu_srlz_op_encode<0>	0.501 F	<null>	<null>
du_iu_store_status<2>	0.625 F	<null>	

***End Node Slopes

==> ibm_gray: Starting generation of PathMill IBMgray file. Program version: Version 04/23/98

==> ibm_gray: Writing output messages into file: idcdsuc_mac.ibmgray.log ...

==> ibm_gray: Program finished, now exiting.

==> ibm_gray: Starting generation of PathMill IBMgray file.

==> ibm_gray: Program log file generated by ibm_gray program Version 04/23/98

==> ibm_gray: Program run on: Sun Apr 18 22:16:29 1999

==> ibm_gray: Pathmill version: PATHMILL PM_DEV

==> ibm_gray: No latches were flagged as NON-TRANSPARENT by the PathMill patterns!

==> ibm_gray: Data Gathering Phase
==> ibm_gray: Storing list of dynamic nodes, latches, and clock gates...

==> ibm_gray: Total number of dangling nodes found: 0
==> ibm_gray: Gathering data on clock tree nodes...
==> ibm_gray: Gathering data on model segments and nodes...
==> ibm_gray: Writing out the data into file: idcdsuc_mac.ibmgray ...

==> ibm_gray: Number of PIS found: 0
==> ibm_gray: Number of POS found: 0
==> ibm_gray: Number of LATCHS found: 0
==> ibm_gray: Number of NON-TRANS LATCHS found: 0
==> ibm_gray: Number of DYNAMIC CIRCUITS found: 0
==> ibm_gray: Number of CLOCK GATES found: 0
==> ibm_gray: Number of GLOBAL CLK SEGS found: 0
==> ibm_gray: Number of OTHER PROP SEGS found: 0

==> ibm_gray: Program finished, now exiting.

CTE Pathmill post-processor: Determining quality record from configuration file
CTE Pathmill post-processor: Determining clock information from pathmill data
CTE Pathmill post-processor: Determining worst internal setup and hold slacks

Start writing model file idcdsuc_mac.c
Finished writing model file

*** Finished Printing Reports. ***

Info Pathmill model build finished with a return code of: 0
Info Running Pathmill-Path Search
CTE: Initializing for technology cmos8s

WARNING: Overriding technology files by command line parameter.

Preprocessing configuration file epic.inp --> epic.inp.final

Include path for cpp...

/afs/apd/func/vlsi/alliance00/libraries/pathmill/config
/afs/watson/projects/vlsi/cte/tech/cmos8s/base/prod/pathmill/config
/afs/apd/func/vlsi/alliance00/bssc8/prod/cc8s/pathmill/config
/afs/watson/projects/vlsi/cte/tools/epic/5.1/local/pathmill/config

Locating cpp include files for epic.inp...

/afs/apd/func/vlsi/alliance00/libraries/pathmill/config/template.cfg
./IDCDSUC.assert
/afs/apd/func/vlsi/alliance00/libraries/pathmill/config/sets.cfg
./IDCDSUC.nodecap

Executing /usr/ccs/lib/cpp...

Executing PERL: substituting CTE vars and generating node lists...

Preprocessing completed successfully

EXEC /afs/apd/func/vlsi/alliance00/libraries/pathmill/audit/pm_audit_alli00 -U
/afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p

```
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early -x -n netlist -c epic.inp.final -L
/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice -b 3 -u
```

```
[pm_audit_alli00] Alliance 2000 Pathmill Audit Program (version 0.1)
[pm_audit_alli00] Executed: Sun Apr 18 22:16:44 EDT 1999
[pm_audit_alli00] WARNING -- Specified 2 tech files:
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early!
[pm_audit_alli00] CTE environment specifies...
[pm_audit_alli00] technology: cmos8s
[pm_audit_alli00] ibmtech version: 5.1
[pm_audit_alli00] pathmill install: 5.1
[pm_audit_alli00] Checking netlist file: netlist
[pm_audit_alli00] WARNING -- Netlist is missing technology audit data!
[pm_audit_alli00] Completed successfully
```

EPIC_CC_OPTIONS is set to: -D_ENABLE_HOOKS -D_PROCESS_MODEL

```
pathmill -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early -x -n netlist -c epic.inp.final -L
/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice -b 3 -u
```

Building libCustom.o

```
#! .epicrun/libCustom.o
```

```
if_setup
```

```
epic_mti_if_quit_ack
```

```
epicState
```

```
shm_put_msg
```

```
put_msg
```

```
ld: 0711-319 WARNING: Exported symbol not defined: estimateDeviceParameters
```

```
ld: 0711-319 WARNING: Exported symbol not defined: timemill_user_init
```

```
ld: 0711-319 WARNING: Exported symbol not defined: powrmill_user_init
```

```
ld: 0711-319 WARNING: Exported symbol not defined: iAreaCap
```

```
ld: 0711-319 WARNING: Exported symbol not defined: iDiffCap
```

```
ld: 0711-319 WARNING: Exported symbol not defined: iFringeCap
```

```
ld: 0711-319 WARNING: Exported symbol not defined: ilnit
```

```
ld: 0711-319 WARNING: Exported symbol not defined: m12cc
```

```
ld: 0711-319 WARNING: Exported symbol not defined: m12dw
```

```
ld: 0711-319 WARNING: Exported symbol not defined: epicUserControl
```

```
ld: 0711-319 WARNING: Exported symbol not defined: epicUserMain
```

```
ld: 0711-319 WARNING: Exported symbol not defined: epic_mti_if_quit_ack
```

```
ld: 0711-319 WARNING: Exported symbol not defined: if_setup
```

```
ld: 0711-319 WARNING: Exported symbol not defined: epicState
```

```
ld: 0711-319 WARNING: Exported symbol not defined: shm_put_msg
```

```
ld: 0711-319 WARNING: Exported symbol not defined: put_msg
```

```
Using /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/libCustom.o ...
```

Notice: License pathmill will expire on 4/30/99.

options:

```
pathmill -t -c epic.inp.final -p
```

```
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early -x -n netlist -c epic.inp.final -L
```

s8s.pathmill.early -o pathmill.out -b 3
Simulator execution begins...

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Notice: License pathmill/pfx will expire on 4/30/99.

Compiling "netlist"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cb_mode_block.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_mode_block.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_invv02.spi"
Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oPfet"
Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oNfet"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_invv01.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_lat_core_s.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cb_clk_32_1.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_32_1.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_core.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_se.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_clk_clka.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invv11e.spi"

Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oPfetLowVt"

Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models/pm_oNfetLowVt"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn12c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn10c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn09c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn07c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n02c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn01c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n04c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn15c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn11c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn13c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv19b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn08c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn12d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn04c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n12c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3v02c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v13c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n03c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2n04c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4n03c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn14c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao12n03c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_xbn2n01b.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n03c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor3n03c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_oa21n10c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n11c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_oa22n10c.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_xbo2n01d.spi"

Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2x14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao12n10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v13d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn06d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n04c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2x14e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4n05d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao22n10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2x14b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3i11b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4v10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2g14e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4v10b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_oa21n10e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_ao12n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n08c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv13b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2g12e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv13c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2v14c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2n06d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor3v10e.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvn16c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invvv09c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3n05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2n05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nor2v11c.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2g11b.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3z10c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn07d.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/zljs_lat_core_b.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_nnd2n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_nnd2n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn05c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_ao22n07c.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_ao22n02c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_invvn06d.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_nnd3n07c.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_nnd3n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_nor2n06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_nor2n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_ao21n07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_ao21n02.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cl_ao21n07c.spi"
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Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cc_ao21n02.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd2f03c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd3z07c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_nnd4v06c.spi"
Notice: License spice_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bssc8/prod/pathmill/spice/cs_invn01e.spi"

|

|

PathMill Version 5.1plus
SN: P013098-AIX
Copyright (c) 1997 Synopsys Inc., All Rights Reserved.

Built by olevi in " PM_DEV " on Fri Jan 30 12:01:27 PST 1998

Enabling ibmgray model bulding code.

Warning: invalid command or arguments on line 69 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.
corners 10 1.45

Warning: invalid command or arguments on line 1920 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.
corners 10 1.45

Warning: invalid command or arguments on line 68 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early.
corners -10 1.70

Warning: invalid command or arguments on line 1919 in file
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early.
corners -10 1.70

Done building data structure

CTE Pathmill post-processor: Determining clock nodes to ignore

CTE Pathmill post-processor: Determining pattern files from configuration file

WARNING:PathMill:0x20521001:Node gp_tr_scan_out does not exist in netlist

WARNING:PathMill:0x20521001:Node gp_tr_scan_out does not exist in netlist

WARNING:PathMill:0x20525001:source_node test_c1 is set to LOW

WARNING:PathMill:0x20525001:source_node scan_in is set to LOW

WARNING:PathMill:0x20521001:Node scan_in<0> does not exist in netlist

WARNING:PathMill:0x20521001:Node scan_in<1> does not exist in netlist

WARNING:PathMill:0x20521001:Node scan_in<2> does not exist in netlist

WARNING:PathMill:0x20525001:source_node a_clk is set to LOW

WARNING:PathMill:0x20525001:source_node b_clk is set to LOW

WARNING:PathMill:0x20525001:source_node clk1_mode7 is set to HIGH

WARNING:PathMill:0x20525001:source_node gp_tr_a_clk is set to LOW

WARNING:PathMill:0x20525001:source_node gp_tr_b_clk is set to LOW

WARNING:PathMill:0x20525001:source_node gp_tr_scan_in is set to LOW

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_P465.IBMtech_P(pf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_P465.IBMtech_P(pf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_N468.IBMtech_N(nf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_core.X_N468.IBMtech_N(nf_epic)
(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_P346.IBMtech_P(pf_e
pic) (l=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_P346.IBMtech_P(pf_e
pic) (l=0.65u) is not in tech file
WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_N344.IBMtech_N(nf_e
pic) (l=0.65u) is not in tech file
WARNING:PathMill:0x20551015:xslow_mode_clockblock.X_cb.X_scan_enable.X_N344.IBMtech_N(nf_e
pic) (l=0.65u) is not in tech file

Working in timing verify mode - clock edge reference, turning on the transparent_mode

Unlimited transparency depth

data_to_latch report is on

latch_to_latch report is on

gated_clock report is on

pattern acac_drv2000: 0 matched

pattern invmux: 0 matched

pattern buffer2: 0 matched

pattern zljs_clk_core_padc1: 0 matched

==> ibm_gray: Opened the NT latch pattern list named:

/afs/apd/func/vlsi/alliance00/libraries/pathmill/patterns/nt_latch_pattern_list

pattern zljs_clk_32_1: 6 matched

pattern zljs_clk_core: 6 matched

pattern zljs_clk_corepar: 0 matched

pattern zljs_clk_32_2: 0 matched

pattern zljs_clk_core: 0 matched

pattern zljs_clk_corepar: 0 matched

pattern zljs_clk_32_3: 0 matched

pattern zljs_clk_core3: 0 matched

pattern zljs_clk_core3par: 0 matched

pattern zljs_lat_core_a: 0 matched

pattern zljs_lat_core_b: 83 matched

pattern zljs_lat_core_c: 0 matched

pattern tg: 42 matched

pattern 4ns: 0 matched

pattern 4ps: 9 matched

pattern 2ns: 96 matched

pattern 2ps: 714 matched

pattern 2ns1a: 28 matched

pattern 2ps1a: 104 matched

pattern 2ns1: 32 matched

pattern 2ps1: 32 matched

pattern 2ns2: 118 matched

pattern 2ps2: 40 matched

pattern XN4: 0 matched

pattern XR4: 0 matched

pattern XN3: 0 matched

pattern XR3: 0 matched

pattern XN2: 0 matched

pattern XN2B: 1 matched

pattern XN2BGoofyExtract: 0 matched

pattern XR2: 0 matched

pattern XR2B: 1 matched

build model name idcdsuc_mac

Done reading setup file for build_model characterize.file

pattern zljs_mode_block: 0 matched
pattern zljs_mode_block: 1 matched

Marking Inverters, Latches and RAM cells
Finished Marking Inverters, Latches and RAM cells

Marking Transfer gates
Finished Marking Transfer gates

Setting transistor Directions
The percentage of elements with direction set is (including bi-directional) 100.00%.
Clock Propagation Begins
Clock Propagation End
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<4>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<4>.l1_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<5>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<5>.l1_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<6>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<6>.l1_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<7>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr_latch.X_mb.X_mode<7>.l1_n

*** start calculating MAX clock skew ***

start propagating clock information for node clkg
stop propagating clock information from node clkg

start propagating clock information for node clkg2
stop propagating clock information from node clkg2

*** finished calculating MAX clock skew ***

*** start calculating MIN clock skew ***

start propagating clock information for node clkg
stop propagating clock information from node clkg

start propagating clock information for node clkg2
stop propagating clock information from node clkg2

*** finished calculating MIN clock skew ***

Path Search Begins

*** start searching LONGEST paths ***

start searching for source node clkg
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<0>.IBMTech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<1>.IBMTech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<0>.IBMTech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<1>.IBMTech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
stop searching from source node clkg

start searching for source node clkg2
stop searching from source node clkg2

start searching for source node op_dsbl_after
stop searching from source node op_dsbl_after

start searching for source node eu_iu_spare1
stop searching from source node eu_iu_spare1

start searching for source node second_op_lat
stop searching from source node second_op_lat

start searching for source node mcr41_trap
stop searching from source node mcr41_trap

start searching for source node ifet_xcptn
stop searching from source node ifet_xcptn

start searching for source node iu_eu_xcpt_pend
stop searching from source node iu_eu_xcpt_pend

start searching for source node iq_blk_d1
stop searching from source node iq_blk_d1

start searching for source node dcd_op_44
stop searching from source node dcd_op_44

start searching for source node ru_write_in_iq
stop searching from source node ru_write_in_iq

start searching for source node ru_iu_rcvy_rst
stop searching from source node ru_iu_rcvy_rst

start searching for source node eu_iu_enter_slow_md
stop searching from source node eu_iu_enter_slow_md

start searching for source node id_instr_stores
stop searching from source node id_instr_stores

start searching for source node op_inq_stores
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2766.X_P1.IBMTech_P to node n1115
DC path exists through the following transistors from node: n1115 to vdd

xc2766.X_P2.IBMtech_P

stop searching from source node op_inq_stores

start searching for source node iq_blk_aa
stop searching from source node iq_blk_aa

start searching for source node aa_ofc_available
stop searching from source node aa_ofc_available

start searching for source node eu_iu_mmode
stop searching from source node eu_iu_mmode

start searching for source node eu_iu_mcset_e1
stop searching from source node eu_iu_mcset_e1

start searching for source node aa_ofc_hold
stop searching from source node aa_ofc_hold

start searching for source node ru_98_43
stop searching from source node ru_98_43

start searching for source node srlz_op_match
stop searching from source node srlz_op_match

start searching for source node first_op_lat
stop searching from source node first_op_lat

start searching for source node zero_branches
stop searching from source node zero_branches

start searching for source node dcd_mcr41_blk
stop searching from source node dcd_mcr41_blk

start searching for source node xu_iu_xlat_busy
stop searching from source node xu_iu_xlat_busy

start searching for source node du_iu_hold_aa_req
stop searching from source node du_iu_hold_aa_req

start searching for source node eu_iu_fpu_end_op
stop searching from source node eu_iu_fpu_end_op

start searching for source node eu_iu_misc_hold
stop searching from source node eu_iu_misc_hold

start searching for source node op_cmp_raw
stop searching from source node op_cmp_raw

start searching for source node op_dsbl_before
stop searching from source node op_dsbl_before

start searching for source node op_drain
stop searching from source node op_drain

start searching for source node eu_iu_fxu_end_op

stop searching from source node eu_iu_fxu_end_op

start searching for source node op_mccnd_raw
stop searching from source node op_mccnd_raw

start searching for source node eu_iu_br_wrong

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node
xex_in_prog_reg_n_lat_0.X_core.l1_n

DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd
xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P

stop searching from source node eu_iu_br_wrong

start searching for source node need_opnd_req
stop searching from source node need_opnd_req

start searching for source node legal_bht_br
stop searching from source node legal_bht_br

start searching for source node bht_branch_req
stop searching from source node bht_branch_req

start searching for source node id_ex_in_mm
stop searching from source node id_ex_in_mm

start searching for source node du_iu_quiesced
stop searching from source node du_iu_quiesced

start searching for source node iu_op_cmp_hit_a
stop searching from source node iu_op_cmp_hit_a

start searching for source node iu_op_cmp_hit_b
stop searching from source node iu_op_cmp_hit_b

start searching for source node iu_op_cmp_hit_c
stop searching from source node iu_op_cmp_hit_c

start searching for source node iu_op_cmp_hit_d
stop searching from source node iu_op_cmp_hit_d

start searching for source node dcd_frc_milli
stop searching from source node dcd_frc_milli

start searching for source node iq_empty
stop searching from source node iq_empty

start searching for source node op_serialize
stop searching from source node op_serialize

start searching for source node aa_agi_lat
stop searching from source node aa_agi_lat

start searching for source node branch_request
stop searching from source node branch_request

start searching for source node ru_9a_52
stop searching from source node ru_9a_52

start searching for source node bu_iu_quiesced
stop searching from source node bu_iu_quiesced

start searching for source node dcd_blk_dsucc
stop searching from source node dcd_blk_dsucc

start searching for source node op_eim_dcd
stop searching from source node op_eim_dcd

start searching for source node iqmcode_mod_390gr
stop searching from source node iqmcode_mod_390gr

start searching for source node eu_iu_e1_exc_cond
stop searching from source node eu_iu_e1_exc_cond

start searching for source node aa_ofc_block_req
stop searching from source node aa_ofc_block_req

start searching for source node eu_iu_fpu_excpn
stop searching from source node eu_iu_fpu_excpn

start searching for source node block_aa_branch
stop searching from source node block_aa_branch

start searching for source node ru_iu_rq_blk
stop searching from source node ru_iu_rq_blk

start searching for source node op_chkpt_synch
stop searching from source node op_chkpt_synch

start searching for source node ireg_valid
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2752.X_P1.IBMtech_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X_P2.IBMtech_P
stop searching from source node ireg_valid

start searching for source node ru_9a_36
stop searching from source node ru_9a_36

start searching for source node three_branches
stop searching from source node three_branches

start searching for source node bht_block_dcd
stop searching from source node bht_block_dcd

start searching for source node ru_9a_20
stop searching from source node ru_9a_20

start searching for source node iu_eu_data_blocked
stop searching from source node iu_eu_data_blocked

start searching for source node op_is_44
stop searching from source node op_is_44

start searching for source node inst_fetches
stop searching from source node inst_fetches

start searching for source node eu_iu_fxu_exc_cond
stop searching from source node eu_iu_fxu_exc_cond

start searching for source node ru_9a_04
stop searching from source node ru_9a_04

start searching for source node br_wrong_targ
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node
xex_in_prog_reg_n_lat_0.X_core.l1_n
DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd
xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P
stop searching from source node br_wrong_targ

start searching for source node scan_enable
stop searching from source node scan_enable

start searching for source node du_iu_store_status<0>
stop searching from source node du_iu_store_status<0>

start searching for source node du_iu_store_status<1>
stop searching from source node du_iu_store_status<1>

start searching for source node du_iu_store_status<2>
stop searching from source node du_iu_store_status<2>

start searching for source node eu_iu_srlz_op_actn<0>
stop searching from source node eu_iu_srlz_op_actn<0>

start searching for source node eu_iu_srlz_op_actn<1>
stop searching from source node eu_iu_srlz_op_actn<1>

start searching for source node ru_9a_0001<0>
stop searching from source node ru_9a_0001<0>

start searching for source node ru_9a_0001<1>
stop searching from source node ru_9a_0001<1>

start searching for source node ireg_0_1<0>
stop searching from source node ireg_0_1<0>

start searching for source node ireg_0_1<1>
stop searching from source node ireg_0_1<1>

start searching for source node num_dcd_cyl<0>
stop searching from source node num_dcd_cyl<0>

start searching for source node num_dcd_cyl<1>
stop searching from source node num_dcd_cyl<1>

start searching for source node ru_9a_3233<32>
stop searching from source node ru_9a_3233<32>

start searching for source node ru_9a_3233<33>
stop searching from source node ru_9a_3233<33>

start searching for source node eu_iu_interrupt_info<0>
stop searching from source node eu_iu_interrupt_info<0>

start searching for source node eu_iu_interrupt_info<1>
stop searching from source node eu_iu_interrupt_info<1>

start searching for source node eu_iu_interrupt_info<2>
stop searching from source node eu_iu_interrupt_info<2>

start searching for source node eu_iu_interrupt_info<3>
stop searching from source node eu_iu_interrupt_info<3>

start searching for source node ru_9a_1617<16>
stop searching from source node ru_9a_1617<16>

start searching for source node ru_9a_1617<17>
stop searching from source node ru_9a_1617<17>

start searching for source node eu_iu_srlz_op_encode<0>
stop searching from source node eu_iu_srlz_op_encode<0>

start searching for source node eu_iu_srlz_op_encode<1>
stop searching from source node eu_iu_srlz_op_encode<1>

start searching for source node eu_iu_srlz_op_encode<2>
stop searching from source node eu_iu_srlz_op_encode<2>

start searching for source node eu_iu_srlz_op_encode<3>
stop searching from source node eu_iu_srlz_op_encode<3>

start searching for source node eu_iu_srlz_op_encode<4>
stop searching from source node eu_iu_srlz_op_encode<4>

start searching for source node eu_iu_srlz_op_encode<5>
stop searching from source node eu_iu_srlz_op_encode<5>

start searching for source node eu_iu_srlz_op_encode<6>
stop searching from source node eu_iu_srlz_op_encode<6>

start searching for source node eu_iu_srlz_op_encode<7>
stop searching from source node eu_iu_srlz_op_encode<7>

start searching for source node eu_iu_srlz_op_encode<8>
stop searching from source node eu_iu_srlz_op_encode<8>

start searching for source node eu_iu_srlz_op_encode<9>
stop searching from source node eu_iu_srlz_op_encode<9>

start searching for source node eu_iu_srlz_op_encode<10>

stop searching from source node eu_iu_srlz_op_encode<10>

start searching for source node eu_iu_srlz_op_encode<11>
stop searching from source node eu_iu_srlz_op_encode<11>

start searching for source node ru_9a_4849<48>
stop searching from source node ru_9a_4849<48>

start searching for source node ru_9a_4849<49>
stop searching from source node ru_9a_4849<49>

start searching for source node ireg_1631<22>
stop searching from source node ireg_1631<22>

start searching for source node ireg_1631<23>
stop searching from source node ireg_1631<23>

start searching for source node ireg_1631<24>
stop searching from source node ireg_1631<24>

start searching for source node ireg_1631<25>
stop searching from source node ireg_1631<25>

start searching for source node ireg_1631<26>
stop searching from source node ireg_1631<26>

start searching for source node ireg_1631<27>
stop searching from source node ireg_1631<27>

start searching for source node ireg_1631<28>
stop searching from source node ireg_1631<28>

start searching for source node ireg_1631<29>
stop searching from source node ireg_1631<29>

start searching for source node ireg_1631<30>
stop searching from source node ireg_1631<30>

*** finished searching LONGEST paths ***

*** start searching SHORTEST paths ***

start searching for source node clk

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_1.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_1.X_core.l1_n

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<0>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum_dcd_reg_n_lat_0.X_gate.X_N4<1>.IBMtech_N to node xnum_dcd_reg_n_lat_0.X_core.l1_n
stop searching from source node clk_g

start searching for source node clk_{g2}
stop searching from source node clk_{g2}

start searching for source node op_dsbl_after
stop searching from source node op_dsbl_after

start searching for source node eu_iu_spare1
stop searching from source node eu_iu_spare1

start searching for source node second_op_lat
stop searching from source node second_op_lat

start searching for source node mcr41_trap
stop searching from source node mcr41_trap

start searching for source node ifet_xcptn
stop searching from source node ifet_xcptn

start searching for source node iu_eu_xcpt_pend
stop searching from source node iu_eu_xcpt_pend

start searching for source node iq_blk_d1
stop searching from source node iq_blk_d1

start searching for source node dcd_op_44
stop searching from source node dcd_op_44

start searching for source node ru_write_in_iq
stop searching from source node ru_write_in_iq

start searching for source node ru_iu_rcvy_rst
stop searching from source node ru_iu_rcvy_rst

start searching for source node eu_iu_enter_slow_md
stop searching from source node eu_iu_enter_slow_md

start searching for source node id_instr_stores
stop searching from source node id_instr_stores

start searching for source node op_inq_stores
stop searching from source node op_inq_stores

start searching for source node iq_blk_aa
stop searching from source node iq_blk_aa

start searching for source node aa_ofc_available
stop searching from source node aa_ofc_available

start searching for source node eu_iu_mmode

stop searching from source node eu_iu_mmode

start searching for source node eu_iu_mcset_e1
stop searching from source node eu_iu_mcset_e1

start searching for source node aa_ofc_hold
stop searching from source node aa_ofc_hold

start searching for source node ru_98_43
stop searching from source node ru_98_43

start searching for source node srlz_op_match
stop searching from source node srlz_op_match

start searching for source node first_op_lat
stop searching from source node first_op_lat

start searching for source node zero_branches
stop searching from source node zero_branches

start searching for source node dcd_mcr41_blk
stop searching from source node dcd_mcr41_blk

start searching for source node xu_iu_xlat_busy
stop searching from source node xu_iu_xlat_busy

start searching for source node du_iu_hold_aa_req
stop searching from source node du_iu_hold_aa_req

start searching for source node eu_iu_fpu_end_op
stop searching from source node eu_iu_fpu_end_op

start searching for source node eu_iu_misc_hold
stop searching from source node eu_iu_misc_hold

start searching for source node op_cmp_raw
stop searching from source node op_cmp_raw

start searching for source node op_dsbl_before
stop searching from source node op_dsbl_before

start searching for source node op_drain
stop searching from source node op_drain

start searching for source node eu_iu_fxu_end_op
stop searching from source node eu_iu_fxu_end_op

start searching for source node op_mccnd_raw
stop searching from source node op_mccnd_raw

start searching for source node eu_iu_br_wrong

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node
xex_in_prog_reg_n_lat_0.X_core.l1_n

DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd

xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P
stop searching from source node eu_iu_br_wrong

start searching for source node need_opnd_req
stop searching from source node need_opnd_req

start searching for source node legal_bht_br
stop searching from source node legal_bht_br

start searching for source node bht_branch_req
stop searching from source node bht_branch_req

start searching for source node id_ex_in_mm
stop searching from source node id_ex_in_mm

start searching for source node du_iu_quiesced
stop searching from source node du_iu_quiesced

start searching for source node iu_op_cmp_hit_a
stop searching from source node iu_op_cmp_hit_a

start searching for source node iu_op_cmp_hit_b
stop searching from source node iu_op_cmp_hit_b

start searching for source node iu_op_cmp_hit_c
stop searching from source node iu_op_cmp_hit_c

start searching for source node iu_op_cmp_hit_d
stop searching from source node iu_op_cmp_hit_d

start searching for source node dcd_frc_milli
stop searching from source node dcd_frc_milli

start searching for source node iq_empty
stop searching from source node iq_empty

start searching for source node op_serialize
stop searching from source node op_serialize

start searching for source node aa_agi_lat
stop searching from source node aa_agi_lat

start searching for source node branch_request
stop searching from source node branch_request

start searching for source node ru_9a_52
stop searching from source node ru_9a_52

start searching for source node bu_iu_quiesced
stop searching from source node bu_iu_quiesced

start searching for source node dcd_blk_dsucc
stop searching from source node dcd_blk_dsucc

start searching for source node op_eim_dcd

stop searching from source node op_eim_dcd

start searching for source node iqmcode_mod_390gr
stop searching from source node iqmcode_mod_390gr

start searching for source node eu_iu_e1_exc_cond
stop searching from source node eu_iu_e1_exc_cond

start searching for source node aa_ofc_block_req
stop searching from source node aa_ofc_block_req

start searching for source node eu_iu_fpu_excpcn
stop searching from source node eu_iu_fpu_excpcn

start searching for source node block_aa_branch
stop searching from source node block_aa_branch

start searching for source node ru_iu_rq_blk
stop searching from source node ru_iu_rq_blk

start searching for source node op_chkpt_synch
stop searching from source node op_chkpt_synch

start searching for source node ireg_valid

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xc2752.X_P1.IBMtech_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X_P2.IBMtech_P

stop searching from source node ireg_valid

start searching for source node ru_9a_36
stop searching from source node ru_9a_36

start searching for source node three_branches
stop searching from source node three_branches

start searching for source node bht_block_dcd
stop searching from source node bht_block_dcd

start searching for source node ru_9a_20
stop searching from source node ru_9a_20

start searching for source node iu_eu_data_blocked
stop searching from source node iu_eu_data_blocked

start searching for source node op_is_44
stop searching from source node op_is_44

start searching for source node inst_fetches
stop searching from source node inst_fetches

start searching for source node eu_iu_fxu_exc_cond
stop searching from source node eu_iu_fxu_exc_cond

start searching for source node ru_9a_04

stop searching from source node ru_9a_04

start searching for source node br_wrong_targ

WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex_in_prog_reg_n_lat_0.X_gate.X_P1<0>.IBMtech_P to node xex_in_prog_reg_n_lat_0.X_core.l1_n

DC path exists through the following transistors from node: xex_in_prog_reg_n_lat_0.dn to vdd

xex_in_prog_reg_n_lat_0.X_gate.X_P2<0>.IBMtech_P

stop searching from source node br_wrong_targ

start searching for source node scan_enable

stop searching from source node scan_enable

start searching for source node du_iu_store_status<0>

stop searching from source node du_iu_store_status<0>

start searching for source node du_iu_store_status<1>

stop searching from source node du_iu_store_status<1>

start searching for source node du_iu_store_status<2>

stop searching from source node du_iu_store_status<2>

start searching for source node eu_iu_srlz_op_actn<0>

stop searching from source node eu_iu_srlz_op_actn<0>

start searching for source node eu_iu_srlz_op_actn<1>

stop searching from source node eu_iu_srlz_op_actn<1>

start searching for source node ru_9a_0001<0>

stop searching from source node ru_9a_0001<0>

start searching for source node ru_9a_0001<1>

stop searching from source node ru_9a_0001<1>

start searching for source node ireg_0_1<0>

stop searching from source node ireg_0_1<0>

start searching for source node ireg_0_1<1>

stop searching from source node ireg_0_1<1>

start searching for source node num_dcd_cyl<0>

stop searching from source node num_dcd_cyl<0>

start searching for source node num_dcd_cyl<1>

stop searching from source node num_dcd_cyl<1>

start searching for source node ru_9a_3233<32>

stop searching from source node ru_9a_3233<32>

start searching for source node ru_9a_3233<33>

stop searching from source node ru_9a_3233<33>

start searching for source node eu_iu_interrupt_info<0>

stop searching from source node eu_iu_interrupt_info<0>

start searching for source node eu_iu_interrupt_info<1>
stop searching from source node eu_iu_interrupt_info<1>

start searching for source node eu_iu_interrupt_info<2>
stop searching from source node eu_iu_interrupt_info<2>

start searching for source node eu_iu_interrupt_info<3>
stop searching from source node eu_iu_interrupt_info<3>

start searching for source node ru_9a_1617<16>
stop searching from source node ru_9a_1617<16>

start searching for source node ru_9a_1617<17>
stop searching from source node ru_9a_1617<17>

start searching for source node eu_iu_srlz_op_encode<0>
stop searching from source node eu_iu_srlz_op_encode<0>

start searching for source node eu_iu_srlz_op_encode<1>
stop searching from source node eu_iu_srlz_op_encode<1>

start searching for source node eu_iu_srlz_op_encode<2>
stop searching from source node eu_iu_srlz_op_encode<2>

start searching for source node eu_iu_srlz_op_encode<3>
stop searching from source node eu_iu_srlz_op_encode<3>

start searching for source node eu_iu_srlz_op_encode<4>
stop searching from source node eu_iu_srlz_op_encode<4>

start searching for source node eu_iu_srlz_op_encode<5>
stop searching from source node eu_iu_srlz_op_encode<5>

start searching for source node eu_iu_srlz_op_encode<6>
stop searching from source node eu_iu_srlz_op_encode<6>

start searching for source node eu_iu_srlz_op_encode<7>
stop searching from source node eu_iu_srlz_op_encode<7>

start searching for source node eu_iu_srlz_op_encode<8>
stop searching from source node eu_iu_srlz_op_encode<8>

start searching for source node eu_iu_srlz_op_encode<9>
stop searching from source node eu_iu_srlz_op_encode<9>

start searching for source node eu_iu_srlz_op_encode<10>
stop searching from source node eu_iu_srlz_op_encode<10>

start searching for source node eu_iu_srlz_op_encode<11>
stop searching from source node eu_iu_srlz_op_encode<11>

start searching for source node ru_9a_4849<48>
stop searching from source node ru_9a_4849<48>

start searching for source node ru_9a_4849<49>

stop searching from source node ru_9a_4849<49>

start searching for source node ireg_1631<22>
stop searching from source node ireg_1631<22>

start searching for source node ireg_1631<23>
stop searching from source node ireg_1631<23>

start searching for source node ireg_1631<24>
stop searching from source node ireg_1631<24>

start searching for source node ireg_1631<25>
stop searching from source node ireg_1631<25>

start searching for source node ireg_1631<26>
stop searching from source node ireg_1631<26>

start searching for source node ireg_1631<27>
stop searching from source node ireg_1631<27>

start searching for source node ireg_1631<28>
stop searching from source node ireg_1631<28>

start searching for source node ireg_1631<29>
stop searching from source node ireg_1631<29>

start searching for source node ireg_1631<30>
stop searching from source node ireg_1631<30>

*** finished searching SHORTEST paths ***

*** Critical Paths Search Completed. ***

*** Printing Reports. ***

A total of 2000 timing errors were reported in pathmill.err
A total of 200 critical paths were reported in pathmill.out

***Node Slopes

NODES WITH LARGE SLOPE

=====

NODE <-> slowest slope <-> node causing this transition

eu_iu_fxu_exc_cond	0.487 F		<null>
du_iu_quiesced	0.422 F		<null>
eu_iu_mmode	0.407 F		<null>
eu_iu_fpu_end_op	0.423 R		<null>
du_iu_hold_aa_req	0.53 F		<null>
eu_iu_enter_slow_md	0.44 R		<null>
eu_iu_misc_hold	0.415 R		<null>
eu_iu_srlz_op_encode<11>		0.625 F	<null>
eu_iu_srlz_op_actn<0>	0.467 F		<null>

eu_iu_srlz_op_actn<1>	0.426 F	<null>	
eu_iu_srlz_op_encode<5>		0.466 F	<null>
eu_iu_srlz_op_encode<4>		0.507 R	<null>
eu_iu_srlz_op_encode<6>		0.442 R	<null>
eu_iu_srlz_op_encode<7>		0.497 R	<null>
eu_iu_srlz_op_encode<8>		0.458 F	<null>
eu_iu_srlz_op_encode<9>		0.403 R	<null>
eu_iu_srlz_op_encode<2>		0.525 F	<null>
eu_iu_srlz_op_encode<1>		0.5 R	<null>
eu_iu_srlz_op_encode<0>		0.501 F	<null>
du_iu_store_status<2>	0.625 F	<null>	

***End Node Slopes

```

==> ibm_gray: Starting generation of PathMill IBMgray file. Program version: Version 04/23/98
==> ibm_gray: Writing output messages into file: idcdsuc_mac.ibmgray.log ...
==> ibm_gray: Program finished, now exiting.
==> ibm_gray: Starting generation of PathMill IBMgray file.
==> ibm_gray: Program log file generated by ibm_gray program Version 04/23/98
==> ibm_gray: Program run on: Sun Apr 18 22:23:03 1999
==> ibm_gray: Pathmill version: PATHMILL PM_DEV

```

```

==> ibm_gray: No latches were flagged as NON-TRANSPARENT by the PathMill patterns!

```

```

==> ibm_gray: Data Gathering Phase ....
==> ibm_gray: Storing list of dynamic nodes, latches, and clock gates...

```

```

==> ibm_gray: Total number of dangling nodes found: 0
==> ibm_gray: Gathering data on clock tree nodes...
==> ibm_gray: Gathering data on model segments and nodes...
==> ibm_gray: Writing out the data into file: idcdsuc_mac.ibmgray ...

```

```

==> ibm_gray: Number of PIS found: 0
==> ibm_gray: Number of POS found: 0
==> ibm_gray: Number of LATCHS found: 0
==> ibm_gray: Number of NON-TRANS LATCHS found: 0
==> ibm_gray: Number of DYNAMIC CIRCUITS found: 0
==> ibm_gray: Number of CLOCK GATES found: 0
==> ibm_gray: Number of GLOBAL CLK SEGS found: 0
==> ibm_gray: Number of OTHER PROP SEGS found: 0

```

```

==> ibm_gray: Program finished, now exiting.

```

```

CTE Pathmill post-processor: Determining quality record from configuration file
CTE Pathmill post-processor: Determining clock information from pathmill data
CTE Pathmill post-processor: Determining worst internal setup and hold slacks

```

```

Start writing model file idcdsuc_mac.c
Finished writing model file

```

*** Finished Printing Reports. ***

```

*Info* Pathmill path search finished with a return code of: 0
laceyl: Message sent
This file is not changed; compression does not save space.

```

feedback directory is defaulted to /afs/apd/func/vlsi/alliance00/timing/bsiu/actual/

WARNING no pis record for aa_blk_dcd_pttR, using default
WARNING no pis record for aa_blk_dcd_pttF, using default
WARNING no pis record for bht_block_dcdR, using default
WARNING no pis record for bht_block_dcdF, using default
WARNING no pos record for iu_slow_mode_t1R, using default
WARNING no eta record for iu_slow_mode_t1R, using default
WARNING no pos record for iu_slow_mode_t1F, using default
WARNING no eta record for iu_slow_mode_t1F, using default
WARNING no pos record for iu_reset_op_c_t1R, using default
WARNING no eta record for iu_reset_op_c_t1R, using default
WARNING no pos record for iu_reset_op_c_t1F, using default
WARNING no eta record for iu_reset_op_c_t1F, using default
WARNING no eta record for iu_milli_mode_t2R, using default
WARNING no eta record for iu_milli_mode_t2F, using default
WARNING no pos record for iu_reset_op_c_t1R, using default
WARNING no pos record for iu_reset_op_c_t1F, using default
WARNING no pos record for iu_slow_mode_t1R, using default
WARNING no pos record for iu_slow_mode_t1F, using default
WARNING no eta record for idcdsuc_errR, using default
WARNING no eta record for idcdsuc_errF, using default
WARNING no pos record for iu_reset_op_c_t1R, using default
WARNING no pos record for iu_reset_op_c_t1F, using default
WARNING no pos record for iu_reset_op_c_t1R, using default
WARNING no pos record for iu_reset_op_c_t1F, using default

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Be it known that in connection with my accompanying affidavit and log file appended to an affidavit of Yu-Hing Chan, I, Lisa Bryant Lacey, retrieved the following lines of information, to help clarify. I added a comment in the log "*****POU92000-0107US1***** code invocation" that should the reader of these pages.

```
*****POU92000-0107US1***** code invocation
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
          > critical
repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPER...
critical( repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPERED_PIN_SWAP)
);
-1865.06 Avg: -167.73
maximum area for proto box IDCDSUC is 4606
repower: setting SCORE option to ALL.
repower: setting TAPERED_PIN_SWAP option.
```

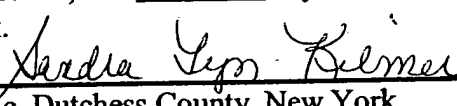
Also, to document the date, note that the log maintains the date when run

```
*****POU92000-0107US1***** code invocation date
Sun Apr 18 21:58:17 1999
Part : IDCDSUC
```



Lisa Bryant Lacey

Sworn to and subscribed before me, this 23rd day of February, 2005
At Poughkeepsie, New York.



Sandra Kilmer, Notary Public, Dutchess County, New York

LYN
SANDRA LYN KILMER
Notary Public, State of New York
No. 6562825
Qualified in Dutchess County
Commission Expires Sept 30, 2006

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